ALPHA LSI QUALITY CONTROL DIAGNOSTIC (QCD)

INTRODUCTION

The ALPHA LSI QCD program verifies the operational capability of the ALPHA LSI computer by means of tests which check the following:

1. Complete instruction repertoire
2. Processor I/O structure
3. Memory integrity
4. Processor-mounted options (teletype, real-time clock, autoload, power fail, and operator console)

ENVIRONMENT

Hardware Required:

1. ALPHA LSI Processor
2. Operator Console
3. 4K read/write memory module

Software Required:

1. Binary Loader (BLD) - not required if Autoload present.
2. QCD Program.

Additional Hardware Supported:

1. Additional memory (up to 32K total)
2. Processor Option Board
3. I/O Test Module

DESIGN FEATURES

QCD provides 13 discrete tests and 4 utility features. The tests are:

1. Instruction diagnostic (IDP)
2. Memory diagnostic (MEM)

3. Internal console test (CON)
4. Real time clock test (RTC)*
5. Autoload ROM verification test (AUT)*
6. I/O instruction and TTY option test (IOT)*
7. Internal I/O test (BRDX)**
8. Real-time clock timing test (RTCX)**
9. Autoload simulation test (AUTX)**
10. Power fail test (PFLX)**
11. Teletype functions test (TELX)**
12. Console functions test (CONX)**
13. Teletype tape test (TTYX)*

*Requires a processor option board
**Requires an I/O test module (These tests are available in extended QCD version 96102-41 only.)

The utility features available are:

1. Memory copy
2. Debug (degraded version of standard Alpha LSI debug)
3. Status summary for each test
4. Resident Bootstrap program

PROGRAM DESCRIPTION

General Design

The standard version of QCD (96102-40) consists of two separate object segments on a single paper tape.

For a system containing 8K or more of memory, the two segments may be loaded contiguously using BLD or Autoload, and run as a complete program.

For a system containing less than 8K of memory, the first segment (which consists of base page data, standard subroutines, and the major portion of IDP) must be loaded using BLD or Autoload, and run as a single program (at least ten minutes of running time is suggested). Then the second segment (consisting of the remainder of IDP and the MEM, CON, RTC, AUT, IOT and TTYX tests) is loaded (overlayed) over IDP segment 1, and run as a second program.

An alternate version of QCD (96102-41) is available upon request from CAI and consists of three separate object segments on a single paper tape. The first two segments are the standard QCD, discussed above. The third segment consists of the I/O test board

tests (BRDX, RTCX, AUTX, PFLX, TELX, and CONX), which require the presence of the I/O test module (part no. 74-53512-00), and appropriate options module. This three-part QCD requires 12K of memory to be loaded contiguously; however, it may be loaded in an overlayed fashion (as discussed above) in as little as 4K.

As each test is being run, the number of the test is displayed in the Console Data Register.

Test Descriptions

Test 1 - Instruction Diagnostic (IDP)

IDP exercises all non-I/O instructions in the ALPHA/LSI instruction repertoire. It determines that each instruction performs as expected and does not affect other volatile registers on memory cells. IDP also develops a check count for each subsection, to insure that no subsection is skipped due to hardware failure. A one- or two-pass mode of IDP may be selected (see QCD Option Selection).

The one-pass mode exercises each instruction without interrupts; while this pass is performed, the hex value : 0001 is displayed in the Console Data Register.

The two-pass mode consists of the non-interrupt pass described above, followed by a second pass, performed under interrupt control. (The second pass runs several times longer than the first pass.) During the second pass, an incrementing pattern is continuously output to the Console Data Register.

Test 2 - Memory Test (MEM)

MEM performs several tests on that area of memory not required for QCD: zeros test, ones test, address test, ripple test, spiral test, worst case pattern test, and byte mode test. For each of the above tests, each word is verified immediately after it has been written into, and again after the entire test area has been written into. During MEM, the Console Data Register displays the following:

Bits 15-8	Memory size, displayed as two hex digits (e.g., 00001000 = 8K, 00010000 = 16K, etc.).
Bits 7-4	An alternating pattern of 0000/1111 to indicate the test is operating correctly.
Bits 3-0	Test number (0010)

Upon completion of the last memory test, if sufficient memory exists (at least twice the length of QCD), QCD is moved to upper memory, and the tests are repeated using low memory as the test area. When QCD is moved to upper memory, it is done in such a way that the first instruction of QCD is moved to the next higher 4K boundary

above the end of the QCD to be moved. (Thus if the 8K version is being run in any memory of 16K or greater, the "relocated" QCD will begin at location : 2000.)

If the memory fails during MEM, the following occurs:

1. A halt (I = : 0824) occurs with the A register containing the actual data and the X register containing the expected data.

2. The operator should now depress RUN.

3. A second halt (I = : 0824) will occur with the A register containing the address of the erroneous data word, and the X register containing the following information:

Bits 0 - 2	Which memory test failed: 000 = Zeros test 001 = Address test 010 = Ripple test 011 = Worst case pattern test 100 = Spiral test 101 = Byte mode test
Bit 3	0 = First (non complement) pass through a particular test (e.g., zeros test pattern = 0000) 1 = Complement pass (e.g., zeros test pattern = FFFF)
Bit 4	0 = Write pass 1 = Verify pass
Bit 7	0 = Standard MEM test to test upper memory 1 = Relocated MEM test to test low memory (QCD moved to upper memory)

NOTE

MEM should not be exited before completion by halting and restarting since you might halt during the time QCD is being relocated in high memory. To abort the test before completion, merely set the SENSE switch, which will cause an immediate, but orderly, exit to the next requested test.

If an error halt occurs in MEM, the correct procedure for continuing or exiting MEM is as follows:

To continue MEM: Press RUN switch.

To exit MEM: Set the SENSE switch on and press the RUN switch.

Test 3 - Console Test (CON)

CON verifies the correct setting, resetting, and sensing of the 8-bit Console Sense Register (overflow, byte mode, interrupt, SENSE switch status, and 4-bit sense register indicators), and the 16-bit Console Data Register, in various combinations of settings. During CON, an incrementing pattern is output to the Console Data Register.

CAUTION

It is possible to produce an error condition during CON by changing the state of the SENSE switch or Console Sense Register during its running, since the console itself is being tested at this time.

Test 4 - Real-Time Clock Test (RTC)

RTC verifies the ability of the real-time clock to generate timing interrupts, with and without sync interrupts. In addition, each non-real-time clock device address except zero is selected to verify that no cross talk occurs. During RTC, the hex value : 0004 is displayed in the Console Data Register.

Test 5 - Autoload Test (AUT)

AUT accesses each instruction from the Autoload ROM, and forms an arithmetic sum of all instructions. This sum is then compared to an expected value within the test. During AUT, the hex value : 0005 is displayed in the Console Data Register.

Test 6 - I/O Instruction Test (IOT)

IOT tests the I/O structure of the ALPHA/LSI by issuing each I/O instruction using the Teletype option full-duplex loop-back diagnostic mode. IOT requires the presence of the teletype option; however, an on-line teletype terminal is not required. If the teletype is on-line, output will be noticeable, in the form of unprintable characters activating the print wheel (no actual printing should take place, however). During IOT, the hex value : 0006 is displayed in the Console Data Register.

Test 7 - I/O Test Board Functions Test (BRDX)

BRDX tests each I/O instruction, with and without interrupts, without requiring the presence of the Teletype option. In addition, IL1/IL2/IUR interrupt priorities, and the I/O stretch features are also tested. During BRDX, the hex value : 0007 is displayed in the Console Data Register.

NOTE

BRDX is included in the extended QCD only (96102-41), and requires the presence of the I/O Test Board.

Test 8 - Real-Time Clock Test (RTCX)

RTCX verifies the operation of the real-time clock at the rates of 100 usec, 1 msec, 10 msec, and twice the line frequency (8.33 msec), by comparing the ratios of each of these rates to each other. During RTCX, the hex value : 0008 is displayed in the Console Data Register.

NOTE

RTCX is included in the extended QCD only (96102-41), and requires the presence of the I/O test board, and the real-time clock option.

Test 9 - Autoload Test (AUTX)

AUTX utilizes the I/O test board to enter Autoload via software control, to insure that Autoload is accessible. ALPHA LSI Autoload contains a diagnostic feature wherein if it is entered with all four bits in the Sense Register set on, it will exit to location : 31. This feature is used in AUTX. During AUTX, the hex value : 0009 is displayed in the Console Data Register.

NOTE

AUTX is included in the extended QCD only (96102-41), and requires the presence of the I/O test board, and the Autoload and Power-Fail options.

Test 10 (:A) - Power Fail Test (PFLX)

PFLX utilizes the I/O test board to simulate a power-down/power-up sequence. Power fails are simulated for standard and offset interrupt locations, as well as under EIN and PFE control. The duration of the power-down sequence is also verified. During PFLX, the hex value : 000A is displayed in the Console Data Register.

NOTE

PFLX is included in the extended QCD only (96102-41), and requires the presence of the I/O test board, and the power fail option.

Test 11(:B) - Teletype Test (TELX)

TELX verifies the ability of the teletype controller to operate with offset interrupts (:2-:6, :22-:26, :102-:106, :122-:126); motor on/off status; step and continuous read modes; 5-, 6-, 7- and 8-bit word lengths; odd, even, or no parity; one or two stop bits; and varying baud rates (75, 110, 134.5, 150, 300, 600, 1200, 1200, 4800, and 9600). During TELX, the hex value :000B is displayed in the Console Data Register.

NOTE

TELX is included in the extended QCD only (96102-41), and requires the presence of the I/O test board and the Teletype option.

Test 12(:C) - Console Test (CONX)

CONX simulates the console interrupt feature, as well as SENSE switch and Sense Register settings, utilizing the I/O test board. During CONX, the hex value :000C is displayed in the Console Data Register.

NOTE

CONX is included in the extended QCD only (96102-41) and requires the presence of the I/O test board.

Test 13(:D) - Teletype Tape Test (TTYX)

TTYX checks to see that the teletype will punch, print, and read tape in conjunction with the ALPHA LSI processor, using step read, continuous read, and auto echo modes of operation. If the operator intends to run this test, he should, before starting QCD, set the teletype punch and reader switches ON, and feed leader from the punch into the read station. (Correct operation of this test will not be affected by punched-tape residue from the other parts of QCD which output to the teletype, namely IOT and the Status Report).

The expected print pattern for this test is:

ABCDEFG
ABCDEFG

GFEDCBA

During TTYX, the hex value : 000D will be displayed in the Console Data Register.

TTYX is requested by setting bit 0 of the Console Sense Register ON.

Status Report

The QCD Status Report is output to the teletype after each pass through the requested test sequence, unless suppressed by setting bit 1 of the Console Sense Register ON.

The Status Report includes:

1. The Option key (4 hex characters representing the test options entered by the operator upon entering QCD).

2. Memory Size, in hexadecimal (e.g., if memory size = 8K, "1FFF" will be output), and decimal (e.g., "8K").

3. Number of passes made through the test sequence, in hexadecimal.

4. The number, in hexadecimal, of power-down/power-up count miscompares occurring since entering QCD.

5. A listing of each requested test number and name, followed by the status for that test:

   "RUN" - Test completed (successfully, if no halts occurred within the test itself).

   "INSUFF MEMORY - Test 2 (MEM)
   Tested all available memory, which was not sizeable enough to permit moving QCD to test low memory.

   "NO OPTION" - Test was specifically requested, but not run because the presence of a required hardware option could not be sensed.

The status report may be exited at any time before its completion by typing a combination "CNTRL" and "X" character while the report is being printed.

QCD Debug

The resident DEBUG routine is a subset of the standard DEBUG program (96004) including the following functions:

"B" Single (not double) breakpoint

"C" Copy memory

"F" Fill memory

"P" Print memory

"S" Search memory (masked search not included)

"J" Jump to memory

"I" Inspect memory - includes inspecting the next higher memory location (space) or the previous location (comma)

"A" Inspect or change A register

"X" Inspect or change X register

"O" Inspect or change the 8-bit status word

In addition, an offset feature is included (only for use in the 4K - overlay - version of QCD) to assist in accessing locations in the second segment of QCD, the addresses of which will not correspond with the addresses shown in the Segment 2 listing. The offset feature is used as follows:

If the user wishes to access a memory location in Segment 2 and knows the listing address but not the actual address in memory, he should enter the address, followed by a minus (-) character; e.g., to inspect relative address :1237, enter

I1237-.

Debug will subtract the offset factor from :1237 automatically, and display the actual address, followed by its contents.

If the user knows the actual address in memory (for example, the P register contents upon an error halt), and wishes to determine the Segment 2 listing address in order to locate the halt and its explanation in the listing, he should enter the actual address followed by a plus (+) character; e.g., to determine the relative (listed) address which corresponds to the actual location :1000, enter

I1000+.

Debug will add the offset factor to :1000 and display the relative address, followed by the contents of the address shown on the teletype. (These contents will normally not be applicable to the operation.)

The offset (+ or -) feature may be used in conjunction with any of the included Debug functions. Also, offset and non-offset addresses may be mixed in a single function; for example, the following input:

B13F 1209-.

will cause a breakpoint function to be performed from actual location :13F to relative (to Segment 2) address :1209.

NOTE

The offset (+ or -) characters may not be used as arithmetic operators; e.g.,

I397+1.

has no meaning, and will produce an incorrect address.

Copy Utility

The Copy Utility permits copying of QCD into each 8K segment of memory. It is entered at its starting address (the listing address (see Appendix B) offset by the 8K segment in which the copy feature resides) and automatically copies the 8K memory module in which it resides, into every other 8K memory module.

Resident Bootstrap Program

A standard teletype bootstrap routine is included in QCD (at TBOOT; See Appendix B), which may be used when MEM destroys data in upper memory.

PROGRAM OPERATION

QCD Option Selection

When entering QCD, the desired tests must be requested via the A register prior to entering the RUN mode (See Table A1-1). Each bit of the A-register represents a different test or option. In addition, the 4-bit Sense Register is used to select additional options (See Table A1-2).

Any combination of options may be used; the following rules apply:

1. IDP, in whichever mode is selected (one-pass or two-pass) is always run at the start of each pass, whether A-register bit 1 is set or not; the purpose of bit 1 is to permit the running of IDP by itself, with no other tests selected.

2. Tests requested via the A-register may only be set at the start of QCD.

3. Options requested via the SENSE Register may be altered at any time.

4. If the Load-and-Go feature of Autoload or LAMBDA is used, QCD is entered with the A-register and SENSE Register set to zero.

5. If memory size is less than 8K, the overlay mode of loading QCD must be used. Thus selection of a non-resident test or option is meaningless. The following lists define the contents of each segment:

Segment 1

Test 1 (IDP - part 1)

Segment 2

Test 1 (IDP - part 2)
Test 2 (MEM)
Test 3 (CON)
Test 4 (RTC)
Test 5 (AUT)
Test 6 (IOT)
Test 13 (:D) (TTYX)
Status Report

Segment 3 (Extended version only)

Test 7 (BRDX)
Test 8 (RTCX)
Test 9 (AUTX)
Test 10 (:A) (PFLX)
Test 11 (:B) (TELX)
Test 12 (:C) (CONX)
Status Report

Common to all Segments

Power Fail Handling
Console Interrupt Testing
QCD Debug
Copy Utility

Console Interrupt Testing

The console interrupt feature is not tested in a particular test. It may be tested at any time by the operator, by pressing the "INT" switch. If the console interrupt is successful, the console display lights will blink an alternating :AAAA/:5555 pattern, and the BYTE indicator, SENSE switch, OV (overflow) indicator, and all four sense register bits will light, for approximately five seconds.

NOTE

The console interrupt feature is suppressed during IOT, pass 2 of IDP and the second half of MEM (that portion of MEM in which QCD resides in upper memory). However, if the console interrupt switch is depressed while in this portion of MEM, the indicator above the switch should stay on (pending) until MEM completes, at which time the flashing display will occur.

Power-Fail Handling

Operation of the Power-Fail option is tested in PFLX. In addition, safeguards against unexpected power failures have been included in the QCD program.

When a power failure occurs, a power-down interrupt is executed, the A, X, Status, and Console Data register are saved, and a power-down tally is incremented. A halt is then entered until power is restored.

When power is restored to the computer, it automatically begins execution at location :0000. At this time a power-up tally is incremented, and the totals of power-downs and power-ups are compared for equality. The address of the location to be executed when the power failure occurred is examined. If it is beyond the end of Test 3 (CON), the program is restarted in IDP, using the options previously requested by the user. If the interrupted address is within the area from Test 1 through Test 3, a return is made to the point at which the interrupt occurred.

In addition, an option exists (bit 3 of the SENSE Register set ON) which causes IDP to avoid an error halt upon occurrence of a power-down/power-up tally miscompare. (The Status Report will note the number of miscompares, whether or not the error halt is executed.) When this option is used, QCD will re-enter at IDP.

Autoload Testing

Certain aspects of the Autoload feature are tested in the AUT and ATUX tests (see Test Descriptions).

In addition, the diagnostic feature contained in Autoload itself may be tested at any time by the user, after QCD has initialized location : 31, as follows:

1. Enter the Run Enable mode, by setting the STOP and RUN indicators off.

2. Enter : F into the Console Sense Register.

3. Press the AUTO switch.

4. If Autoload has been accessed successfully, a halt should occur at location : 31 (P = : 32, I = : 801), since the Autoload diagnostic mode (all sense bits on) causes an unconditional jump to absolute location : 31, which in QCD always contains : 801.

   CAUTION

   Do not depress RUN upon this halt, as a runaway condition will occur within the QCD data area.

Error Handling

When a hardware error is detected, the computer will halt with the following information in the I register:

Bits 15-8	: 08
Bits 7-4	Test number, in binary
Bits 3-0	Type of error:

0000 = unclassified
0001 = instruction failure (non-I/O)
0010 = instruction failure (I/O)
0100 = Memory error
1000 = Interrupt failure

In addition, the A and X registers may contain pertinent information. To determine the exact nature of the error, the halt location (P register contents-1) should be located in the listing, wherein an annotated error description will be found. Depression of the RUN switch upon an error halt will continue the program.

Required Hardware Options for Each Test

IDP	None
MEM	None
CON	Console
RTC	Real-Time Clock
AUT	Autoload
IOT	Teletype option (teletype terminal not required)
TTYX	Teletype, on-line
BRDX	I/O Test Board
RTCX	I/O Test Board, Real-Time Clock option
AUTX	I/O Test Board, Autoload option, Power-Fail option
PFLX	I/O Test Board, Power-Fail option
TELX	I/O Test Board, Teletype option
CONX	I/O Test Board
Status Report	On-line Teletype

Offset Interrupts

QCD assumes offsets to be at their standard, non-offset locations. However, QCD may be run using offset interrupts, which requires the following program modification:

NOTE

This change must be made when QCD is first loaded.

QCD LABEL	ABSOLUTE MEMORY LOCATION	DESCRIPTION
"OFFSET"	:2A	Nominally = :0000. Change to :0100 for standard offset.
"TTYOFF"	:2B	Nominally = :0002. Change to :0022 for teletype offset.

Important Memory Locations

Label	Address	Description
QCDENT	:100 (ABS)	Entry point to QCD (default). A register unconditionally set to zero.

Label	Address	Description
QCD1NT	:101 (ABS)	Selective entry point to QCD. This is the starting location when specific tests have been entered in the A register.
QCD4NT	:115 (ABS)	Re-entry point. Does not reset power-fail history or pass counter. A-register must be set to tests requested before entering here.
BOOTNT	:116 (ABS)	Teletype Bootstrap routine
DEBUG	:120 (ABS)	QCD DEBUG routine
COPY	:121 (ABS) or :2121 (ABS) or :4121	Copy Utility entry point.
Q01001	:316 (ABS)	Start of overlay (2) when running QCD in less than 8K. This is the starting load address needed by BLD or Autoload when overlaying Segments 2 and 3.
Q12000	:FAD (ABS)	Start of Segment 2 when running QCD in 8K or more memory. This is the starting load address needed by BLD or Autoload when loading (but not overlaying) Segment 2.

Appendix A

QCD OPERATION SUMMARY

The procedure to load QCD into memory with Autoload or BLD is as follows:

Contiguous Load - requires at least 8K of memory for Standard QCD 96102-40, or at least 12K for Extended QCD 96102-41. If insufficient memory, the overlayed load method must be used (see Overlayed Load below):

1. Enable the Console by moving the Console Enable slide switch (located in the recess on the right side of the Console) to the enable position (up). The ENABLE indicator on the front panel will turn on.

2. If required, load BLD into memory using the Bootstrap procedure (location : 1FBO for 8K, : 2FBO for 12K).

3. If the STOP indicator is off, press the STOP switch to halt the computer. The indicator will turn on.

4. Press the RESET switch to clear the computer.

5. Set the A and X registers to : 0000; and if using BLD set the P register to the first location of BLD (: 1FBO for 8K, : 2FBO for 12K, etc.).

6. Load the 4-bit Console Sense Register with : 8 for teletype load, or : 9 for high speed reader load.

7. Reset the SENSE switch. The indicator will turn off.

8. Load the QCD tape into the selected reader (TTY or HSR) and ready the device.

9. Reset the STOP switch to enable operation (STOP indicator will turn off).

10. Press the RUN (for BLD) or AUTO (for Autoload) switch to load Segment 1 of QCD. Computer will halt with I = : 0800 if load successful.

11. Press RUN (for BLD) or auto (for Autoload) to load Segment 2. Computer will halt with I = : 0800 for successful load.

12. If loading extended QCD (version 96102-41), Press RUN (for BLD) or AUTO (for Autoload to load Segment 3. Computer will halt with I = : 0800 if load successful.

13. Enter the desired tests and options into the A register and Console Sense Register (see QCD Option Selection, Appendix B).

14. If Test 13 (TTYX) is selected (bit 0 of the Console Data Register ON), feed leader from the teletype punch into the teletype reader, and turn the punch and reader ON.

15. Begin execution of QCD at location : 0101.

Overlayed Load (BLD or Autoload) - assumes less than 8K of memory for standard QCD 96102-40, or less than 12K for extended QCD 96102-41:

1. Enable the Console by moving the Console Enable slide switch (located in the recess on the right side of the Console) to the enable position (up). The ENABLE indicator on the front panel will turn on.

2. If required, load BLD into memory using the Bootstrap procedure (location : 0FB0 for 4K, : 1FB0 for 8K).

3. If the STOP indicator is off, press the STOP switch to halt the computer. The indicator will turn on.

4. Press the RESET switch to clear the computer.

5. Set the A and X registers to : 0000; and if using BLD, set the P register to the first location of BLD (: 0FB0 for 4K, : 1FB0 for 8K, etc.).

6. Load the 4-bit Console Sense Register with : 8 for teletype load, or : 9 for high speed reader load.

7. Reset the SENSE switch. The indicator will turn off.

8. Load the QCD tape in the selected reader (TTY or HSR) and ready the device.

9. Reset the STOP switch to enable operation (STOP indicator will turn off).

10. Press the RUN (for BLD) or AUTO (for Autoload) switch to load Segment 1 of QCD. Computer will halt with I = : 0800 if load successful.

11. Load the A register with : 0000 to run the 1-pass IDP test, or : 0001 to run the 2-pass IDP test (see TEST DESCRIPTIONS, Test 1).

12. Enter QCD at location : 0101. It is advisable to run this portion of QCD for at least ten minutes before loading Segment 2.

13. To load Segment 2, repeat steps 3 through 10 with the X register set to :316 (beginning of QCD overlay area).

14. Enter the desired tests and options into the A register and Console Sense register (see QCD Option Selection, Appendix B).

15. If QCD is being loaded through the teletype, remove the tape at this time to permit teletype testing. In addition, if Test 13 is selected (TTYX), feed paper tape leader from the teletype punch into the reader, and turn the punch and reader ON.

16. Enter QCD at location :0101. The selected tests may then be cycled indefinitely.

17. To load and execute Segment 3 (Extended QCD, version 96102-41 only); repeat steps 3 through 10 and 14 through 16.

Appendix B

QCD TEST AND OPTION SELECTION

Test Selection

Test No.	Name	A register bit set															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	IDP (2-Pass)																X
1	IDP (1-Pass)															X	
2	MEM														X		
3	CON													X			
4	RTC												X				
5	AUT											X					
6	IOT										X						
7	BRDX									X							
8	RTCX								X								
9	AUTX							X									
10(:A)	PFLX						X										
11(:B)	TELX					X											
12(:C)	CONX				X												
Unused				X													
Unused			X														
MEM Option		X															

Option Selection

Option Desired	Sense Register Bit On			
	3	2	1	0
Run TTYX (Test 13)				X
Suppress Status Report			X	
Halt after each pass of QCD		X		
Bypass error halt upon power down/up count miscompare	X			

SENSE switch set: Abort MEM test.

Additional Options

1. Default mode - A register bits 14-0 = 0. This option will cause each Test (1-12) to be run consecutively. If a missing hardware option is sensed, the normal error halt will be bypassed.

2. MEM option - A register bit 15 = 1. This option will prevent MEM, if run, from relocating QCD to high memory, even if there is sufficient memory to do so.