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GEC PLESSEY
SEMICONDUCTORS

MAY 1994

DS3005-2.0

ZN425E8

8-BIT D-A/A-D CONVERTER

The ZN425 is a monolithic 8-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches, and in addition a counter and a 2.5V precision voltage reference. The counter is a powerful addition which allows a precision staircase to be generated very simply by clocking the counter.

FEATURES

- $\pm^1/_2$ LSB Linearity Error
- 0°C to +70°C
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time (D-A) 1µs Typical
- Conversion Time (A-D) 1ms Typical, using Ramp and Compare Technique
- Extra Components Required

  D-A: Reference Capacitor (Direct Voltage Output through 10kOhms Typ.)

  A-D: Comparator, Gate, Clock and Reference Capacitor

ORDERING INFORMATION

Ambient operating temperature 0°C to +70°C
PackageDP16

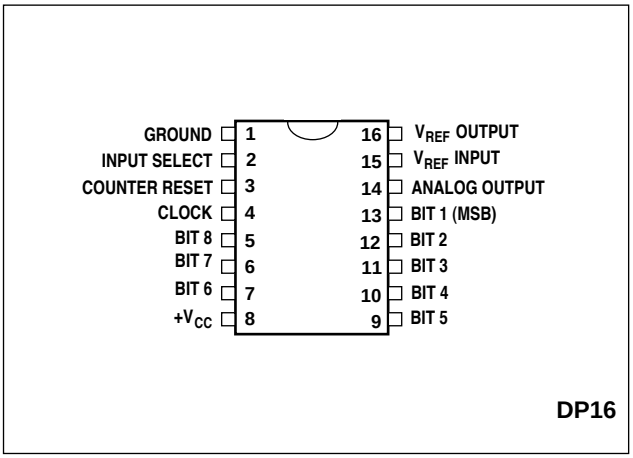

Fig.1 Pin connections (not to scale) - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7.0V
Max. voltage, logic and V_{REF} inputs	+5.5V See note 3
Operating temperature range	0°C to +70°C
Storage temperature range	-55°C to +125°C

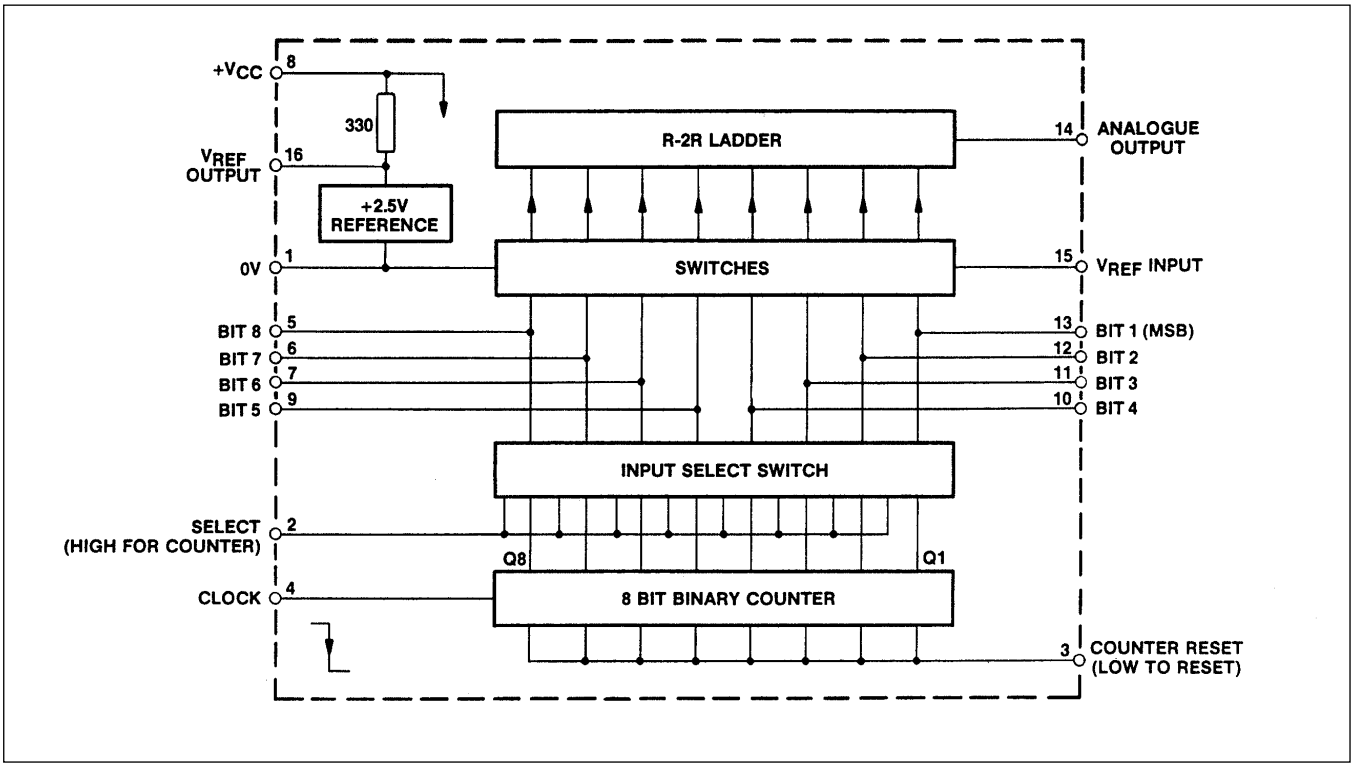

Fig.2 System diagram

ELECTRICAL CHARACTERISTICS

(at T_{amb} = 25°C and V_{CC} = +5V unless otherwise stated)

INTERNAL VOLTAGE REFERENCE

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output voltage	V_{REF}	2.4	2.55	2.7	V	I = 7.5mA (internal)
Slope resistance	R_S	-	2	4	Ω	I = 7.5mA (internal)
V_{REF} temperature coefficient		-	40	-	ppm/°C	I = 7.5mA (internal)

NOTE: The internal reference requires a 0.22µF stabilising capacitor between pins 1 and 16.

8-BIT D-A CONVERTER AND COUNTER

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Resolution		8	-	-	bits	
Non-linearity		-	-	±0.5	LSB	see note 3
Differential non-linearity		-	±0.5	-	LSB	see note 6
Settling time		-	1.0	-	µs	1LSB step
Settling time to 0.5LSB		-	1.5	2.5	µs	All bits ON to OFF or OFF to ON
Offset voltage ZN425E8	V_{OS}	-	3	8	mV	All bits OFF See note 3
Full-scale output		2.545	2.550	2.555	V	All bits ON Ext. V_{REF} = 2.56V
Full-scale temp. coefficient		-	3	-	ppm/°C	Ext. V_{REF} = 2.56V
Linearity error temp.coeff.		-	7.5	-	ppm/°C	relative to F.S.R.
Analog output resistance	R_O	-	10	-	kΩ	
External reference voltage		0	-	3.0	V	
Supply voltage	V_{CC}	4.5	-	5.5	V	See note 3
Supply current	I_S	-	25	35	mA	
High level input voltage	V_{IH}	2.0	-	-	V	See notes 1 and 2
Low level input voltage	V_{IL}	-	-	0.7	V	
High level input current	I_{IH}	-	-	10	µA	V_{CC} = max. V_I = 2.4V
		-	-	100	µA	V_{CC} = max. V_I = 5.5V
Low level input current bit inputs	I_{IL}	-	-	-6.8	mA	V_{CC} = max. V_I = 0.3V
Low level input current, clock reset and input select	I_L	-	-	-0.18	mA	

ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
High level output current	I_{OH}	-	-	-40	µA	
Low level output current	I_{OL}	-	-	1.6	mA	
High level output voltage	V_{OH}	2.4	-	-	V	V_{CC} = min. Q = 1 I_{load} = -40µA
Low level output voltage	V_{OL}	-	-	0.4	V	V_{CC} = min. Q = 0 I_{load} = 1.6mA
Maximum counter clock frequency	f_c	3	5	-	MHz	See note 5
Reset pulse width	t_R	200	-	-	ns	See note 4

NOTES:
1. The input select pin (2) must be held low when bit pins (5, 6, 7, 9, 10,11,12, and 13) are driven externally.
2. To obtain counter outputs on bit pins the select pin (2) should be taken to $+V_{CC}$ via a 1kΩ resistor.
3. (a) Maximum operating voltage. Between 70°C and 125°C the maximum supply voltage is reduced to 5.0V.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
4. The device may be reset by gating from its own counter.
5. F_{max} in A-D mode is 300kHz, see Operating Note 2.
6. Monotonic over full operating temperature range.

INTRODUCTION

The ZN425 is an 8-bit dual mode D-A/A-D converter. It contains an 8-bit D-A converter using an advanced design of R-2R ladder network and an array of precision bipolar switches plus an 8-bit binary counter and a 2.5V precision voltage reference all on a single monolithic chip.

The special design of the ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip voltage reference is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

By including an 8-bit binary counter on the chip, A-D conversion can be obtained simply by adding an external comparator (LM311) and clock inhibit gating (7400).

By simply clocking the counter the ZN425 can be used as a self-contained precision ramp generator.

A logic input select switch is incorporated which determines whether the precision switches accept the outputs from the binary counter or external digital inputs depending upon whether the control signal is respectively high or low.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig.3.

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

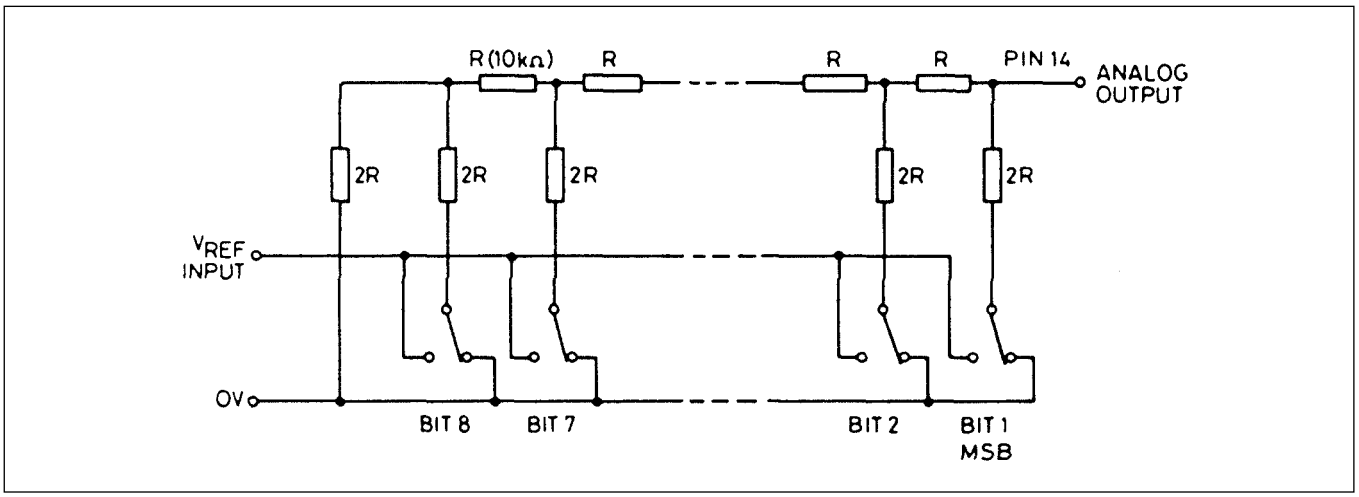

Fig.3 The R-2R ladder network

If pin 2 is high then the output equals the Q output of the corresponding counter.

If pin 2 is low then the output transistor, Tr1 is held off.

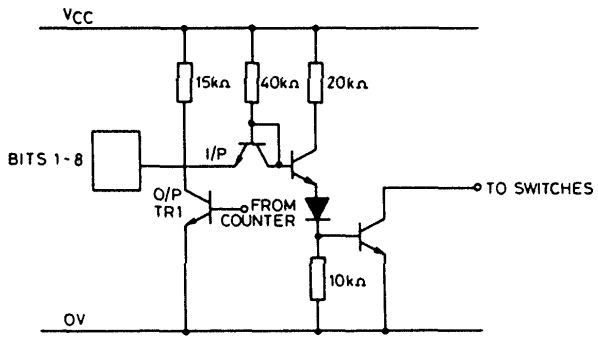

Fig.4 Bit inputs/outputs

OPERATING NOTES

1. 8-bit D-A Converter

The ZN425 gives an analog voltage output directly from pin 14 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the analog output resistance R_O, will be less than 0.004% per °C (or 1LSB/100°C) if R_L is chosen to be ≥ 650kΩ.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig.5 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{OUT} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{OUT} = Nominal full-scale reading - 1LSB

iii. Repeat i. and ii.

e.g. Set F.S.R. to + 3.840V - 1LSB
=3.825V

(1LSB = $\frac{3.84}{256}$ =15.0mV)

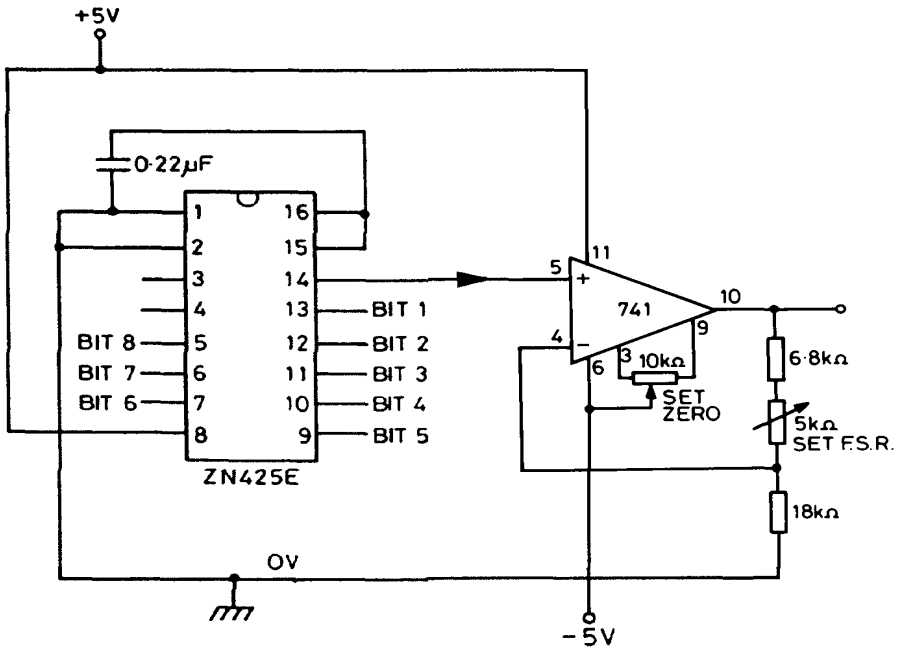

Fig.5 8-bit D-A converter

2. 8-bit A-D Converter

A counter type ADC can be constructed by adding a voltage comparator and a latch as in Fig.6. On the negative edge of the CONVERT COMMAND pulse (15µs minimum) the counter is set to zero and the STATUS latch to logical 1.On the positive edge the gate is opened, enabling clock pulses to be fed to the counter input of the ZN425. The minimum negative clock pulse width of the ZN425 is 100ns. The analog output of the ZN425 ramps until it equals the voltage on the other input of the comparator. At this point the comparator output goes low and resets the STATUS to inhibit further clock pulses. The logical 0 from the status latch indicates that the 8-bit digital output is a valid representation of the analog input voltage.

A small capacitor of 47pF is added to the ZN425 output to stop any positive going glitches prematurely resetting the status latch. This capacitance is in parallel with the ZN425 output capacitance (20-30pF) and they form a time constant with the ZN425 output resistance (10kΩ). This time constant is the main limit to the maximum clock frequency. With a fast comparator the clock frequency can be up to 300kHz. The conversion time varies with the input being a maximum for full-scale input.

Maximum conversion time =

$$\frac{256}{\text{clock frequency in Hz}} \text{ seconds}$$

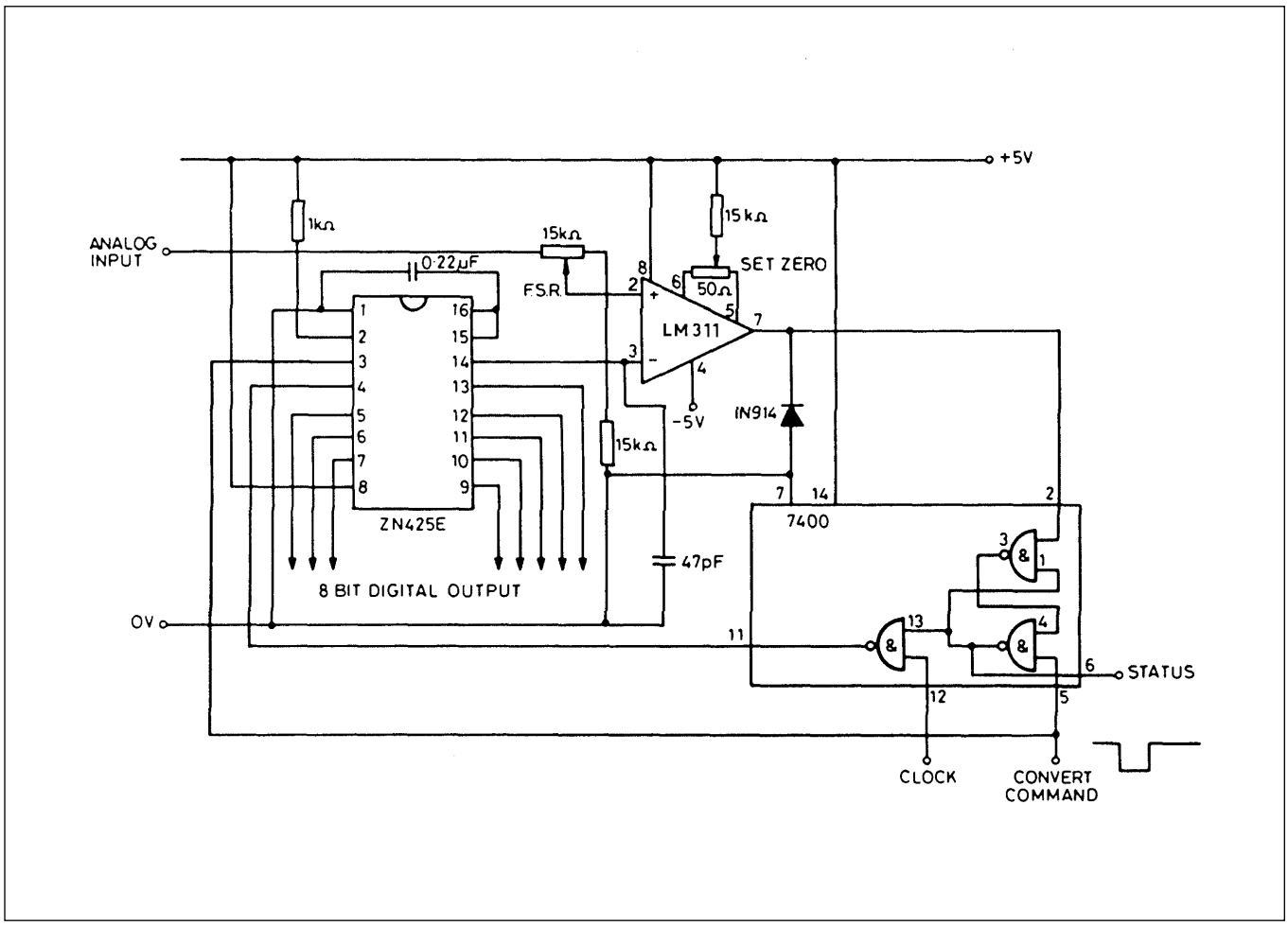

Fig.6 8-bit A-D converter

3. Precision Ramp generator

The inclusion of an 8-bit binary counter on the chip gives the ZN425 a useful ramp generator function. The circuit, Fig. 7, uses the same buffer stages as the D-A converter. The calibration procedure is also the same. Holding pin 2 low will set all bits to ON and if RESET is taken low with pin 2 high all the bits are turned OFF. If the end voltages of the ramp are not required to be set accurately then the buffer stage could be omitted and the voltage ramp will appear directly at pin 14.

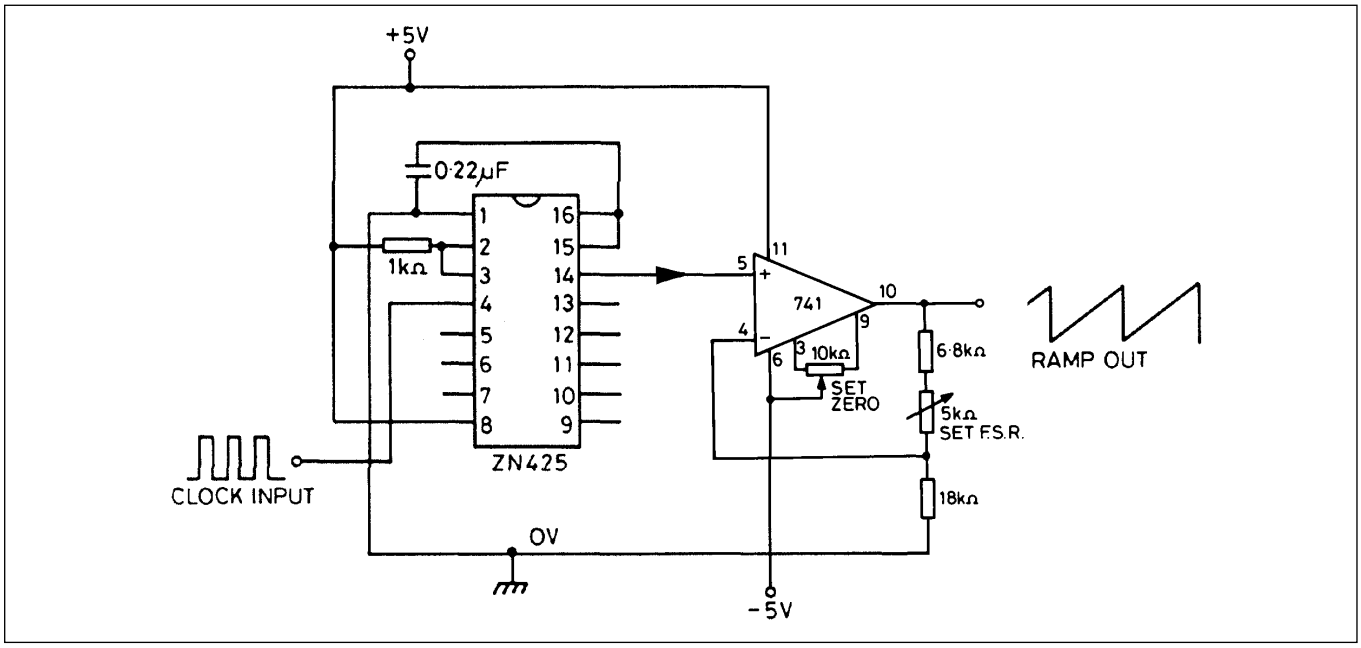

Fig.7 Precision ramp generator

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