SHIPPING REQUIREMENTS

Packing form is shown in Figure 13.

Carton Storage Conditions

- Number of layers of cartons in pile: 10 layers maximum.
- Environmental conditions:
  - Temperature: 0°C to 40°C.
  - Humidity: 60% RH or less (at 40°C). No dew condensation even at a low temperature and high humidity.
  - Atmosphere: Harmful gases such as acid and alkali which corrode electronic components and wires must not be detected.
  - Storage Period: Approximately three months.
  - Opening of Package: To prevent the TFT-LCD module from being damaged by static electricity, adjust the room humidity to 50% RH or higher and provide an appropriate measure for electo-static grounding before opening the package.

Result Evaluation Criteria

Under the display quality test conditions with normal operation state, there shall be no change which may affect practical display function.

OTHER INFORMATION

If any problem should arise from this specification, the supplier and user should work out a mutually acceptable solution.

COCOM

This product falls under 'strategic product' according to the export trade control ordinance in force. -Export **of** the item requires an export license issued by the related authorities.

Please confirm with Sharp whether the license is necessary since the ordinance may be revised by the authori-ties.

RELIABILITY TEST ITEMS

NUMBER	TEST ITEM	CONDITIONS
1	High Temperature Storage Test	t_A = 60°C, 240 H
2	Low Temperature Storage Test	t_A = –25°C, 240 H
3	High Temperature and High Humidity Operation Test	t_A = 40°C, 95% RH, 240 H
4	High Temperature Operation Test	t_A = 40°C, 240 H
5	Low Temperature Operation Test	t_A = 0°C, 240 H
6	Electrostatic Discharge Test	t-200 V, 200 pF (0 Ω), Once for each terminal
7	Shock Test	100 G, 6 ms, ±X/±Y/±Z, three times for each direction (JIS C7021, A-7 Condition C)
8	Vibration Test	Frequency range: 10 to 55Hz Stroke: 1.5 mm Sweep: 10 Hz to 55 Hz to 10 Hz Two hours for each direction of X/Y/Z (six hours total) (JIS C7021, A-10 Condition A)
9	Heat Shock Test	-25°C to +60°C/5 cycles, (two hours/cycle) (1H) (1H)

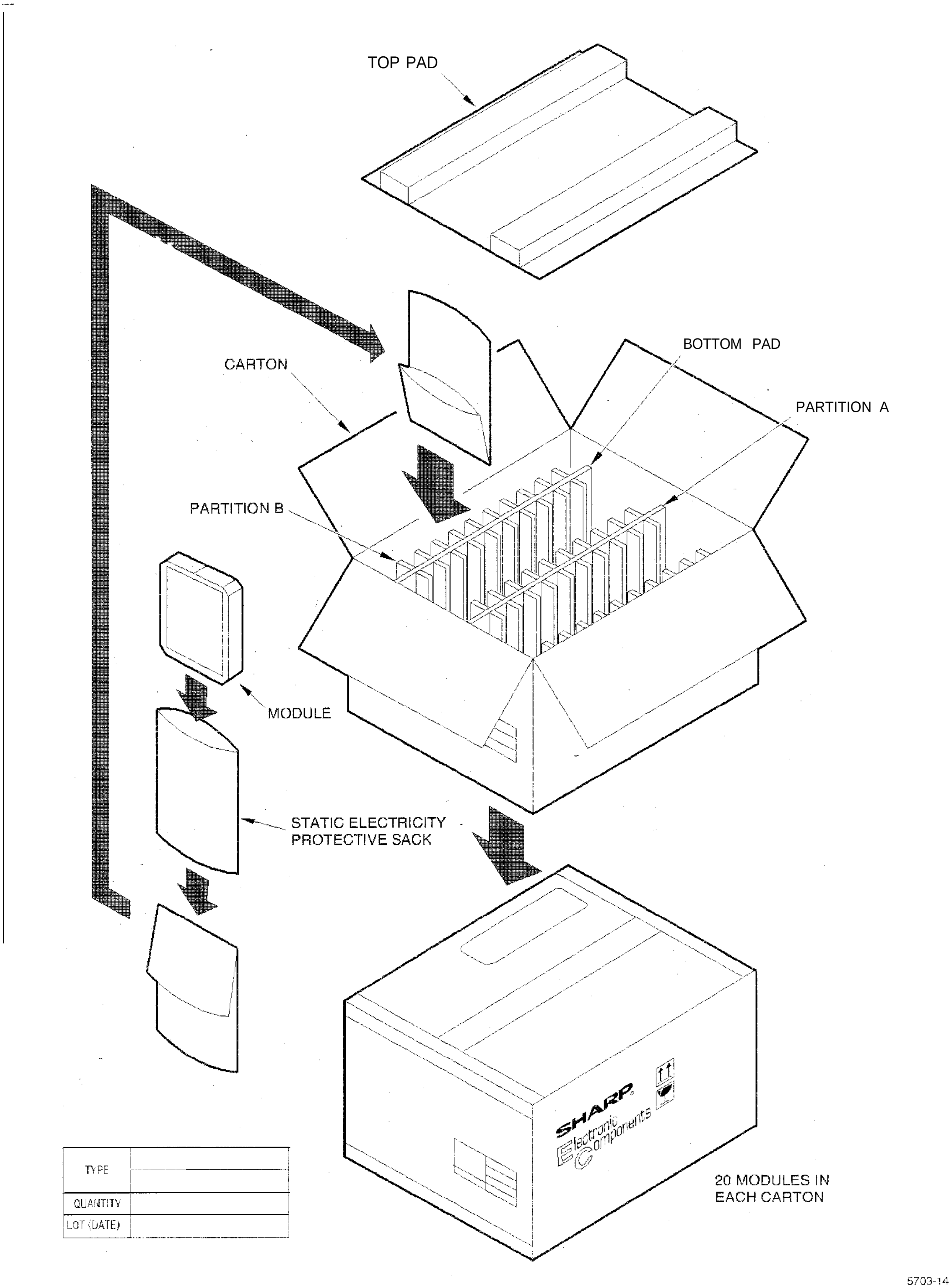


Figure 13. Packing Form

CONSTRUCTION OF TFT-LCD MODULE

TFT-LCD module is composed of an LCD panel, driver ICs for the LCD panel, a control circuit for the driver ICs, a video signal processing circuit (video interface circuit) peculiar to LCD, and a backlight.

The driver ICs, are divided into two types: a source driver (data driver) which receives RGB signals and sends them sequentially by one horizontal line of the LCD panel, and a gate driver (scan driver) which scans 240 gate lines of **the** LCD panel.

The circuit diagram is shown in Figure 3.

The module displays an image on the LCD panel as it receives power supplies (V_{SH}, V_{SL}), composite video signal, RGB video signals, DC **bias** voltage of common electrode driving signal (V_{CDC}), selection signal of composite and RGB video signals (VSW), brightness adjusting DC voltage (BRT), color gain adjusting DC voltage (COL), tint adjusting DC voltage (TIN), and contrast adjusting DC voltage (CNT), from the exterior.

The composite video signal is subject to synchronous separation in the module and used to write a video signal accurately on each pixel on the module.

The control circuit receives composite synchronizing signal separated in the video interface circuit, generates clock pulses synchronized with the com**posite** synchronizing signal and gate and source drivers-driving signals, and outputs internal horizontal synchronizing signal (HSY), internal vertical synchronizing signal (VSY) and polarity inversion signal (FRP).

The voltage level of RGB video signals applied to the liquid crystal layer of each pixel through the source driver and TFT is about 3.7 Vp.p. from black to white level. In order to prevent the electro-chemical decomposition of the liquid crystal, it is necessary to **apply AC** voltage to the liquid crystal. For this purpose, the polarity of the video signals must be alternated. Since the amplification and polarity inversion of the video signals are performed in the video interface circuit in the module using the polarity inversion signal (FRP), **composite** video signal of 1.0 Vp.p. or standard analog RGB signals of 0.7 Vp.p. may be used for both of the inputs to the module.

Power supplies to this module are 5 V (V_{SH}), 0 V (GND), and -8 V (V_{SL}). Control IC operates on 0 V to 5 V line so that it outputs HSY and VSY at 0 V to 5 V level. Power supplies to the video interface circuit are V_{SH} and V_{SL}.

VSW is used to select **composite** or RGB video signals. VSW selects composite video signal when it is 'High' or open, and selects RGB signals when it is 'Low.'

BRT, COL TIN, CNT and V_{CDC} are adjusted to the optimum value on shipping.

The module contains backlight (cold cathode fluorescent tubes) but not a driving circuit for the backlight. Therefore, it is necessary to install a DC/AC inverter for driving the fluorescent tubes.

Standard DC/AC inverter (Model name: LQOJO4 is available as an option.

In addition, the backlight of the module is designed to be replaceable, and backlight unit (Model name: LQ0B04) is available as a service par-t for the replacement.

EXAMPLE OF TFT-LCD TV

Figure 14 shows a block diagram example of the TFT-LCD module applied to a TV set.

The block enclosed by the dotted line is the TFT-LCD module.

Other signal processing systems are the **same as** those in ordinary CRT-TVs.

The following seven signals must be supplied to this module from the exterior:

- Composite video signal: VBS
- Standard analog RGB video signals
- Signal for selecting input video signals: VSW
- DC bias voltage **of** common electrode driving signal: Vcoc
- Brightness adjusting DC voltage: BRT
- Color gain adjusting DC voltage: COL
- Tint adjusting DC voltage: TIN

The following two signals are output from this module **to** the exterior:

- Internal horizontal synchronizing signal: HSY
- Internal vertical synchronizing signal: VSY

When this module is applied to a TV set, for example, HSY and VSY are used to display selected channel number and characters on the screen.

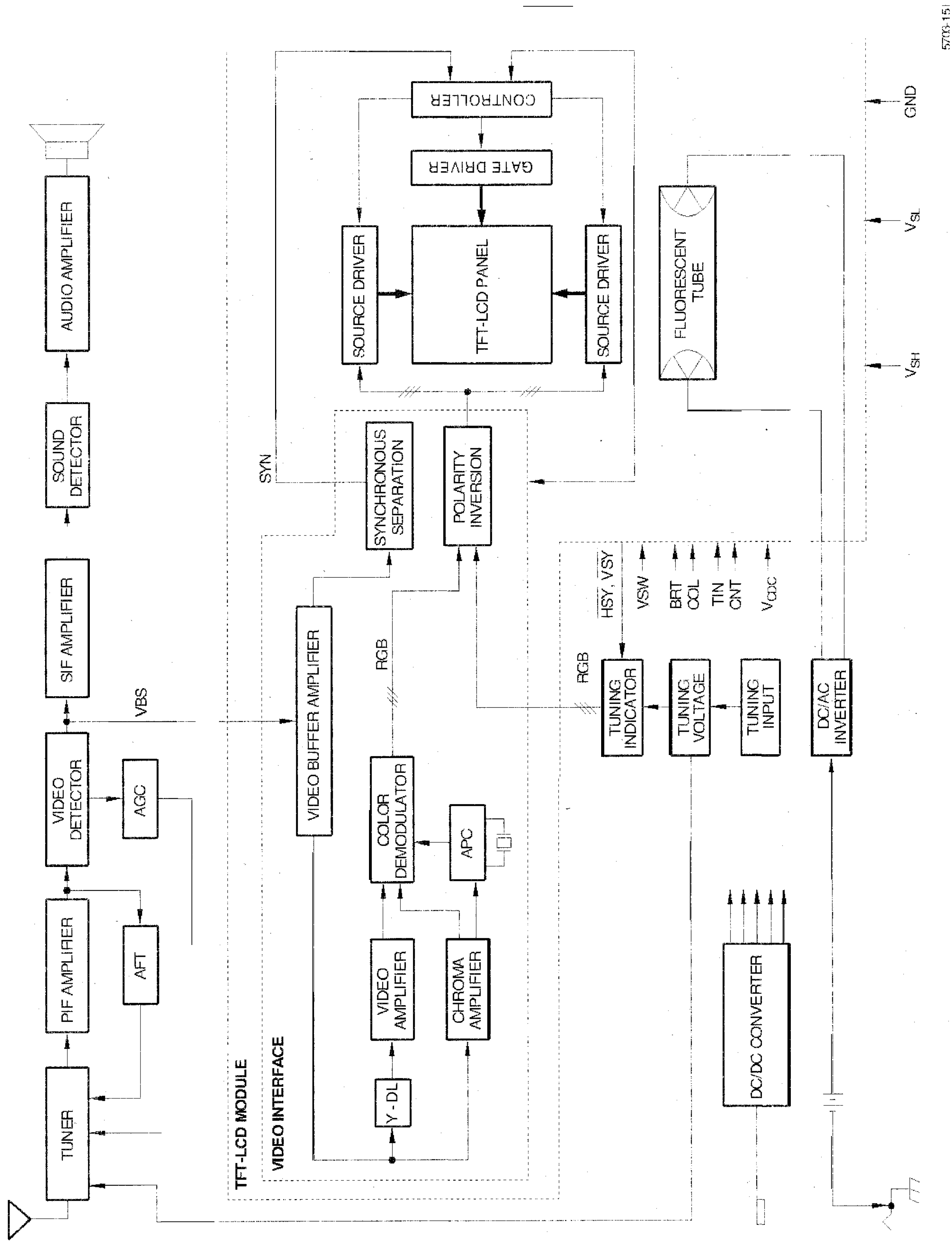


Figure 14. **Block Diagram of** TFT-LCD TV Set

ADJUSTING METHOD OF OPTIMUM COMMON ELECTRODE DC BIAS VOLTAGE

To obtain optimum DC bias voltage of common electrode driving signal (V_{CDC}), photoelectric devices are very effective, and the accuracy is within 0.1 V. (In visual examination method, the accuracy is about 0.5 V because of the difference among individuals.)

To gain optimum common electrode DC bias voltage, there are two methods which use photoelectric devices. The value of optimum DC bias voltage is the same in both methods:

- Measurement of Flicker:
  DC bias voltage is adjusted so as to minimize 60 Hz (30 Hz) flicker.
- Measurement of Contrast:
  DC bias voltage is adjusted so as to minimize the photoelectric output voltage.

Measurement of Flicker

Photoelectric output voltage is measured by an oscilloscope at a system shown in Figure 15.

DC bias voltage must be adjusted to minimize the 60 Hz (30 Hz) flicker with DC bias voltage changing slowly (Figure 16).

Measurement of Contrast

Photo-electric output voltage is measured by oscilloscope or X-Y recorder by using the system in Figure 15. Common electrode DC bias voltage must be adjusted so as to minimize the photoelectric output voltage with DC bias voltage changing slowly (Figure 17).

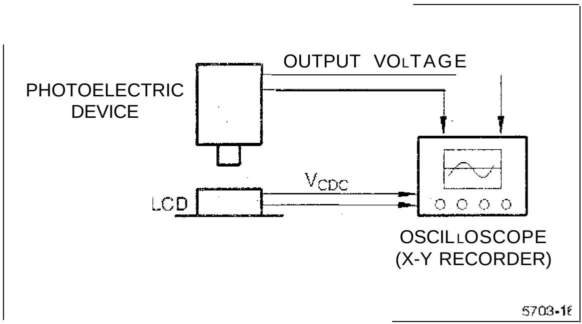
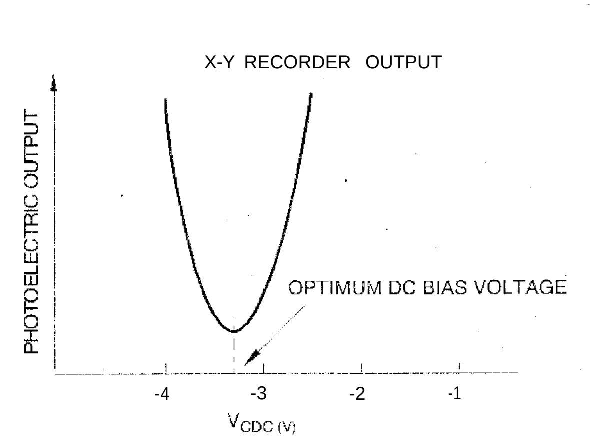


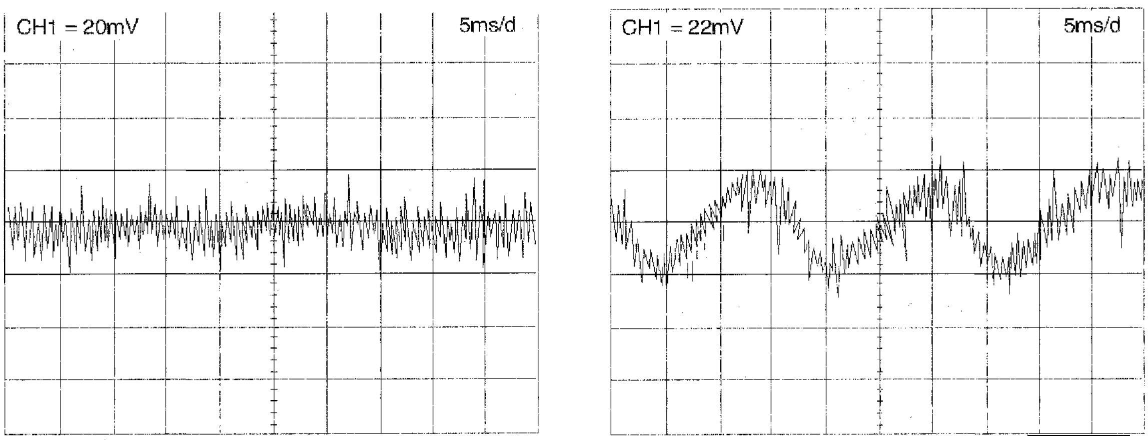
Figure 15. Measurement System



NOTES:
1. Measurement is more accurate at half tone as compared with other gradation level. Change of photoelectric output is sma!! at black level.
2. DC bias voltage must be adjusted slowly. The value of optimum common electrode DC bias changing fast is different from that when changing slowly because DC response is slow.
3. The final adjustment of DC bias voltage must be made by changing from positive to negative.

5703-18

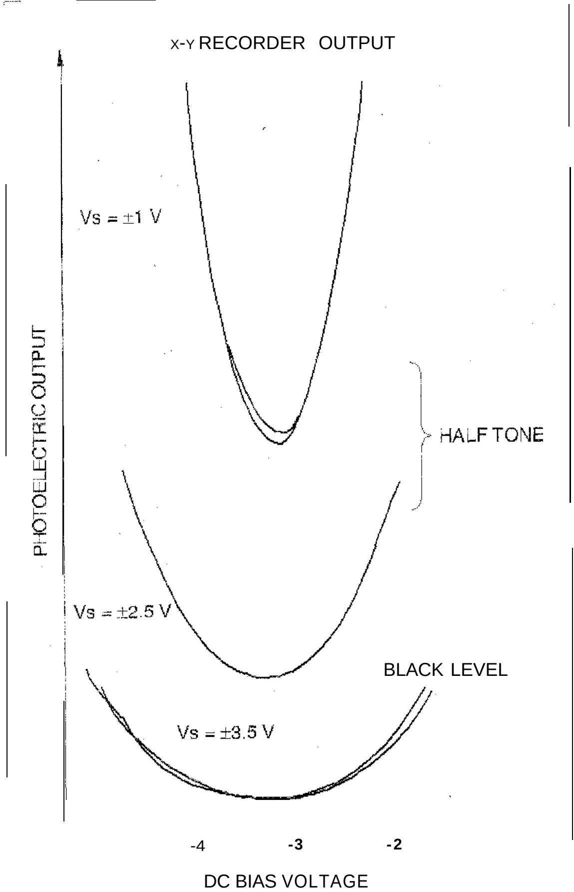
Figure 17. Optimum Common Electrode DC Bias Voltage By Measurement of Contrast



DC bias voltage = Optimum **DC bias voltage = Optimum +1 V**

5703-17

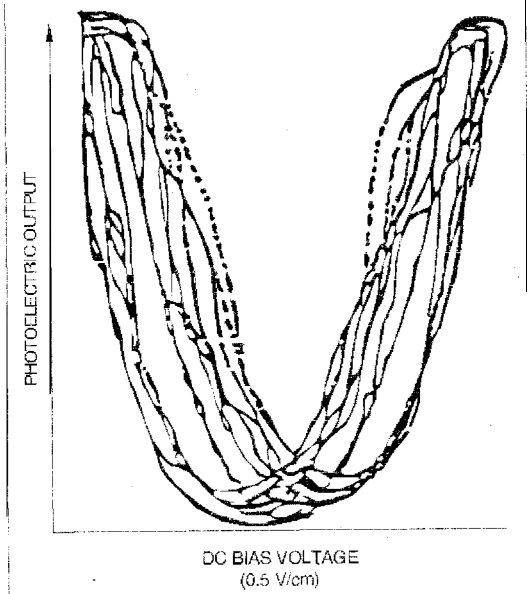
Figure 16. **Waveform of Flicker**



NOTE: **Optimum common electrode DC bias voltage is almost equal between haltone and black level It is difficult to decide the optimum point a: black level.**

5703-1

Figure 18. Relation Between Gradation Level and DC Bias Voltage



NOTE: The value of the minimum point is not definite because DC response is slow and the optimum point can not be attained.

5703-20

Figure 19. Output Voltage With DC Bias Voltage Changing Fast

OUTLINE DIMENSIONS