@ELECTRICAL CHARACTERISTICS

- **Absolute Maximum Ratings**

Item	Symbol	Limit	Unit	Note
Power Supply Voltage (1)	V_{CC}	-0.3 to +7.0	V	
Power Supply Voltage (2)	V1 to V5	V_{CC}-13.5 to V_{CC}+0.3	V	3
Input Voltage	V_T	-0.3 to V_{CC}+0.3	V	
Operating Temperature	Topr	-20 to +75	°C	
Storage Temperature	Tstg	-55 to +125	°C	

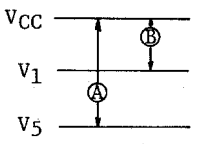
Note 1: If LSI's are used above-absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristic limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Note 2: All voltage values are referenced to GND=OV.

Note 3: Applies to V1 to V5. Must maintain $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

(high ← → low)

● Electrical Characteristics (VCC = 5V±10%, Ta = -20 to +75°C)



Ⓐ = $V_{CC}-V_5$
Ⓑ = $V_{CC}-V_1$
Ⓐ ≧ 1.5V
Ⓑ ≦ 0.25 × A

The conditions of V_1, V_5 voltages are for proper operation of the LSI and not for the LCD output level. The LCD drive voltage condition for the LCD output level is specified in "LCD voltage V_{LCD}".

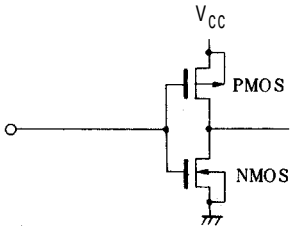
Item	Symbol	Test condition	Limit min	Limit typ	Limit max	Unit	Note
Input "High" Voltage (1)	V_{IH1}		2.2	-	Vcc	V	(2)
Input "Low" Voltage (1)	V_{IL1}		-0.3	-	0.6	V	(2)
output "High" voltage (1) (TTL)	V_{OH1}	$-I_{OH}$=0.205mA	2.4	-	-	V	(3)
Output "Low" Voltage (1) (TTL)	V_{OL1}	I_{OL}=1.2mA		-	0.4	V	(3)
Output "High" Voltage (2)(CMOS)	V_{OH2}	$-I_{OH}$=0.04mA	0.9V_{CC}	-	-	V	(4)
Output "Low" Voltage (2) (CMOS)	V_{OL2}	L_{OL}=0.04mA		-	0.1V_{CC}	V	(4)
Driver Voltage Descending (COM)	VCOM	Id=0.05mA		-	2.9	V	(10)
Driver Voltage Descending (SEG)	VSEG	Id=0.05mA		-	3.8	V	(10)
Input Leakage Current	I_{IL}	V_{in}=0 to V_{CC}	-1	-	1	μA	(5)
Pull UP MOS Current	$-I_p$	V_{CC}=5V	50	125	250	μA	
Power Supply Current (1)	I_{CC1}	Ceramic filter oscillation V_{CC}=5V, f_{osc}=250kHz		0.55	0.8	mA	(6)
Power Supply Current (2)	I_{CC2}	Rf oscillation External clock operation V_{CC}=5V, f_{osc}=fcp=270kHz		0.35	0.6	mA	(6) (11)
External Clock Operation							
External Clock Frequency	f_{cp}		125	250	350	kHz	(7)
External Clock Duty	Duty		45	50	55	%	(7)
External Clock Rise Time	t_{rcp}				0.2	μs	(7)
External Clock Fall Time	t_{fcp}				0.2	μs	(7)
Input "High" Voltage (2)	V_{IH2}		V_{CC}-1.0	-	Vcc	V	(12)
Input "Low" Voltage (2)	V_{IL2}		-0.3	-	1.0	V	(12)
Internal Clock Operation (Rf oscillation)							
Clock Oscillation Frequency	f_{osc}	Rf=91kΩ±2%	190	270	350	kHz	(8)
Internal Clock Operation (Ceramic filter oscillation)							
Clock Oscillation Frequency	f_{osc}	Ceramic filter	245	250	255	kHz	(9)
LCD Voltage	V_{LCD1}	V_{CC}-V_5 1/5 bias	4.6	-	11	V	(13)
	V_{LCD2}	1/4 bias	3.0	-	11	V	(13)

Note 1: The following are I/O terminal configurations except for liquid crystal display output.

. Input Terminal

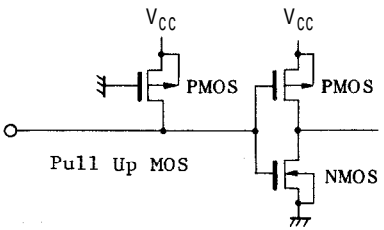
Applicable Terminals: E

(No pull up MOS)



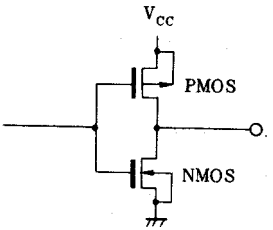
Applicable Terminals: RS, R/W

(With pull up MOS)



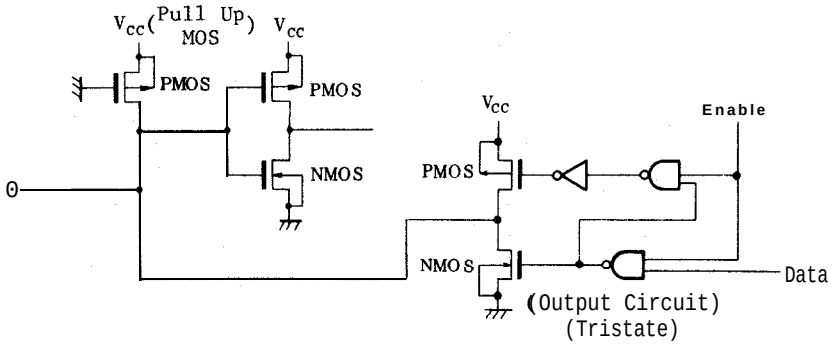
• Output Terminal

Applicable Terminals: CL_1, CL_2, M, D



. I/O Terminal

Applicable Terminals: DBO to DB_7



Note 2: Input terminals and I/O terminals. Excludes OSC_1 terminals.

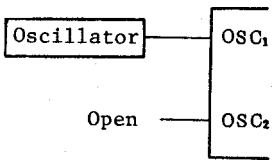
Note 3: I/O terminals.

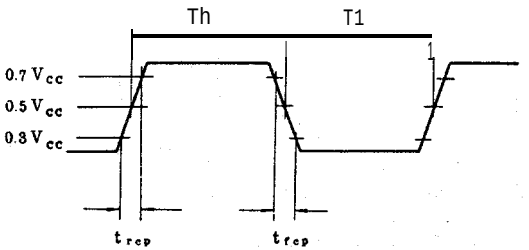
Note 4: Output terminals.

Note 5: Current flowing through pull-up MOS's and output drive MOS's is excluded.

Note 6: Input/Output current is excluded. When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply. To avoid this, input level must be fixed at high or low.

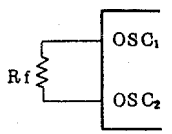
Note 7: External clock operation.





$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

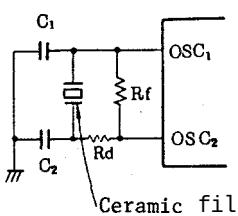
Note 8: Internal oscillator operation using oscillation resistor Rf.



Rf : 91kΩ± 2 %

Since oscillation frequency varies depending on OSC_1 and OSC2 terminal capacity, wiring length for these terminals should be minimized.

Note 9: Internal oscillator operation using a ceramic filter.is used.



Ceramic filter: CSB250A (Murata)

Rf: 1MΩ ±10%

C_1: 680pF±10%

C_2: 680pF±10%

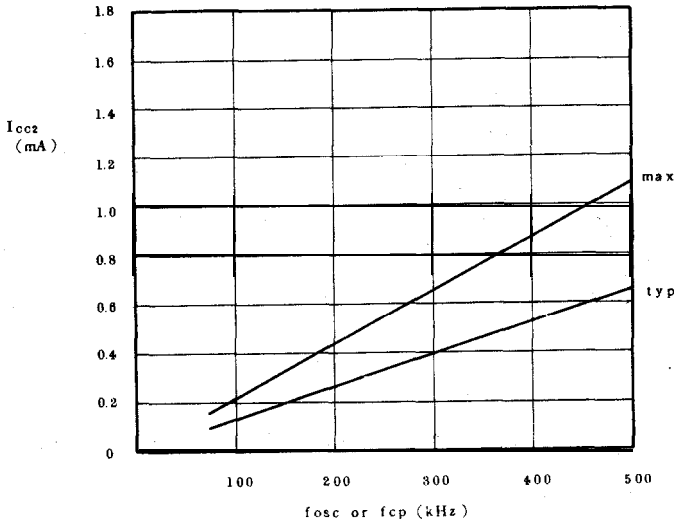
Rd: 3.3kΩ±5%

Note 10: Applies to both V_{COM} and VSEG voltage drops.

V_{COM}: From poer supply terminal VCC, Vl, V_4, V_5 to each common signal terminal (COM_1 to COM_{16})

V_{SEG}: From power supply terminal VCC, V_2, V_3, V_5 to each segment signal terminal (SEG_1 to SEG_{40})

Note 11: Relation between operation frequency and current consumption is shown in this diagram. (V_{CC} = 5V)



Note 12: Applied to OSC_1 terminal.

Note 13: The condition for COM pin voltage drop (V_{COM}) and SEG pin voltage drop (V_{SEG}).

● Timing Characteristics

Write Operation

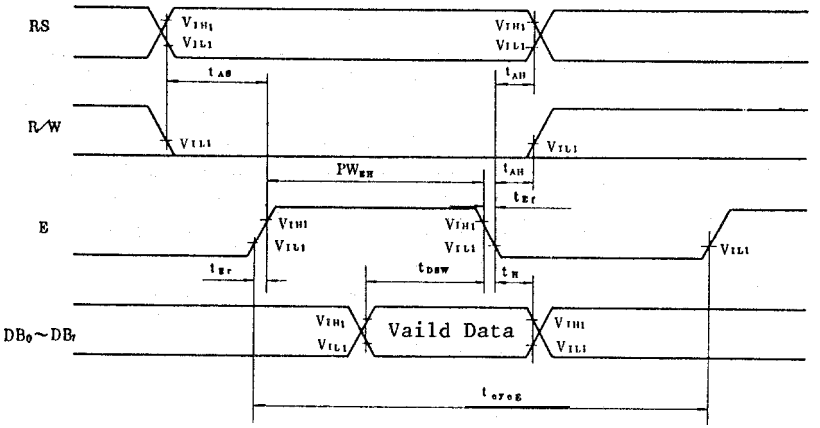


Fig. 1 Bus Write Operation Sequence
(Writing data from MPU to HD44780)

Read Operation

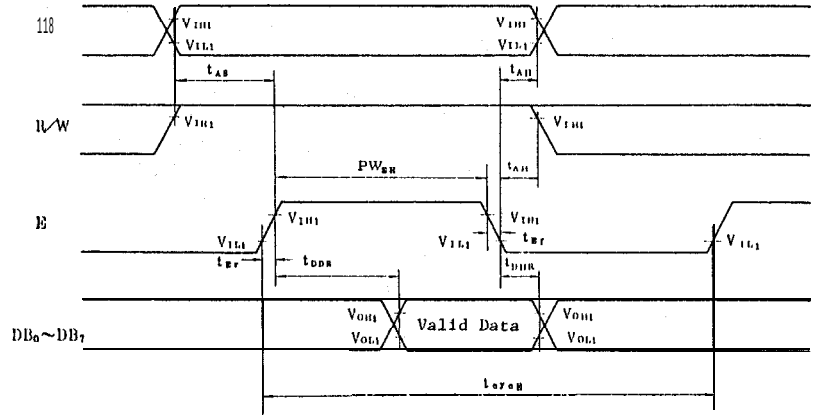


Fig. 2 Bus Read Operation Sequence
(Reading out data from HD44780 to MPU)

Interface Signal with Driver LSI HD44100H

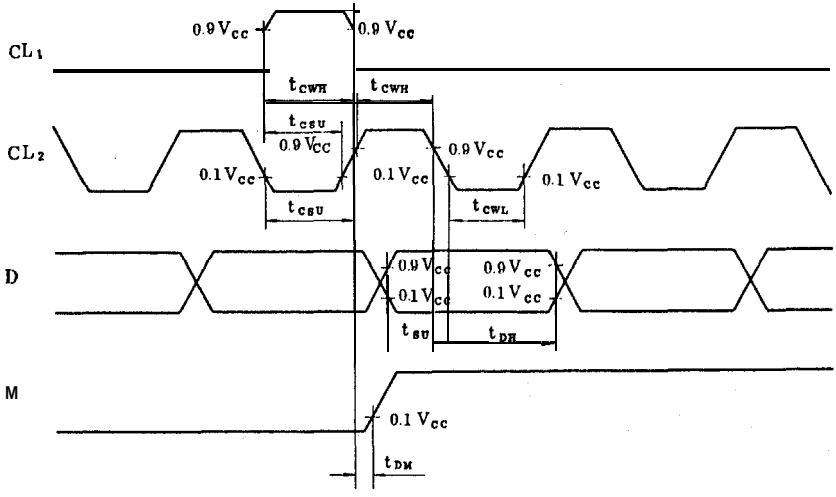


Fig. 3 Sending Data to Driver LSI HD44100H

- **BUS Timing Characteristics** (V_{CC} = 5.0V ± 10%, GND = 0V, Ta = -20 to +75°C)

Write Operation (Writing data from MPU to HD44780)

Item		Symbol	Test condition	Limit min	Limit max	Unit
Enable Cycle Time		$t_{cyc}E$	Fig. 1	1000	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 1	450	-	ns
Enable Rise/Fall Time		t_{Er}, t_{Ef}	Fig. 1	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 1	140	-	ns
Address Hold Time		t_{AH}	Fig. 1	10	-	ns
Data Set-up Time		t_{DSW}	Fig. 1	195	-	ns
Data Hold Time		t_H	Fig. 1	10	-	ns

Read Operation (Reading data from HD44780 to MPU)

Item		Symbol	Test condition	Limit min	Limit max	Unit
Enable Cycle Time		$t_{cyc}E$	Fig. 2	1000	-	ns
Enable Pulse Width	"High" level	PW_{EH}	Fig. 2	450	-	ns
Enable Rise/Fall Time		t_{Er}, T_{Ef}	Fig. 2	-	25	ns
Address Set-up Time	RS, R/W —E	t_{AS}	Fig. 2	140	-	ns
Address Hold Time		t_{AH}	Fig. 2	10	-	ns
Data Delay Time		t_{DDR}	Fig. 2	-	320	ns
Data Hold Time		t_{DHR}	Fig. 2	20	-	ns

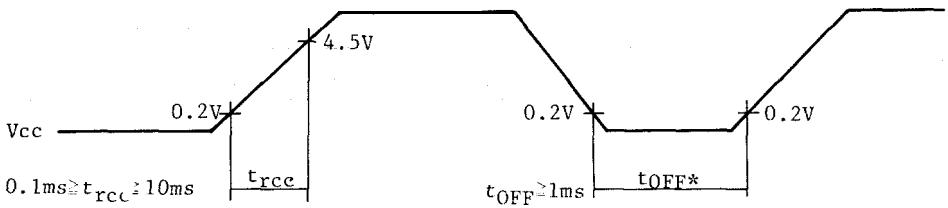
- **Interface Signal with HD44100H Timing Characteristics**
  (V_{CC} = 5.0V ± 10%, GND = 0V, Ta = -20 to +75°C)

Item		Symbol	Test condition	Limit min	Limit max	Unit
Clock Pulse Width	"High" level	t_{CWH}	Fig. 3	800	–	ns
Clock Pulse Width	"High" level	t_{CWL}	Fig. 3	800	–	ns
Clock Set-up Time		t_{CSU}	Fig. 3	500	–	ns
Data Set-up Time		t_{SU}	Fig. 3	300	–	ns
Data Hold Time		t_{DH}	Fig. 3	300	–	ns
M Delay Time		t_{DM}	Fig. 3	-1000	1000	ns

- **Power Supply Conditions Using Internal Reset Circuit**

Item	Symbol	Test condition	Limit min	Limit max	Unit
Power Supply Rise Time	trcc		0.1	10	ns
Power Supply OFF Time	t_{OFF}		1	–	ns

Since the internal reset circuit will not operate normally unless the preceding conditions are met, initialize by instruction.
(Refer to "Initializing by Instruction")



(Note) t_{OFF} stipulates the time of power OFF for power supply instantaneous dip or when power supply repeats ON and OFF.