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SECTION 2 HARDWARE OVERVIEW

moved to Sect 1
H The Serial I/O Board communicates with the SCOUT processor via the SCOUT-BUS. Interface is accomplished by means of a 70 pin Card edge Connector. ~~The board is designed to have two or four channels, each of which operates independently.~~

H Linkage of the RS422 board to I/O device is accomplished by means of a 60 pin mass terminated flat ribbon cable connector. An optional three foot long interface cable and paddleboard are available with the RS422 board. The paddleboard contains four 37 pin Sub miniature D-shell Connectors. Connector wiring and pin assignments are consistent with RS449 Connector specifications.

H Linkage of the RS232 board to I/O device is accomplished by means of two or four ten pin connectors. An appropriately configured 25-pin D-shell Connector links the interface ~~device~~ cable to peripheral devices. → The relationship of the Serial I/O Board to its environment is shown

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in Figure — for RS422, and in Figure —
for RS232.

The Board consists of several basic functional units: Band Rate Generator, 2 or 4 UARTs, Drivers and Receivers, DC to DC Converters (RS232 only), Station ID, and Wrap Around Circuits.

2.1 BAND RATE GENERATOR

The band rate generator consists of a series of synchronous counters driven by the SCOUT ^{system clock} bus ~~bus~~ CLK, a 15.2064 MHz square wave. The generator divides the 15.2064 MHz clock into frequencies ranging from ^{1760 (110 Baud) hertz} ~~110 hertz~~ to ^{153,600 (9600 Baud) hertz} ~~9600 hertz~~. Band rates for each channel are selectable via an eight position DIP switch SW1-SW4.

NOTE

Not more than 1 position of each switch may be set to the "ON" position at any given time.

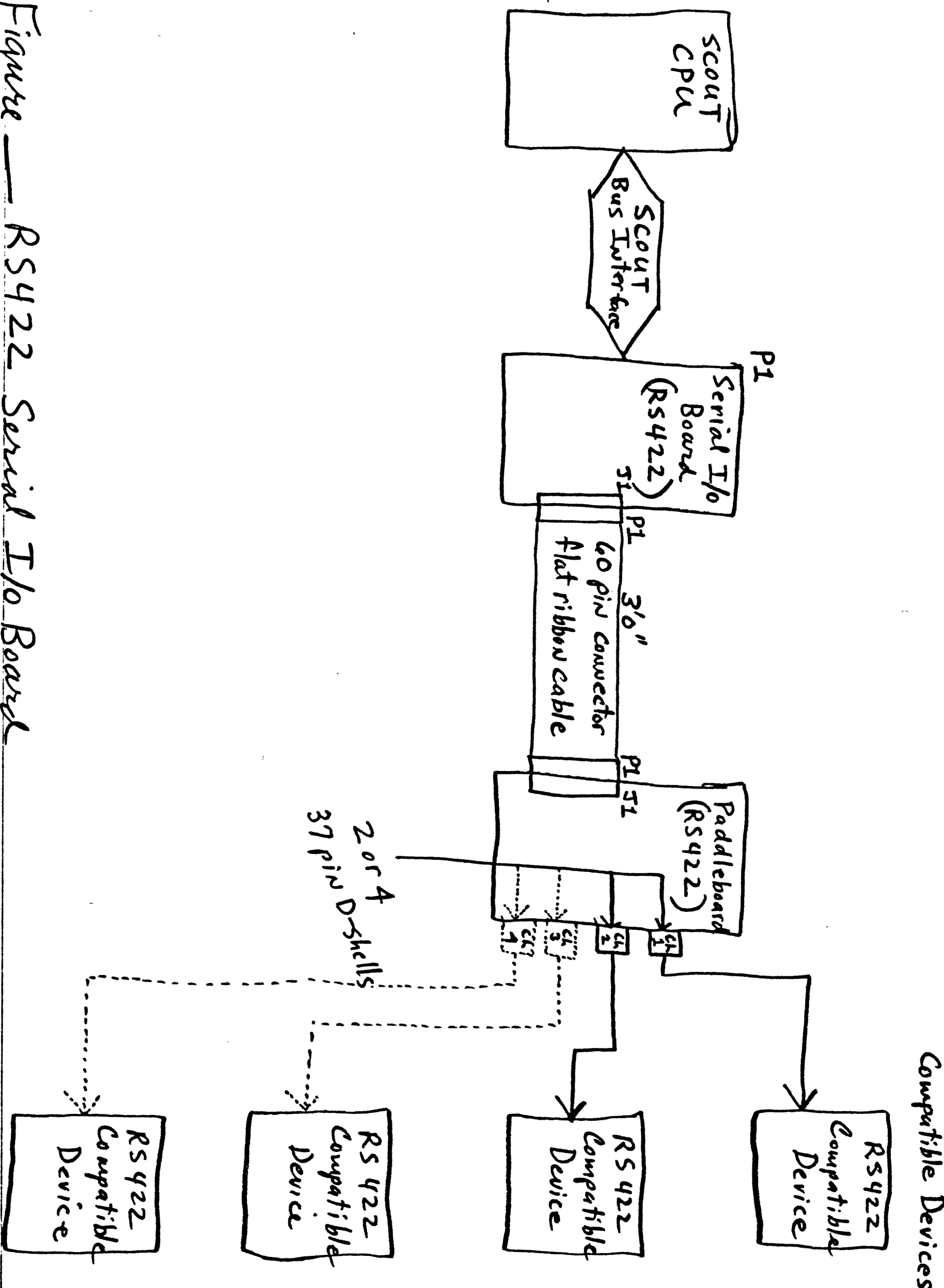


Figure — RS422 Serial I/O Board

Block Diagram

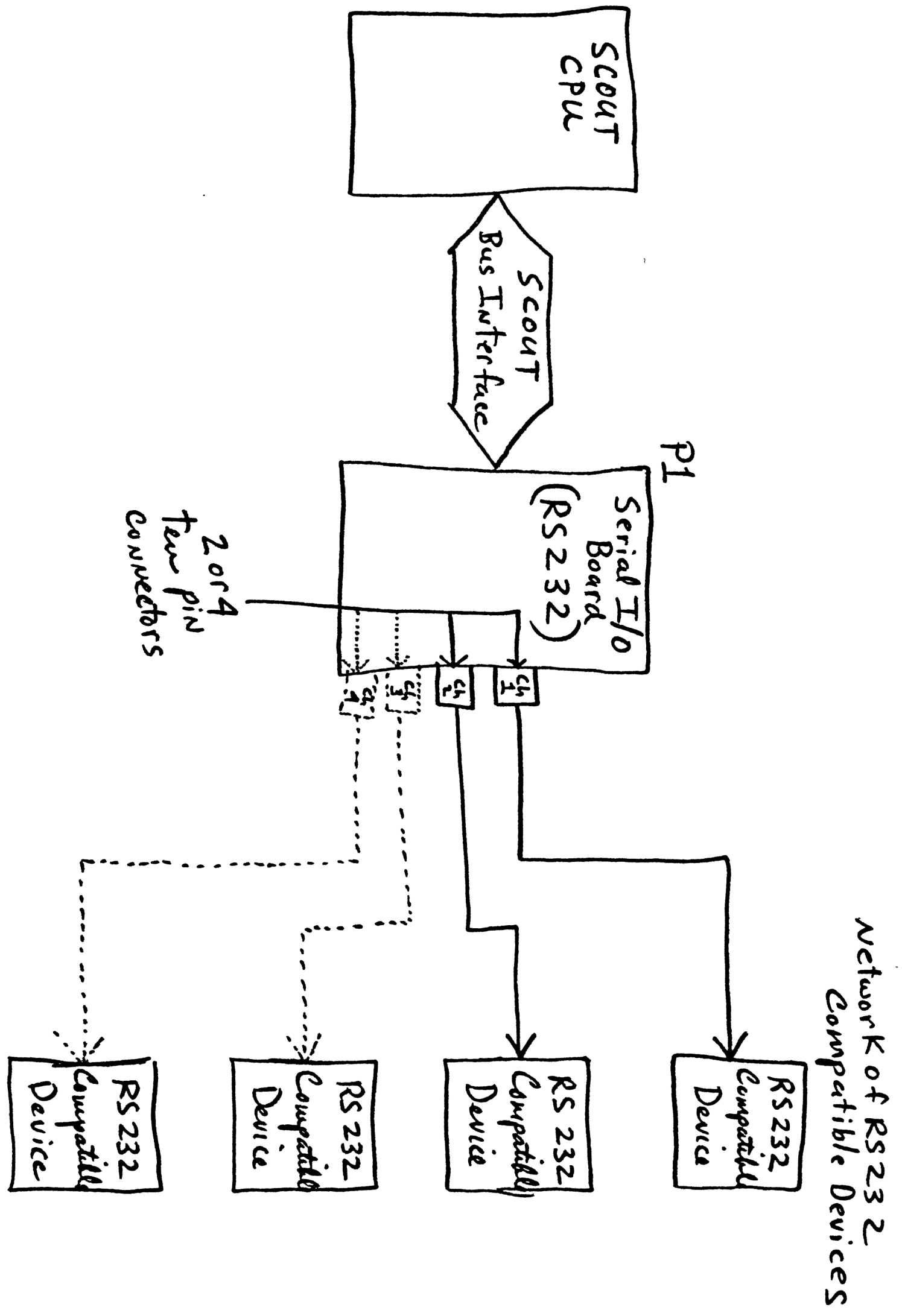


Figure — RS-232 Serial I/O Board Block Diagram

2.2 UARTs

The Universal Asynchronous Receiver Transmitter (UART) is programmed by system software for maximum flexibility, allowing the system to receive or transmit almost any serial data communication signal. The UART performs serial to parallel conversion on data characters received from an input/output device or MODEM, and parallel to serial conversion on data characters received from the CPU. The Serial I/O Board is designed to accommodate either 2 or 4 UARTs. For a description of UART initialization procedures, the reader is referred to Section 4 (Programming).

2.3 DRIVERS and RECEIVERS

RS422 drivers transmit digital data over balanced lines. They are designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines. The RS422 receivers ~~are quad line~~ and meet requirements for balanced and unbalanced digital data transmission.

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① RS232 drivers ~~and receivers~~ convert the UART's ^{digital} output ^{signals} to RS232 compatible signal levels. The RS232 ^{receivers} ~~drivers~~ convert the ^{RS232 input signals to TTL compatible levels on the board} ~~serial data streams from TTL levels~~ to approximately ± 12 volts. The RS232 receiver converts serial data streams from ~~approximately ± 12 volts~~ to TTL levels.

2.4 DC TO DC CONVERTER

① The RS232 Board provides a DC to DC converter which translates +5 volts input from the main supply to the ~~5~~ voltage level required by the RS232 drivers and receivers. The DC to DC converter ~~is~~ ^{is} not used on the RS422 ~~to~~ Board.

2.5 STATION ID

① A Station ID Switch (SW6) provides Multi-Drop Communication Systems capability. The Station ID can be read under software command, and can then be used as an addressing mechanism in a multi-drop communication network. The result is that each computer in the system can be assigned a unique address. The 8-position DIP switch allows a maximum of 256 unique Station I.D's.

2.6 WRAP AROUND CIRCUITRY

H The SCOUT Serial I/O Board includes wrap around circuitry which enables the ISOLITE self test diagnostic feature to test a large part of the board by communicating between Channel's 1 and 2, and between Channel's 3 and 4 (in four channel version only). The ISOLITE diagnostic is then able to transmit and receive data between the two channel pairs. The data ~~path~~ path between the two channel pairs does not normally include the drivers and receivers. However, an external wrap around Test Cable can be connected between Channel's 1 and 2 and between Channel's 3 and 4 (in four channel version only), to allow the drivers and receivers to be included in the data path. A more detailed explanation of this feature is ~~provided~~ given in Section ____.

SECTION 3 HARDWARE INSTALLATION

This section describes installation considerations unique to the Serial I/O Board. For a description of general installation procedures pertaining to I/O controllers, the reader is referred to the SCOUT NAKED MINI 404 Reference Handbook. Figures — and — show Board layout which includes switch block locations.

3.1 DEVICE ADDRESS SELECTION

Communication between the CPU and the Serial I/O Board is accomplished by means of a four bit device address. The four bits are selectable with Switch SW7. SW7-1 selects the most significant bit (AB⁴) and SW7-4 selects the least significant bit. SW7-5 is undefined, but its state will be displayed in data bit 11 during execution of a RAL instruction cycle together with the device address and data read from the ISOLITE ROM. DA switch position 1 corresponds to bit position 7 on the Address Bus; DA switch position 4 corresponds to bit position 4.

there is a note in the instruction manual that says "see page 11" (top)

SWS
BOARD I.D. NUMBER
SELECT SWITCH

TERMINATION BLOCKS

ISOLITE HEADER

ISOLITE
ROM —

SW7
DEVICE ADDRESS
SELECT
SWITCH

SW6
STATION
IDENTIFICATION
SELECT SWITCH

SW4
BAUD RATE
SELECT
CHANNEL 4
(in four channel
version only)

SW3
BAUD RATE
SELECT
CHANNEL 3
(in four channel
version only)

SWZ
BAUD RATE
SELECT
CHANNEL Z

SW1
BAUD RATE
SELECT
CHANNEL 1

LUARTs

ISOLATED
LED
IND

51
04
C01

AUT
ANS
HEA

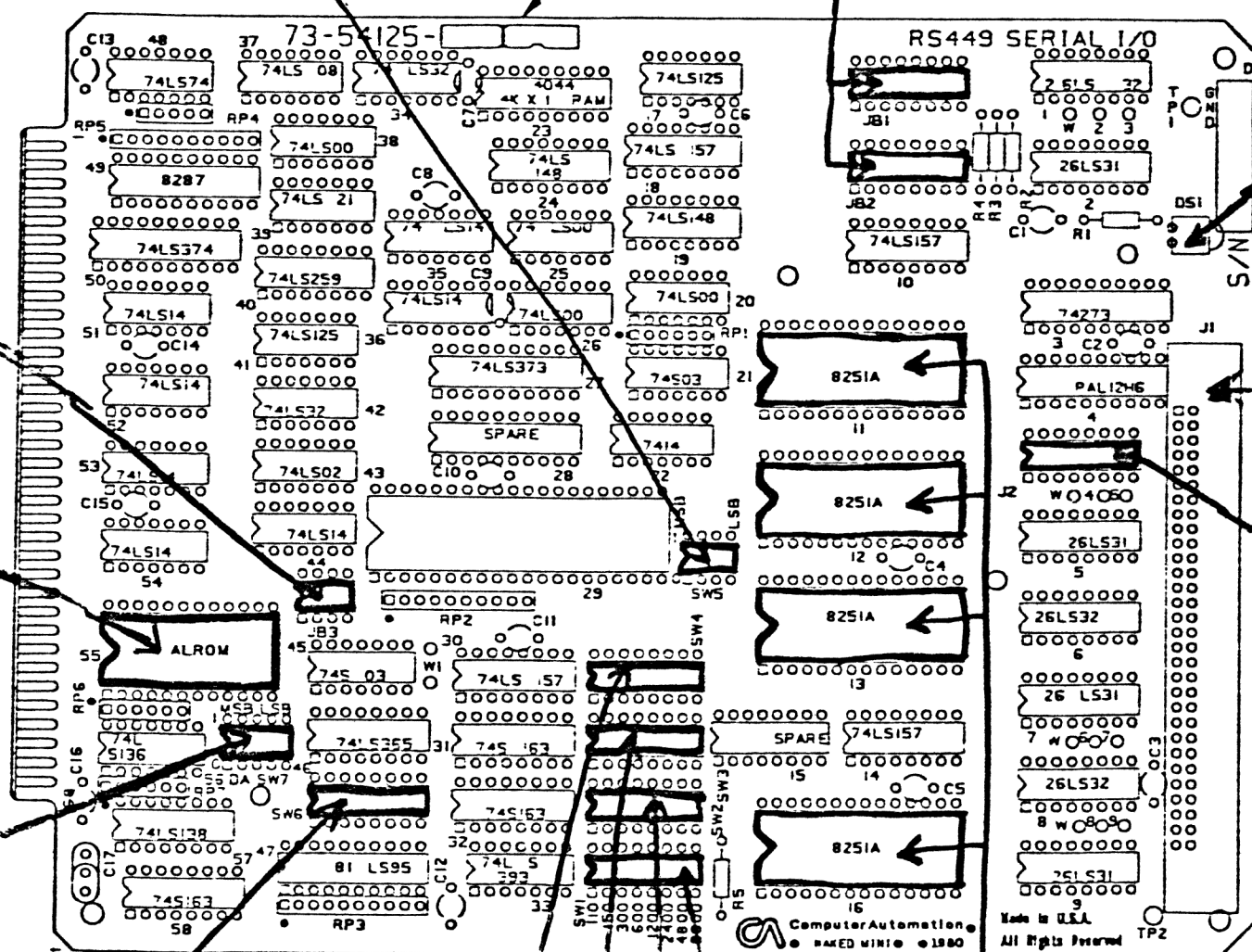


Figure ____ RS422 Switch Block Locations

Figure — RS232 Switch Block Locations

The device address is used during a data read, status read, data write, mode write, and control write. The switch is represented in Figure —.

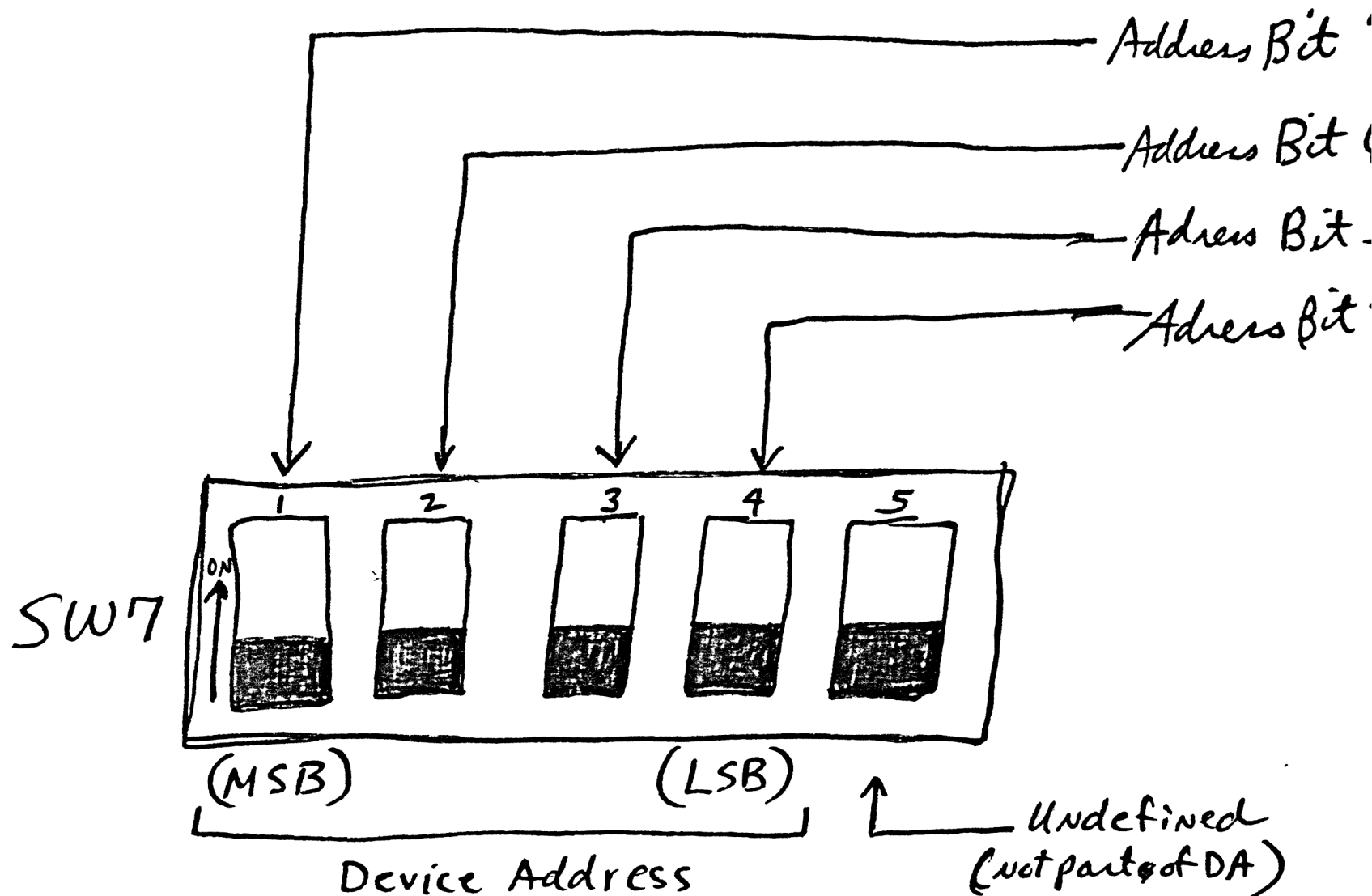


Figure — Configuration for Switch Block 7

3.2 STATION ID

The Station ID is an eight position DIP SWITCH (SW6), and can be read by the CPU at any time during the execution of a status read from any channel. The address is placed on the most significant byte of the system Data Bu.

(DB 08 - DB 15) simultaneously with the status data read from the selected Channel. Status information from the UARTs is placed on the least significant byte of the Data Bus (DB 00 - DB 07). The Status ID switch is represented in Figure — .

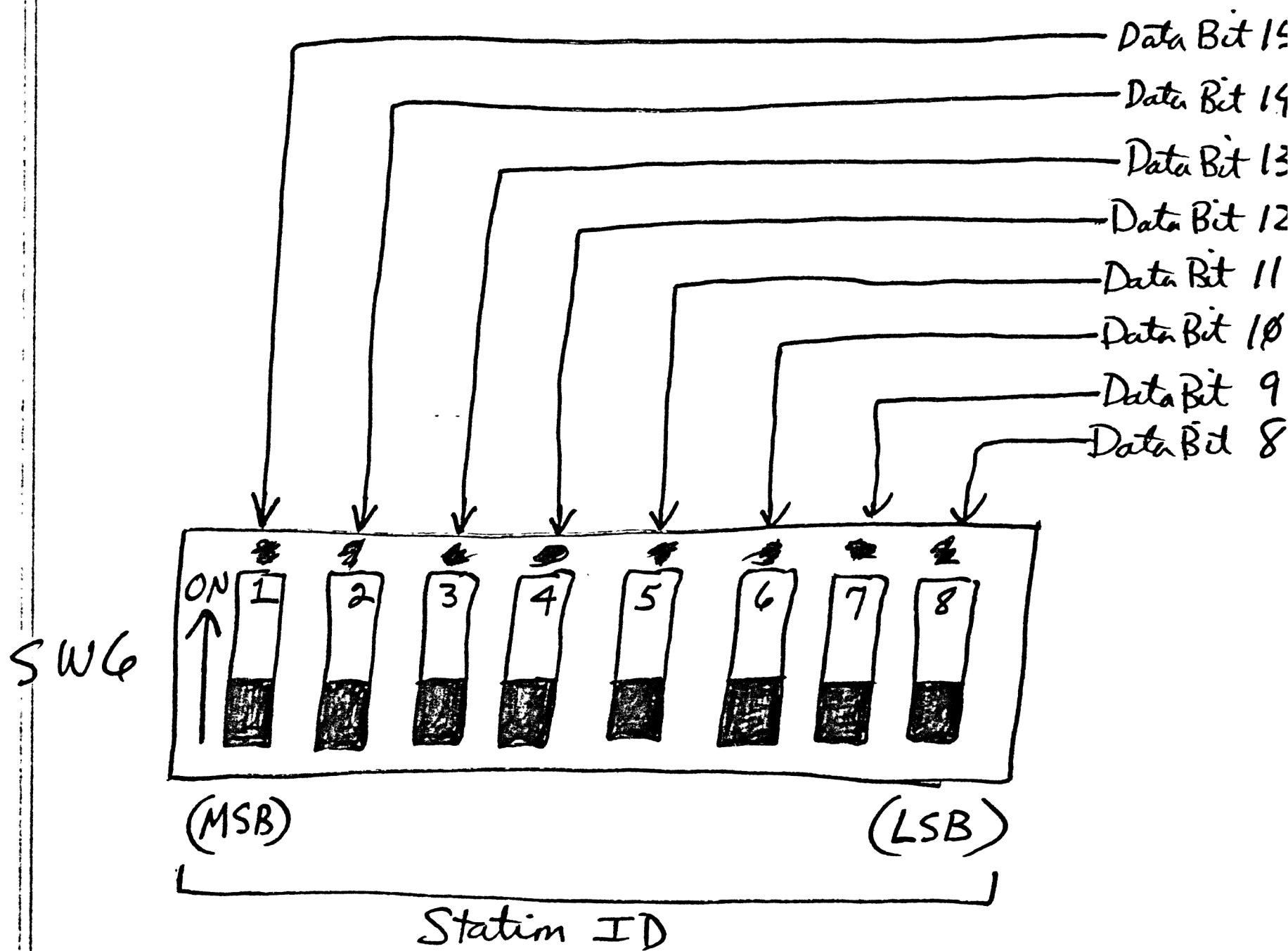


Figure — Configuration for Switch Block 6

3.3 BOARD ID (BDID)

If The onboard ISOLITE ROM is addressed via board ID. A four bit DIP switch allows one of 16 addresses to be used during the execution of a RAL instruction. The switch determines the order in which individual board ISOLITE ROM are read.

If Board ID is selectable with SW5. SW5-1 selects the most significant bit, and SW5-4 selects the least significant bit. BDID switch position 1 corresponds to bit position 3 on the Address Bus; BDID switch position 4 corresponds to bit position $\emptyset$ on the Address Bus. The "ON" switch position represents a logical "1". The Board ID switch is represented in Figure —.

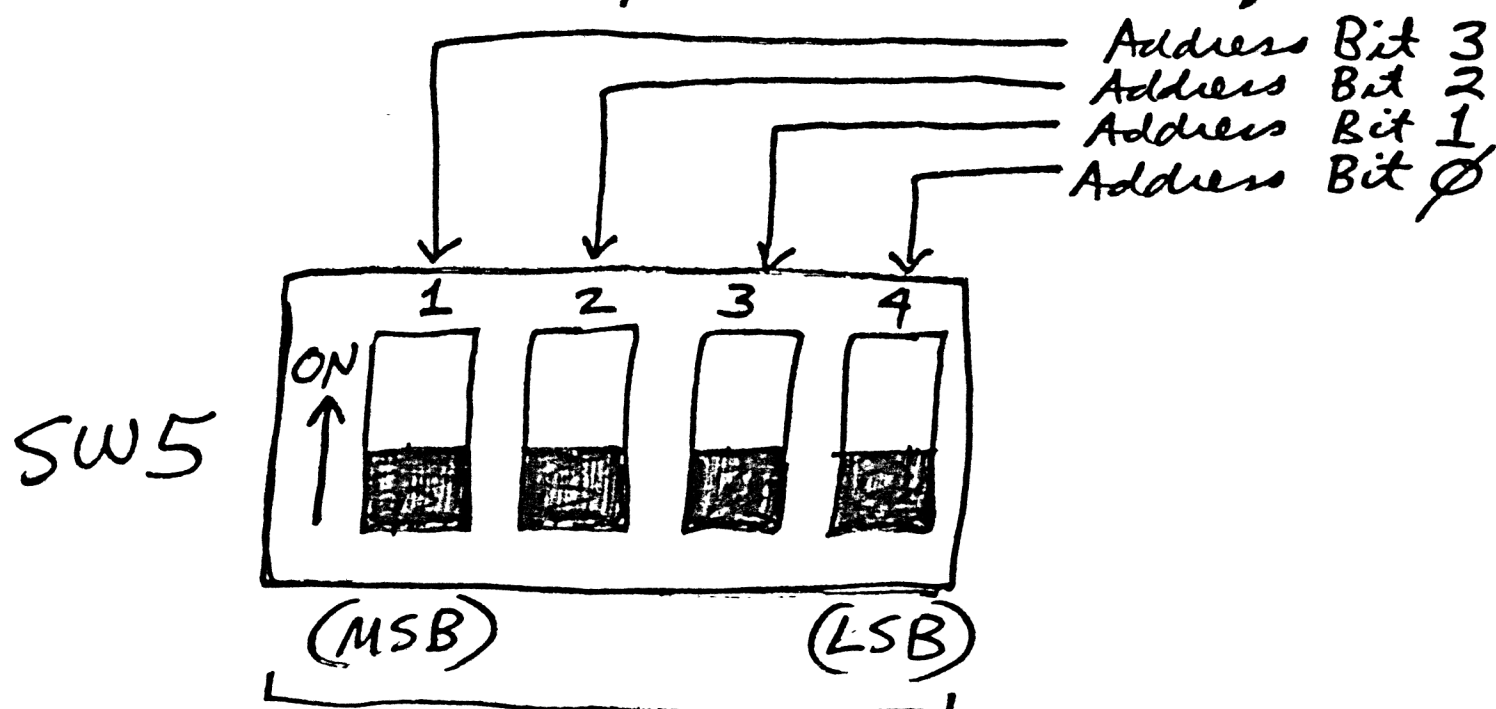
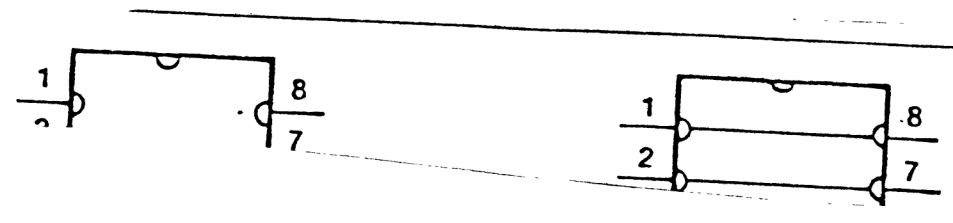


Figure — Configuration for Switch Block 5

3.4 ISOLITE HEADER

If The Serial I/O Board is equipped with an ISOLITE ~~feature~~ header, factory configured for the ROM supplied. If a different model ROM is selected, the ~~jumper~~^{header} block must be rewired. The configuration of the header ~~is~~ for different ~~types of ROM~~ type ROMs is shown in Figure _____. The ICs listed are typical. Use AWG 24 to 28 solid wire for the jumpers and solder all connections. The LED on all boards is mounted on the edge of the card face the user when the unit is installed in the chassis. The LED lights when the ROM is accessed, and stays lit if the test program is not successfully completed, to indicate board failure.



3.5 TERMINATION ~~RESISTORS~~ RESISTORS

The RS422 Board contains two Termination blocks (JB1 and JB2) which provide the capability for optional termination resistors. The termination blocks are layed out to accommodate two basic types of termination configurations, displayed in Figure —. Termination blocks are not used on the RS232 Board.

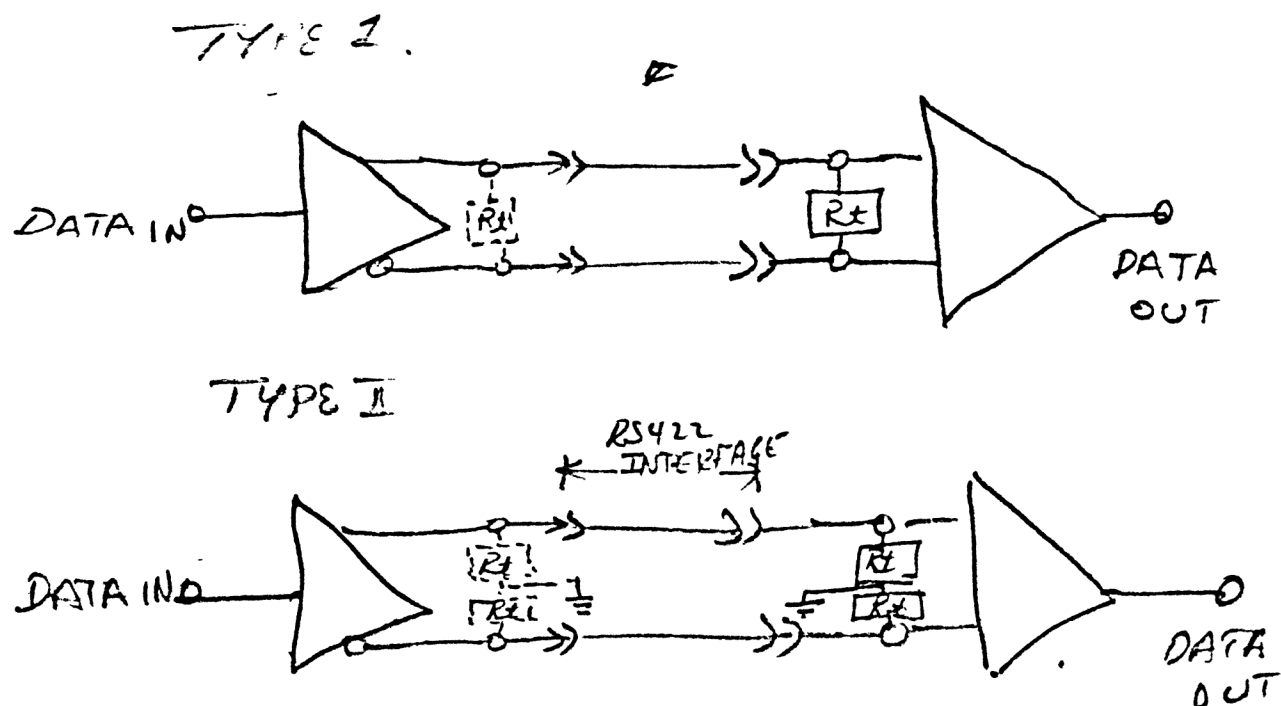


Figure — RS422 Termination Configurations

3.6 WIRE JUMPERS

The RS422 drivers are permanently enabled when the board is shipped from the factory. However, by removing ~~permanently enabled or disabled~~ jumpers W2, W4, W6, and W8, and installing a wire jumper ~~means of~~ wire jumpers (W2, W4, W6, W8). Enabling or disabling occurs in W3, W5, W7, and W9. The drivers can be ~~disabled~~ ~~disabled under software control~~ ~~disabled under software control~~ by controlling the state of the "RTS" bit in the UART's control word.

The Request to Send signal (RTS) is used to manipulate a channel's associated driver or receiver by removing the corresponding jumper and inserting an alternate jumper. The correspondence between channel number and jumper number is shown in Figure —. Wire jumpers ~~do not fit on~~ ~~are not relevant~~ to the RS232 Board.

<u>Channel</u>	<u>Factory Installed Jumper</u>	<u>Optimal (RTS) Jumper</u>
Ch 1	W2	W3
Ch 2	W4	W5
Ch 3	W6	W7
Ch 4	W8	W9

Figure — Channel/Jumper Correspondence

3.7 CONNECTOR PIN LIST

- If The Serial I/O Board plugs directly into the SCOUT Chassis. The SCOUT-BUS edge connector, P1, follows standard SCOUT-BUS pinout, loading, and timing specifications. (See SCOUT-BUS specifications).
- If For the RS422 Board, pin assignments pertinent to the 60 pin external device connector (J1) are given in Table —. Pin assignments for the 37 pin D-connector are given in Table —.
- If For the RS232 Board, pin assignments for the ten pin external device connector (J1) are given in Table —.

go to next page



Table — RS422 S1 Output Connector 18

PIN NUMBER	SIGNAL NAME	DIRECTION	PIN NUMBER	SIGNAL NAME	DIRECT
1	$\overline{\text{OTXD}}\phi$	OUT	31	TEST	IN
2	$\text{OTXD}\phi$	OUT	32	NC	
3	$\text{ODTR}\phi$	OUT	33	$\overline{\text{OTXD}}2$	OUT
4	$\overline{\text{ODTR}}\phi$	OUT	34	$\text{OTXD}2$	OUT
5	$\text{ORTS}\phi$	OUT	35	$\text{ODTR}2$	OUT
6	$\overline{\text{ORTS}}\phi$	OUT	36	$\overline{\text{ODTR}}2$	OUT
7	$\overline{\text{IRXD}}\phi$	IN	37	$\text{ORTS}2$	OUT
8	$\text{IRXD}\phi$	IN	38	$\overline{\text{ORTS}}2$	OUT
9	$\text{IDSR}\phi$	IN	39	$\overline{\text{IRXD}}2$	IN
10	$\overline{\text{IDSR}}\phi$	IN	40	$\text{IRXD}2$	IN
11	$\text{ICTS}\phi$	IN	41	$\text{IDSR}2$	IN
12	$\overline{\text{ICTS}}\phi$	IN	42	$\overline{\text{IDSR}}2$	IN
13	CEINT1	IN	43	$\text{ICTS}2$	IN
14	GND	IN	44	$\overline{\text{ICTS}}2$	IN
15	+5V	IN	45	CEINT3	IN
16	+5V	IN	46	GND	IN
17	$\overline{\text{OTXD}}1$	OUT	47	CEINT4	IN
18	$\text{OTXD}1$	OUT	48	GND	IN
19	$\text{ODTR}1$	OUT	49	$\overline{\text{OTXD}}3$	OUT
20	$\overline{\text{ODTR}}1$	OUT	50	$\text{OTXD}3$	OUT
21	$\text{ORTS}1$	OUT	51	$\text{ODTR}3$	OUT
22	$\overline{\text{ORTS}}1$	OUT	52	$\overline{\text{ODTR}}3$	OUT
23	$\overline{\text{IRXD}}1$	IN	53	$\text{ORTS}3$	OUT
24	$\text{IRXD}1$	IN	54	$\overline{\text{ORTS}}3$	OUT
25	$\text{IDSR}1$	IN	55	$\overline{\text{IRXD}}3$	IN
26	$\overline{\text{IDSR}}1$	IN	56	$\text{IRXD}3$	IN
27	$\text{ICTS}1$	IN	57	$\text{IDSR}3$	IN
28	$\overline{\text{ICTS}}1$	IN	58	$\overline{\text{IDSR}}3$	IN
29	CEINT2	IN	59	$\text{ICTS}3$	IN
30	GND	IN	60	$\overline{\text{ICTS}}3$	IN

Table — RS422 J1 Output
Connector
(Cont'd.)

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Note: Recommended Mating I/O
Connector (J1) part numbers:

AMP P/N 88476-9
BERG P/N 65948-360
WINCHESTER P/N 51-1160-01

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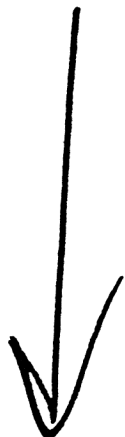


Table — RS422 37 Pin
D-Shell Connector

PIN NUMBER	SERIAL I/O SIGNAL NAME	RS449 SIGNAL NAME	PIN NUMBER	SERIAL I/O SIGNAL NAME	RS449 SIGNAL NAME
1	GND	SHIELD	26		RT
2		SI	27	$\overline{ICTS\emptyset}$	CS
3		SPARE	28		IS
4	OTXD $\emptyset$	SD ^{or} _{SO?}	29	$\overline{IDSR\emptyset}$	DM
5		ST	30	$\overline{ODTR\emptyset}$	TR
6	IRXD $\emptyset$	RD	31		RR
7	ORTS $\emptyset$	RS	32		SS
8		RT	33		SQ
9	ICTS $\emptyset$	CS	34		NS
10		LL	35		TT
11	IDSR $\emptyset$	DM	36		SB
12	ODTR $\emptyset$	TR	37		SC
13		RR			
14	+5VDC	RL			
15	CEINT1	IC			
16		SF/SR			
17		TT			
18		TM			
19	GND	SG			
20		RC			
21	+5V	SPARE			
22	$\overline{OTXD\emptyset}$	SD			
23		ST			
24	$\overline{IRXD\emptyset}$	RD			
25	$\overline{ORTS\emptyset}$	RS			

Note: Recommended mating (plug)
37 pin subminiature
D-shell connector Par
Numbers are AMP
P/N 205210-1;
TRW/CINCH P/N
DCMA - 37p
(cont'd - next page)

Note: For mounting the 37
pin connector board ^{again}
as a panel, the recommended male-
female standoff is
Amp Part Number 205818-
or equivalent.

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Table — RS232 Ten Pin J1-J4 Serial I/O Connectors

PIN NUMBER	SIGNAL NAME
1	Test
2	Data Terminal Ready
3	Transmit Data
4	Receive Data
5	Clear to Send
6	Data Set Ready
7	Ground
8	Ring Indicator
9	Reserved
10	Request to Send

Note: Recommended mating J1-J4
connector part number is
Berg double row conn. housing
P/N 65043-032, loose pin
crimp, 40u gold over
nickel P/N 47745.

SECTION 4 : PROGRAMMING

If The Serial I/O Board conforms to I/O programming procedures described in SCOUT reference literature. Operations can be performed in polled mode, interrupt mode, or auto I/O mode. The reader is referred to Section 5 for a description of data operations in each of these modes.

If Section 4 contains general I/O information pertinent to the Serial I/O Board, and describes software procedures in relation to board control functions, channel control functions, and data operations.

4.1 INPUT/OUTPUT INSTRUCTIONS

If These instructions are used to transfer information to and from peripheral devices. The Serial I/O Board uses two types of I/O instructions: programmed I/O and auto I/O.

If Programmed I/O instructions supported by the Board are:

SECTION 4 PROGRAMMING

(Outline)

4.1 INPUT/OUTPUT INSTRUCTIONS

4.2 BOARD CONTROL FUNCTIONS

4.2.1 Write Board Control Word

Interrupt

Auto Answer

Test

Reset

Auto Echo

4.2.2 Write Interrupt Vector Base Address

4.3 CHANNEL CONTROL FUNCTIONS

4.3.1 IN Instruction

4.3.2 OUT Instruction

4.3.3 SELP Instruction

4.4 DATA OPERATIONS

(IN, OUT, AIB, AOB)

SELP	4 Reg, DaFc
IN	DaFc, 4 Reg
OUT	4 Reg, DaFc
SST	DaFc

H Automatic I/O instructions supported by the Board are:

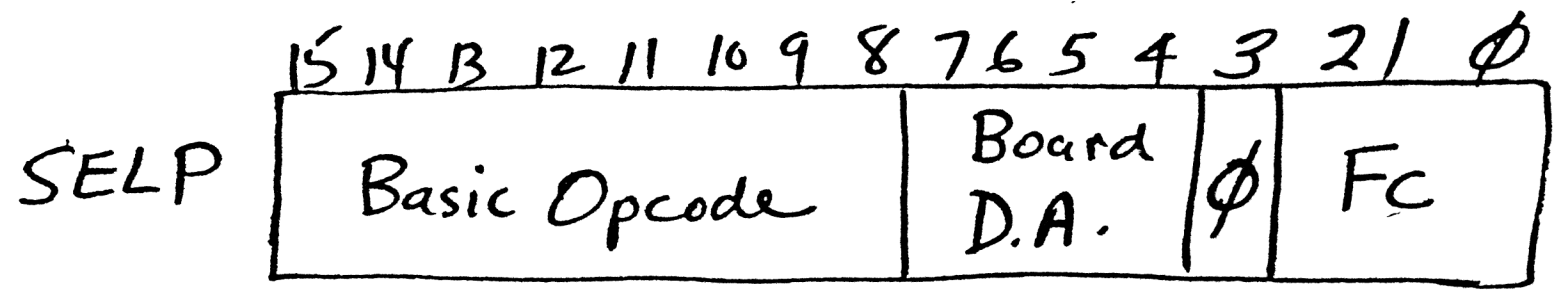
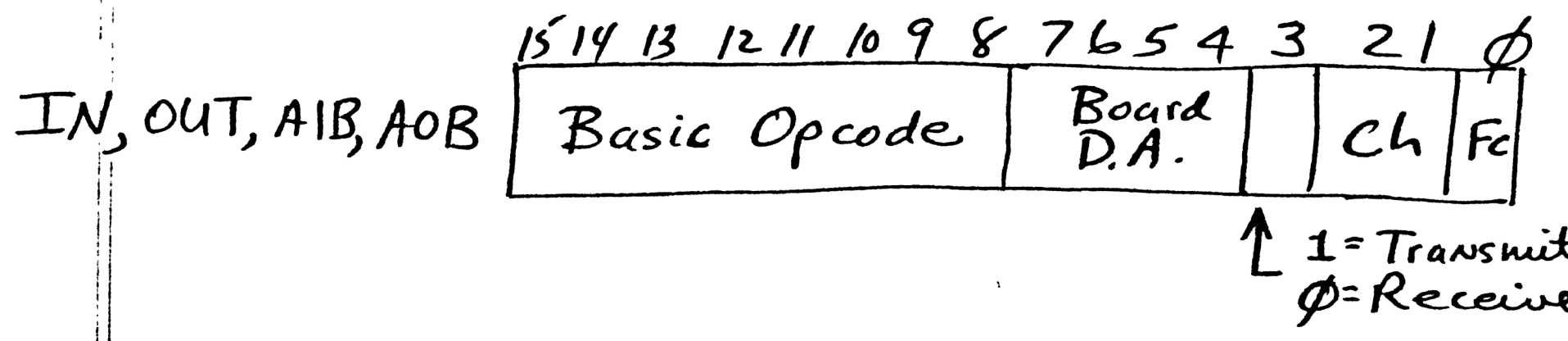
AIB	DaFc	(Automatic Input Byte)
AOB	DaFc	(Automatic Output Byte)

The reader is referred to the NAKED MINI Family Assembler Reference Manual for descriptions of these instructions.

H Addressing the I/O Controller is accomplished by means of the DaFc operand, defined as the lower 8 bits of the opcode word for each instruction. General formats for I/O instructions relative to the Serial I/O Board are shown in Figure -

go to next page





Binary Format for SELP Function Code

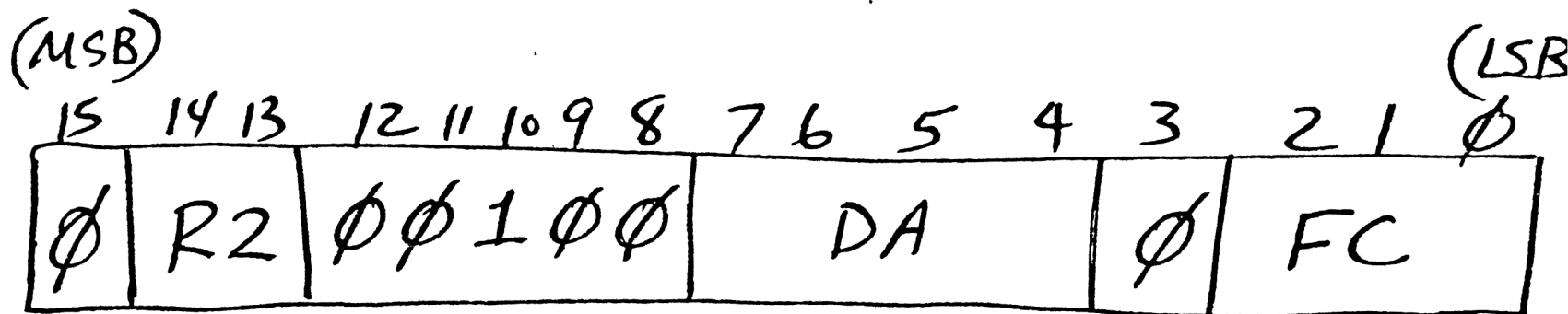
	Function
0 0 0	Write Special Character to Ch 0
0 0 1	Write Interrupt Vector Base Address
0 1 0	Write Special Character to Ch 1
0 1 1	Write Board Control Word
1 0 0	Write Special Character to Ch 2
1 0 1	Undefined
1 1 0	Write Special Character to Ch 3
1 1 1	Undefined

Figure — INPUT/OUTPUT instruction formats

4.2 BOARD CONTROL FUNCTIONS

¶ The board control functions are software controllable operations that affect all I/O channels on the board Simultaneously. All board control functions ^{are programmed using} ~~are incorporated~~ SELP instructions, and are differentiated from channel control functions that use the SELP instruction by bit ϕ (the LSB) of the function code. A function code with bit $\phi = 1$ indicates board control functions; a function code with bit $\phi = 0$ indicates channel control functions.

¶ Board control functions are implemented by means of the board control word and the interrupt vector base address. Both words ^{are set using} ~~contain~~ a SELP output instruction ^{which} ~~designed to~~ transfers the 16-bit content of the specified register to the addressed I/O Controller. Bits ϕ , 1, and 2 of the SELP instruction are combined to define the desired function, as shown in Figure —.



R2: 00, A Register
 01, X Register
 10, Q Register
 11, Y Register

FC: 001 Wide Interrupt Vector Base Address
 011 Write Board Control Word (Function Decode Register)

2 & change name
 3 suppose to represent
 4.2.1 + 4.2.2
 KT

Figure — Binary Format for Board Control Word

4.2.1 Write Board Control Word (Function Decode Register)

This word generally controls the hardware interface between the Serial I/O Board and peripheral devices. Whenever any bit within the board control word is changed, the entire word must be re-written. The ~~lower byte~~ format of the specified register content is shown in Figure —.

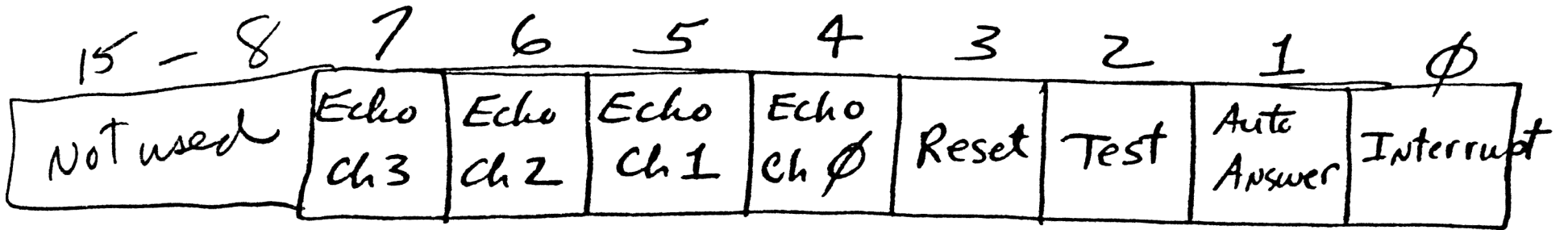


Figure — Format for Board Control Word
Board Interrupt (Bit 0)

Interrupt for all channels is controlled by the Board Interrupt bit.

0 Board Interrupt Disable
 1 Board Interrupt Enable

Auto Answer (Bit 1)

A sixteen pin Dip Socket is provided on the 2/4 channel serial I/O Board to accommodate an optional auto-answer piggy-back board. The auto-answer circuitry is contained on a PCB that is dimensionally scaled down to allow simultaneous placement with the existing bus interface controller (BIC) emulator board. The ring indicator signal (CE) for each channel is prioritized with channel one having the highest priority. Data and End-of-Block (EOB) interrupts all have priority over the ring interrupts. Each channel ring interrupt will vector to a unique memory address. ~~Refer to Paragraph 6.4.1.~~

0 Auto Answer Disable
 1 Auto Answer Enable

Test (Bit 2)

The test bit enables internal wrap-around between channel pairs. The bit is set during execution of a diagnostic program in the ISOLITE ROM.

5. This have meaning for software people?

$\emptyset$ Test Disabled (Normal Operation)
 1 Local Loop-Back

Board Reset (Bit 3)

The reset bit holds all UARTs/channels in the reset state. When bit 3 = $\emptyset$, the Serial I/O Board is inoperative.

$\emptyset$ Reset
 1 Normal

Auto Echo (Bits 4-7)

These bits instruct the Serial I/O Controller to echo received data back to the peripheral device that originally transmitted it. The feature is enabled for each channel independently by setting bits 4-5 (4-7 for four channel version) to a logic "1". The correspondence between channel number and board control word bit number is ~~shown~~^{repeated} in Figure —.

If In the Auto Echo mode, received data is automatically directed to the TXD line while normal receive operation continues. The receiver must be enabled ^(see Sec. 4.3.2) (~~CR2=1~~), but the transmitter need not be enabled.

CPU to receiver communications continue normally, but the CPU to Transmitter link is disabled.

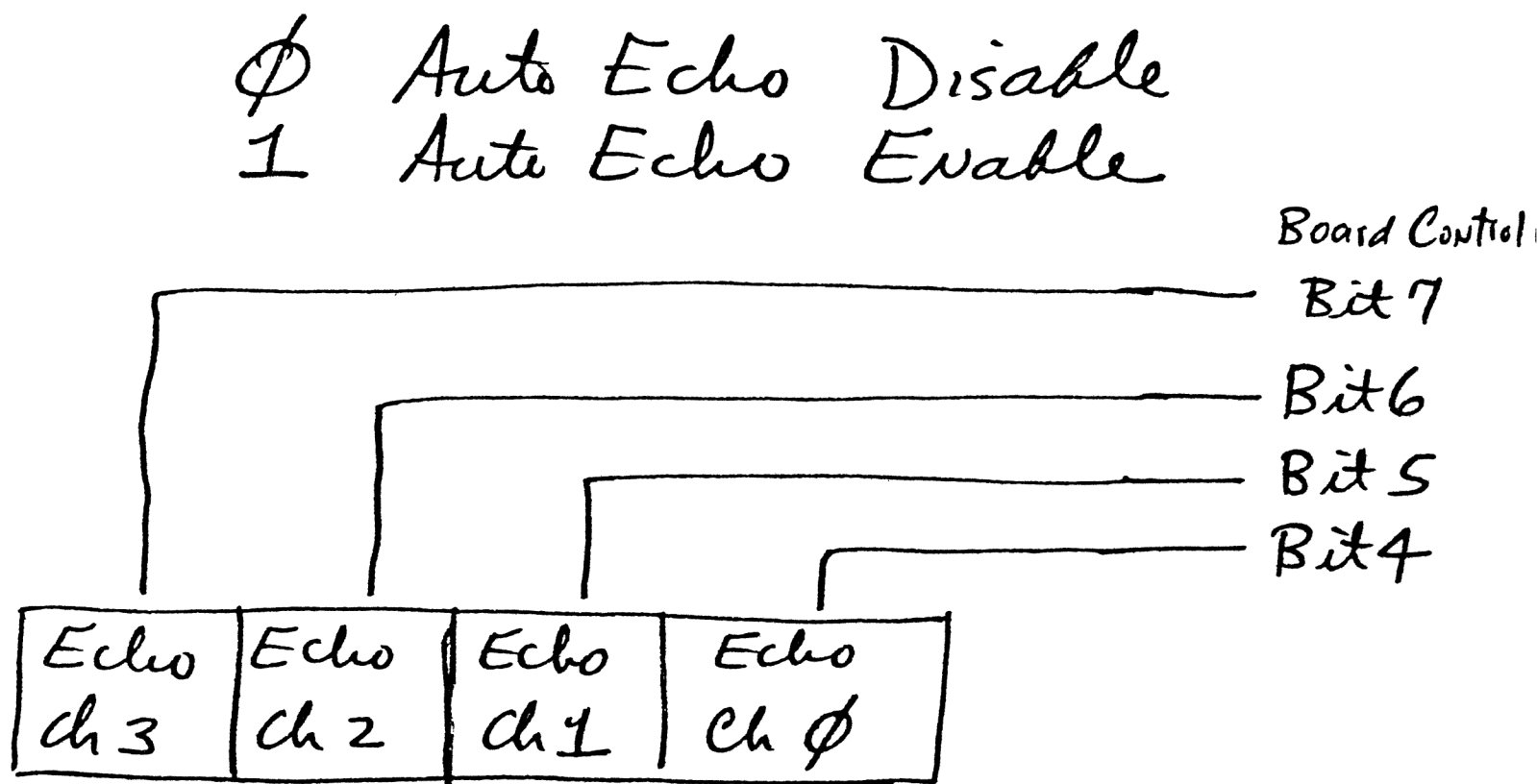


Figure — Board Control Word Bit Identification for Auto Echo

4.2.2 Write Interrupt Vector Base Address

~~The~~ This word defines the starting address for the block of interrupt vectors to be generated by the Serial I/O controller. When a data interrupt is generated, the CPU responds with a read vector condition code. The interrupt vector transmitted to the CPU consists of the base address (bits 7-12), ~~together with a~~ ^{and possibly a} displacement.

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(bits 2-6) ^{that is dependent} ~~depending~~ on the source of the interrupt. Bits 0 and 1 are always zero to allow four program instructions at each vector. To write the Interrupt Vector Base Address to the Serial I/O Controller using the SLP instruction, the format of the specified register content is shown in Figure —.

polish (

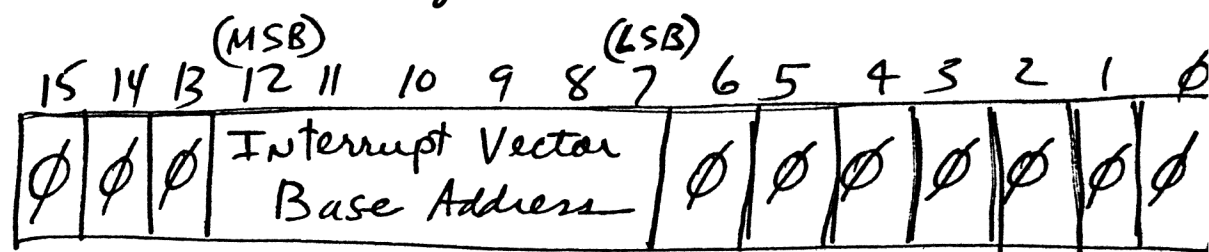


Figure — Format for Interrupt Vector Base Address

The actual interrupt vector generated by the Serial I/O Controller in response to the read Vector Condition Code from the CPU ~~is~~ depends on the event that initiated the interrupt request.

Data interrupt vectors are as follows: Note: Interrupt indexes listed below are in hexadecimal notation. Channels 3 & 4 are not applicable to 2 channel version of the Serial I/O Board.

Vector Base Address + 0	Channel 1 - Read
Vector Base + 8	Channel 2 - Read
Vector Base + 10	Channel 3 - Read
Vector Base + 18	Channel 4 - Read
Vector Base + 20	Channel 1 - Transmit
Vector Base + 28	Channel 2 - Transmit
Vector Base + 30	Channel 3 - Transmit
Vector Base + 38	Channel 4 - Transmit

EOB interrupt vectors are as follows:

Vector Base Address + 4	Channel 1 - Read
Vector Base Address + 0C	Channel 2 - Read
Vector Base Address + 14	Channel 3 - Read
Vector Base Address + 1C	Channel 4 - Read
Vector Base Address + 24	Channel 1 - Transmit
Vector Base Address + 2C	Channel 2 - Transmit
Vector Base Address + 34	Channel 3 - Transmit
Vector Base Address + 3C	Channel 4 - Transmit
Vector Base Address + 40	Channel 1 - Ring Interrupt
Vector Base Address + 44	Channel 2 - Ring Interrupt
Vector Base Address + 48	Channel 3 - Ring Interrupt
Vector Base Address + 4C	Channel 4 - Ring Interrupt

4.3 CHANNEL CONTROL FUNCTIONS

If Channel control functions are software programmable controllable operations that affect only one specified channel. Channel communication is accomplished by means of IN, OUT, or SELP I/O instructions. Input to Register (IN) transfers a 16-bit data word from the addressed I/O controller to a specified register. Output from Register (OUT) transfers the 16-bit contents of the specified register to the addressed I/O controller. The SELP is used to program a special character detection RAM for the selected channel (see Section 4.3.3). Channel functions together with their respective I/O instructions are ~~listed~~ shown in Figure —. The binary format for channel control functions is shown in Figure —.

<u>Function</u>	<u>I/O Instruction</u>
Read Channel Status/Station ID	IN
Write Channel Mode Word	OUT
Write Channel Control Word	OUT
Write Special Character RAM	SELP

Figure — Channel Functions

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	ϕ
ϕ	R2	$\phi\phi$	C3	DA				ϕ	CH	FC					

R2 $\phi\phi$, A Register
 $\phi 1$, X Register
 1 ϕ , Q Register
 11, Y Register

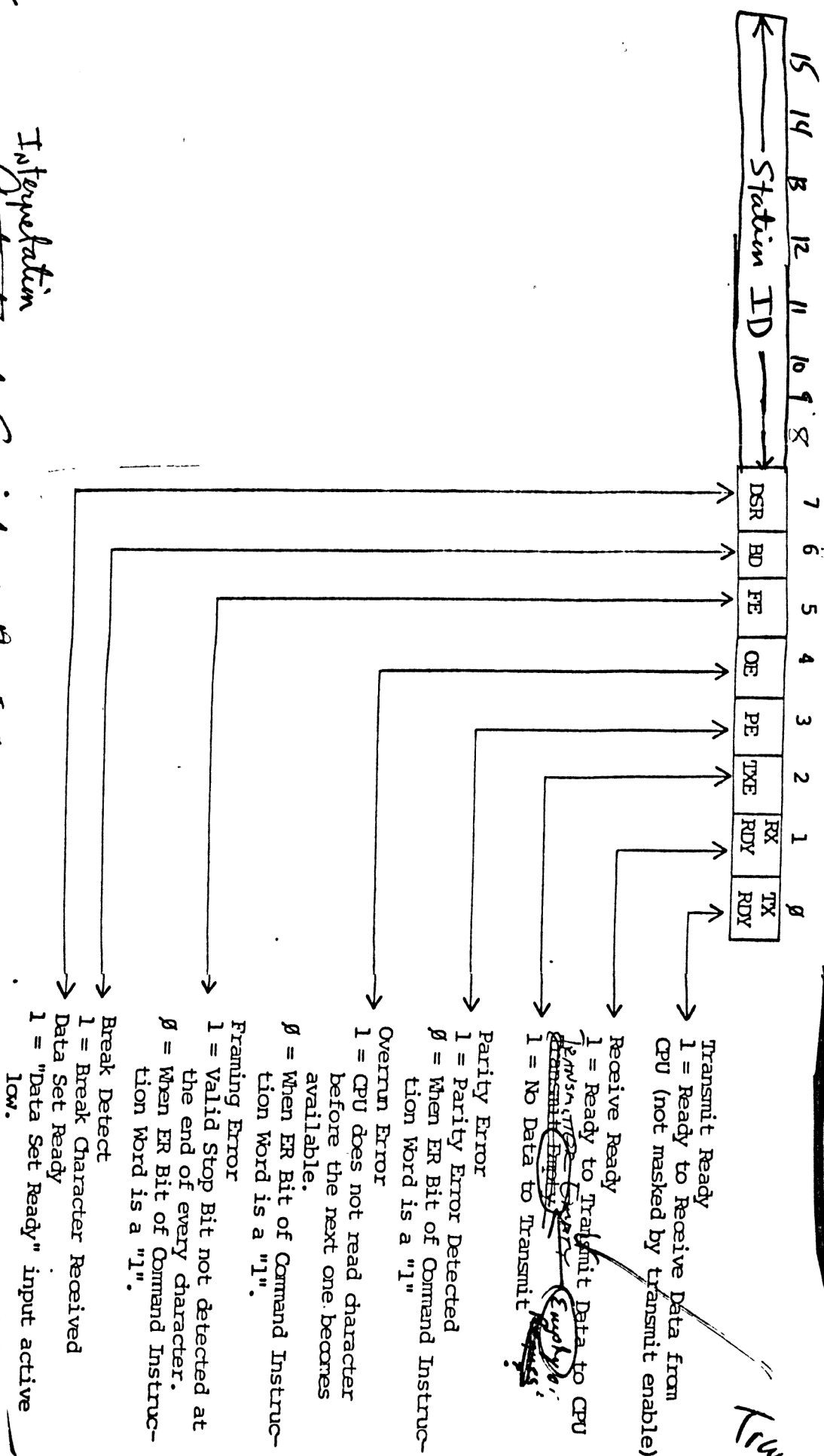
CH $\phi\phi$ Channel ϕ
 $\phi 1$ Channel 1
 1 ϕ Channel 2
 11 Channel 3

Instruction (Function)	C3	FC
Read Channel Status/ Station ID	$\phi\phi 1$	1
Write Channel Mode Word	$\phi 1\phi$	1
Write Channel Control Word	$\phi 1\phi$	1
Write Special Character RAM	1 $\phi\phi$	ϕ

Figure — Binary Format for Channel Control Functions

4.3.1 IN Instruction

④ An IN instruction with $FC=1$ loads Station ID information into the upper byte of the specified register, and loads UART/channel status information into the lower byte. This is shown in Figure —.



Transmitter Busy

Figure — Interpretation of Specified Registers
with $FC=1$

4.3.2 OUT Instruction

An OUT instruction with $FC=1$ generate either channel mode word information or channel control word information, depending on sequential order. The first word written to the UART (channel) following a system or channel reset is the mode word. All subsequent words ($FC=1$) written to the UART (channel) are control words. Interpretations of register contents ~~for~~ using an OUT instruction with $FC=1$ are shown in Figures — and —. Only the lower byte of the register content is used by the Serial I/O Controller,

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7	6	5	4	3	2	1	0
S2	S1	E/O	PE	L2	L1	1	0

Baud Rate Always = 10

Character Length

0	1	0	1
0	0	1	1
5 bits	6 bits	7 bits	8 bits

Parity Enable

1 = Enable

0 = Disable

Even/Odd Parity

1 = Even

0 = Odd

Number of Stop Bits

0	0	1	1
0	1	0	1
invalid	1 bit	1.5 bits	2 bits

Figure — Interpretation of Specified Register Content For Channel Mode Word

go to next page



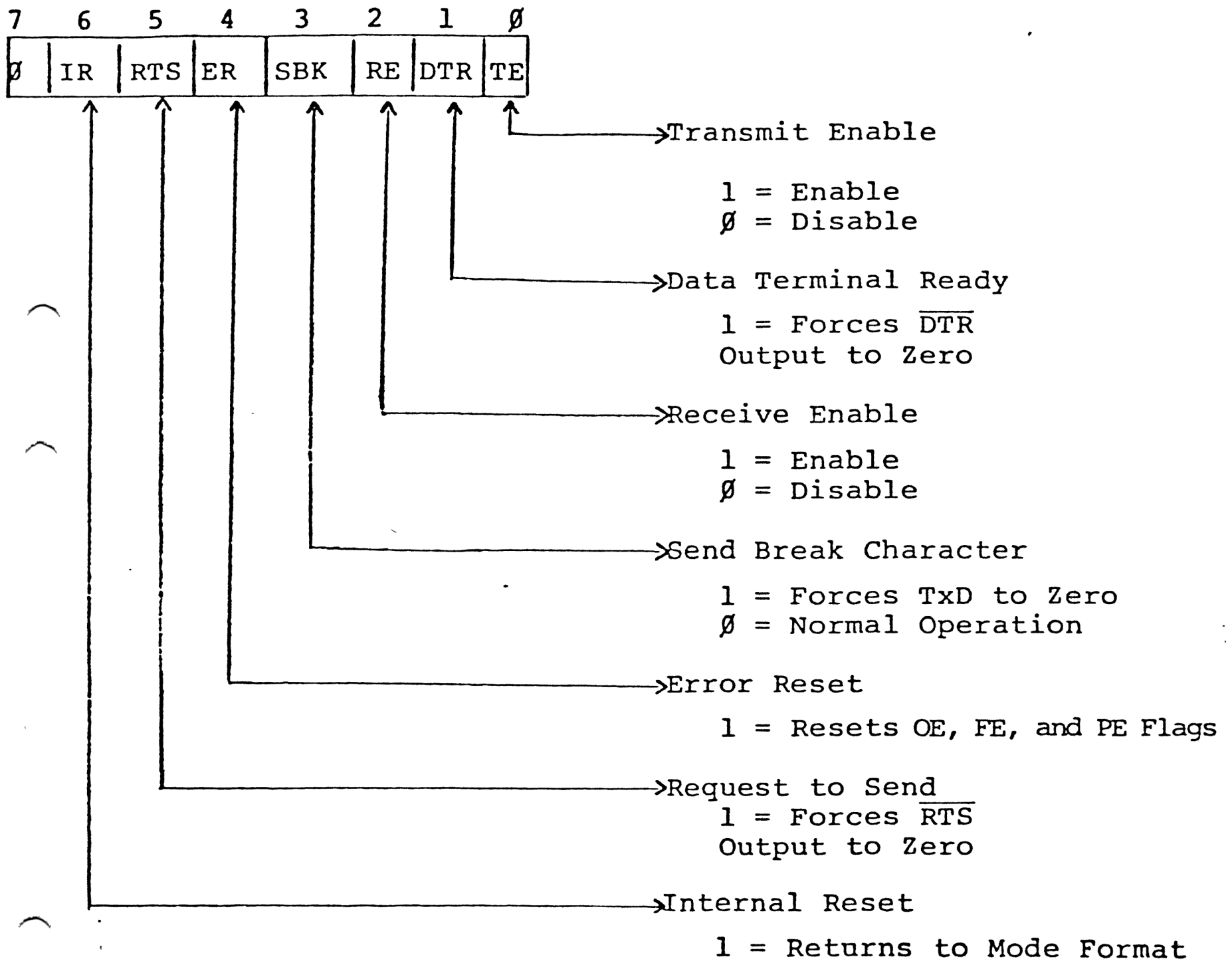


Figure — Interpretation of Specified Register Content For Channel Control Word

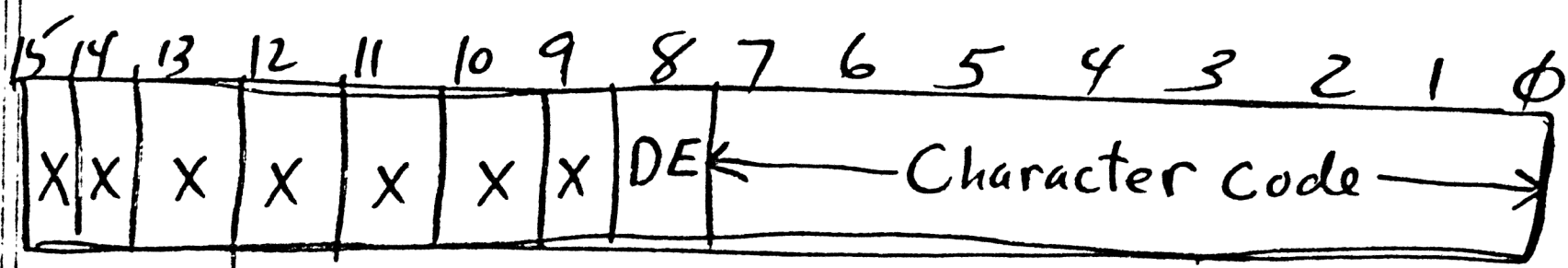
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4.3.3 SELP Instruction

If Each SELP instruction with FC bit ϕ = ϕ programs a location in the special character detect RAM corresponding both to the character code in the specified register and to the Channel specified by the SELP function code. Bit 8 in the specified register selects the character either as a special character or not as a special character, ~~and~~ shown in Figure —. The Serial I/O Board is capable of detecting 256 different special characters per channel. The detection of a special character generates a receive EOB interrupt. All possible character codes should be specifically enabled or disabled for special detection during the Initialization Routine for the board. If no special characters are required for any Channel, all 256 RAM locations for that channel must be filled with zeros to disable the detection feature.





DE: $\emptyset$ Special Character Detect Disable
 1 Special Character Detect Enable

Figure — Interpretation of Specified Register Content For Special Character Detection

4.4. DATA OPERATIONS

A Programmed data I/O instructions transfer ~~a single 8-bit byte from~~ the least significant byte of the specified register (A, Q, X, or Y) ~~to the~~ addressed Serial I/O controller. The controller works with two programmed I/O instructions:

IN (Input to Register)
 OUT (Output from Register)

Automatic I/O instructions cause a specified number of ~~words~~ bytes to be transferred one by one, between memory and an addressed I/O controller. These

(18)

instructions are always initiated by an interrupt, and are therefore defined only as 'interrupt instructions'.

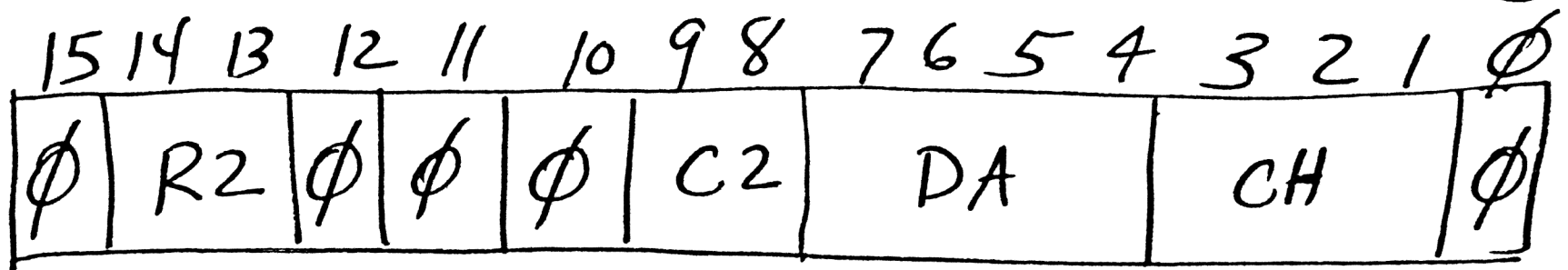
Q In addition to the vectored interrupt to the Automatic I/O instruction interrupt location, the Serial I/O controller will issue an additional interrupt when all required data has been transferred. This final interrupt, called an End of Block interrupt, provides a vector to the data interrupt location (Auto I/O instruction) + 4. The Serial I/O Controller supports two ~~Auto~~ I/O instructions:

AIB (Automatic Input Byte)

AOB (Automatic Output Byte)

The Programmed Data I/O instructions are single-word instructions, whereas the Automatic I/O instructions are three-word instructions.

Q The binary format for ^{Programmed I/O} data operations ~~in programmed I/O mode~~ is shown in Figure —, and for ^{Auto I/O} data operations ~~in Auto I/O mode~~ in Figure —.

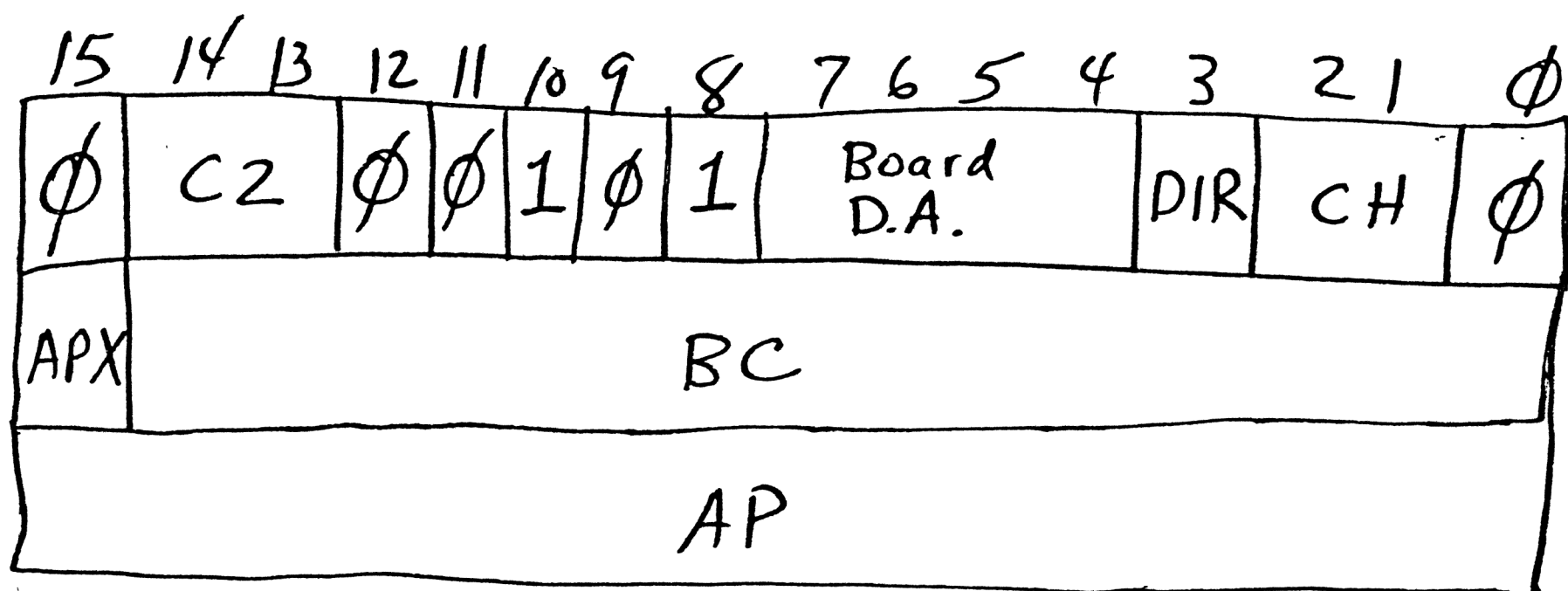


R2 00, A Register
 01, X Register
 10, Q Register
 11, Y Register

CH 000 Channel 0
 001 Channel 1
 010 Channel 2
 011 Channel 3

Instruction	C2
Read Data	01
Write Data	10

Figure — Binary Format for Programmed I/O data operations



Instruction

C2

Automatic Input Byte 10

Automatic Output Byte 11

DIR : bit which indicates direction of transfer (1 = output ; ϕ = input)

BC : low-order 15 bits of a 16-bit two complement of the word count or byte count

AP : 16-bit absolute address of the word/byte memory location that immediately precedes the starting transfer location (ie. $AP+1$ is the starting address)

APX : 1-bit complemented extension of the AP field that provides 128 K byte addressability, and specifies whether

AP addresses a byte in the lower 64K byte locations ($APX=1$) or the upper 64K byte locations ($APX=\emptyset$).

CH: $\emptyset\emptyset$ Channel $\emptyset$
 $\emptyset 1$ Channel 1
 $1\emptyset$ Channel 2
 11 Channel 3

Figure — Binary Format for Automatic I/O data operations