



RAM/PROM SEMICONDUCTOR MEMORY

1.1 INTRODUCTION

The RAM/PROM memory, for Naked Mini LSI Series Computers, is available in various 16-bit word configurations in the range of zero to 2K* words of RAM (in 1K increments) and zero to 4K words of PROM (in increments of 256). Access and cycle times are 1.6 μ s.

The RAM is a static MOS read-write device. The PROM is a 256 word x 8 bit read-only memory that is electrically programmable and eraseable by ultra violet radiation. The PROM array is designed to allow the devices to be programmed when mounted on the board. Except for memory banking and interleaving, other features of the LSI core memory are retained.

When programming PROM off the board, note that a high PROM output equals a zero and a low PROM output equals a one. Procedures for on-board programming of PROM are covered in the PROM Programmer User's Manual, 90-20550.

1.2 IDENTIFICATION

Memories are identified by RAM/PROM configuration and whether or not the battery backup option (BBU, paragraph 1.8) is present. The basic assembly number is 73-53595-xx.

RAM PROM	Without BBU			With BBU	
	0	*1K	*2K	*1K	*2K
0	00	10	20	60	70
256	01	11	21	61	71
512	02	12	22	62	72
1K	03	13	23	63	73
1.5K	04	14	24	64	74
2K	05	15	25	65	75
2.5K	06	16	26	66	76
3K	07	17	27	67	77
3.5K	08	18	28	68	78
4K	09	19	29	69	79

*K = 1024 words



1.3 INSTALLATION

A RAM/PROM memory is half-card size and installed in any slot in the 200 side of the motherboard (left side of motherboard as viewed from the rear). It is joined physically with a half-card I/O module or half-card "filler" card.

Joining the RAM/PROM memory with an I/O module or filler card can be accomplished in the field. A half-card memory is shipped with one card extractor mounted on the card and mounting blocks.

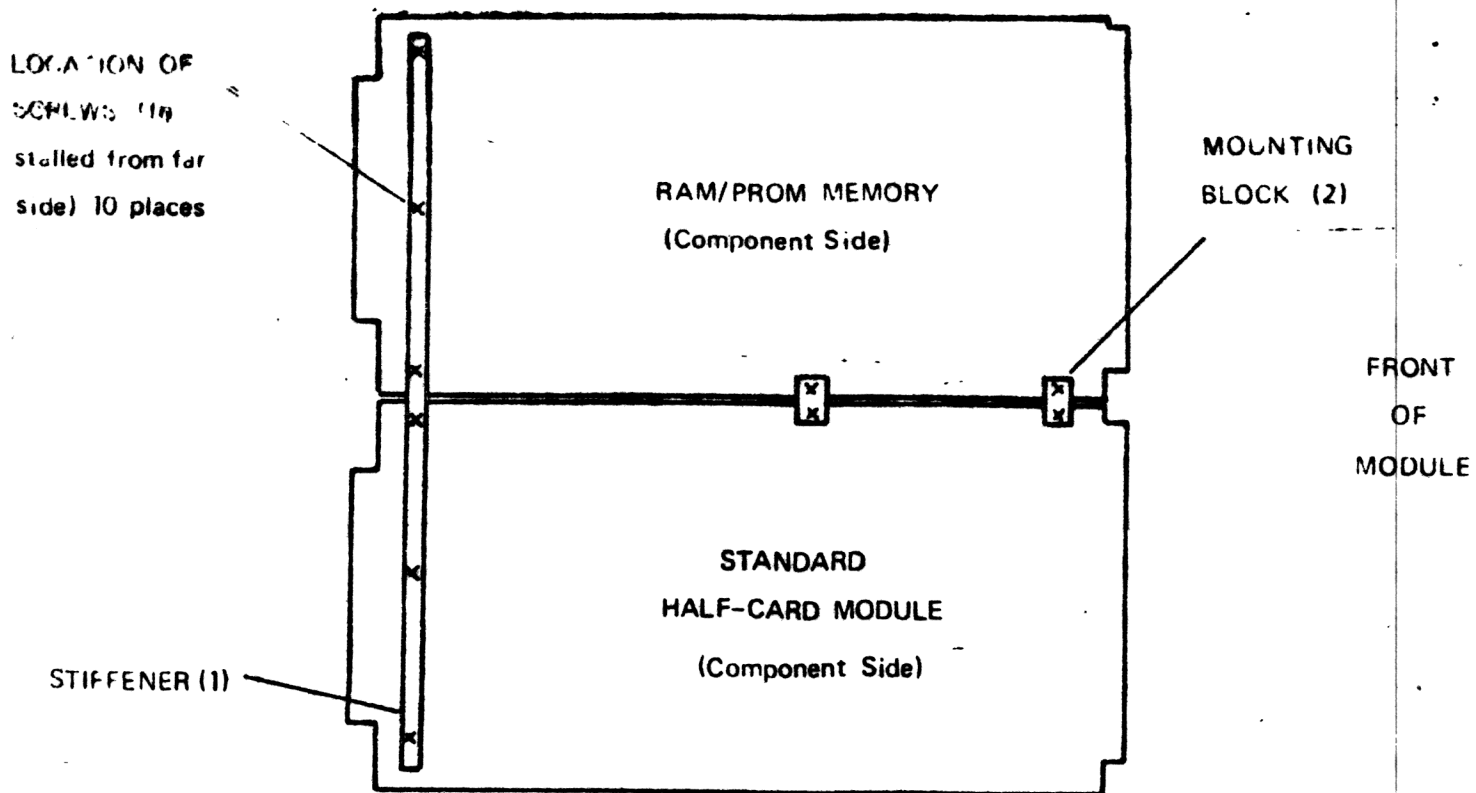


Figure 1. Joining Half-Cards

To join it with a standard half-card, proceed as follows:

- (a) Install the two plastic mounting blocks between the two cards (figure 1) by inserting two nylon screws (supplied with standard half-card) into tapped holes in each block from the solder side of the cards. Do not tighten screws firmly at this point.
- (b) Place stiffener at the rear edge of the component side of the cards as shown in the figure. Only one stiffener (supplied with the standard half-card) is used. Insert three nylon screws from the solder side of each card into tapped holes in the stiffener (total 6 screws), but do not tighten firmly.
- (c) Stand the cards (now joined as a single module) vertically on a level surface with the front edge down. Position the cards so that the sides are butted together and both front edge connectors are touching the level surface. Tighten each of the screws securely while maintaining position of the two cards.



UPPER LIMIT	S2-1	S2-2	S2-3	S2-4	S2-5	S2-6
LOWER LIMIT	-	S1-2	S1-3	S1-4	S1-5	S1-6
0	ON	ON	ON	ON	ON	ON
1K	ON	ON	ON	ON	ON	OFF
2K	ON	ON	ON	ON	OFF	ON
3K	ON	ON	ON	ON	OFF	OFF
4K	ON	ON	ON	OFF	ON	ON
5K	ON	ON	ON	OFF	ON	OFF
6K	ON	ON	ON	OFF	OFF	ON
7K	ON	ON	ON	OFF	OFF	OFF
8K	ON	ON	OFF	ON	ON	ON
9K	ON	ON	OFF	ON	ON	OFF
10K	ON	ON	OFF	ON	OFF	ON
11K	ON	ON	OFF	ON	OFF	OFF
12K	ON	ON	OFF	OFF	ON	ON
13K	ON	ON	OFF	OFF	ON	OFF
14K	ON	ON	OFF	OFF	OFF	ON
15K	ON	ON	OFF	OFF	OFF	OFF
16K	ON	OFF	ON	ON	ON	ON
17K	ON	OFF	ON	ON	ON	OFF
18K	ON	OFF	ON	ON	OFF	ON
19K	ON	OFF	ON	ON	OFF	OFF
20K	ON	OFF	ON	OFF	ON	ON
21K	ON	OFF	ON	OFF	ON	OFF
22K	ON	OFF	ON	OFF	OFF	ON
23K	ON	OFF	ON	OFF	OFF	OFF
24K	ON	OFF	OFF	ON	ON	ON
25K	ON	OFF	OFF	ON	ON	OFF
26K	ON	OFF	OFF	ON	OFF	ON
27K	ON	OFF	OFF	ON	OFF	OFF
28K	ON	OFF	OFF	OFF	ON	ON
29K	ON	OFF	OFF	OFF	ON	OFF
30K	ON	OFF	OFF	OFF	OFF	ON
31K	ON	OFF	OFF	OFF	OFF	OFF
32K	OFF	ON	ON	ON	ON	ON

Table 1. Address Limit Code

AMOUNT OF RAM	SWITCH		
	S2-7	S2-8	S1-8
0	ON	OFF	X
1K (a)	OFF	ON	OFF
1K (b)	OFF	OFF	ON
2K	OFF	OFF	OFF

X = Doesn't matter
a = Normal 1K operation
b = Ghost memory (when board
is first memory in system)
Switch S1-7 is unused

Table 2. RAM Portioning Switch Positions
(See page 7 for setting of switch S1-1)

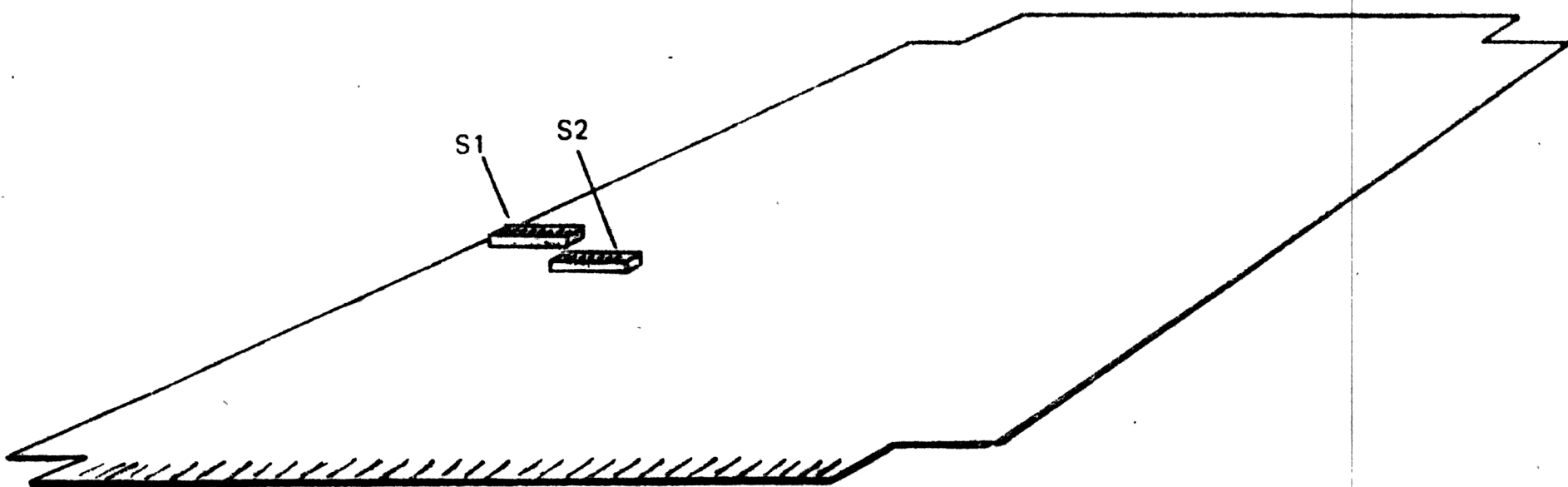


Figure 2. Switch Location

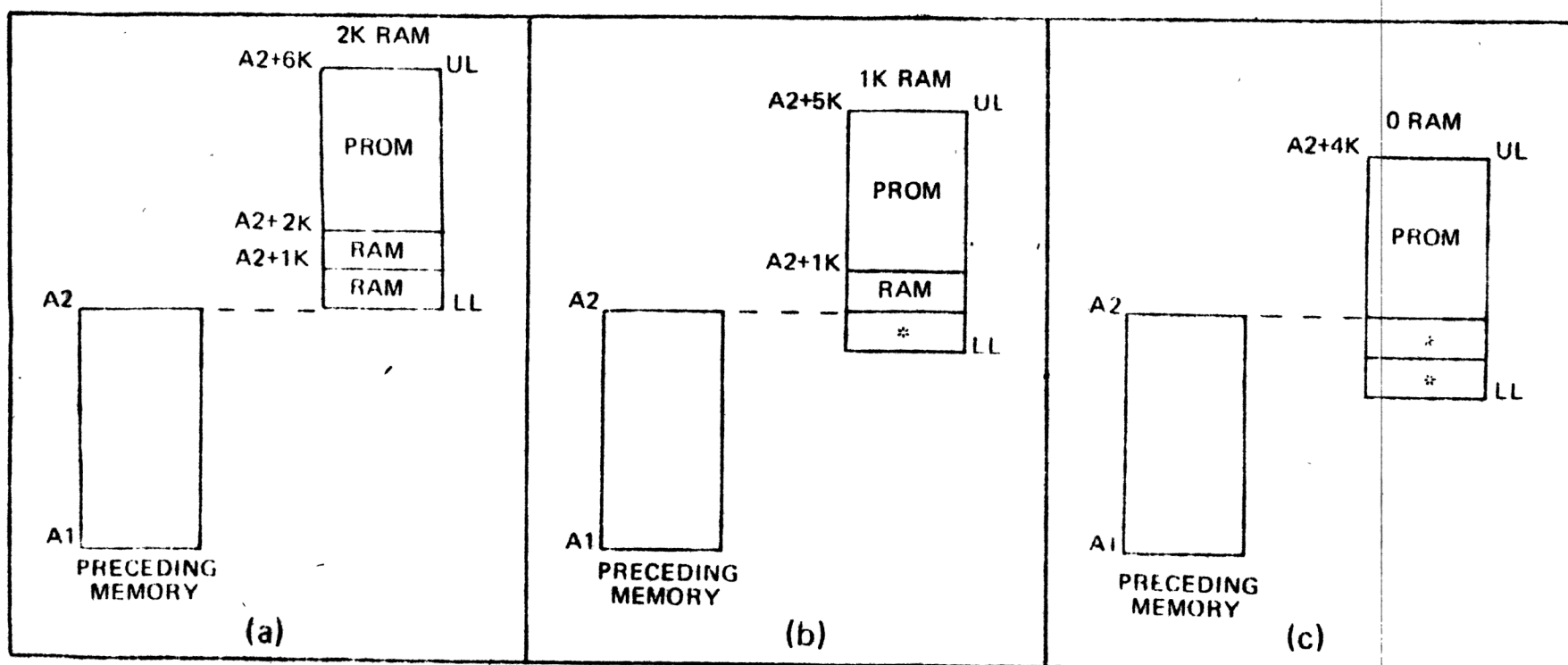
1.4 ADDRESSING

Upper and lower address limits are selected by two sets of switches labeled S1 and S2 located on the memory board (see figure 2). S1 selects the lower limit (LL); S2 selects the upper limit (UL). An input address received on the address bus is compared with the upper and lower address limits. If it is within limits, the memory card is activated.

Tables 1 and 2 tabulate the functions of switches S1 and S2 according to memory capacity configuration and option selection.

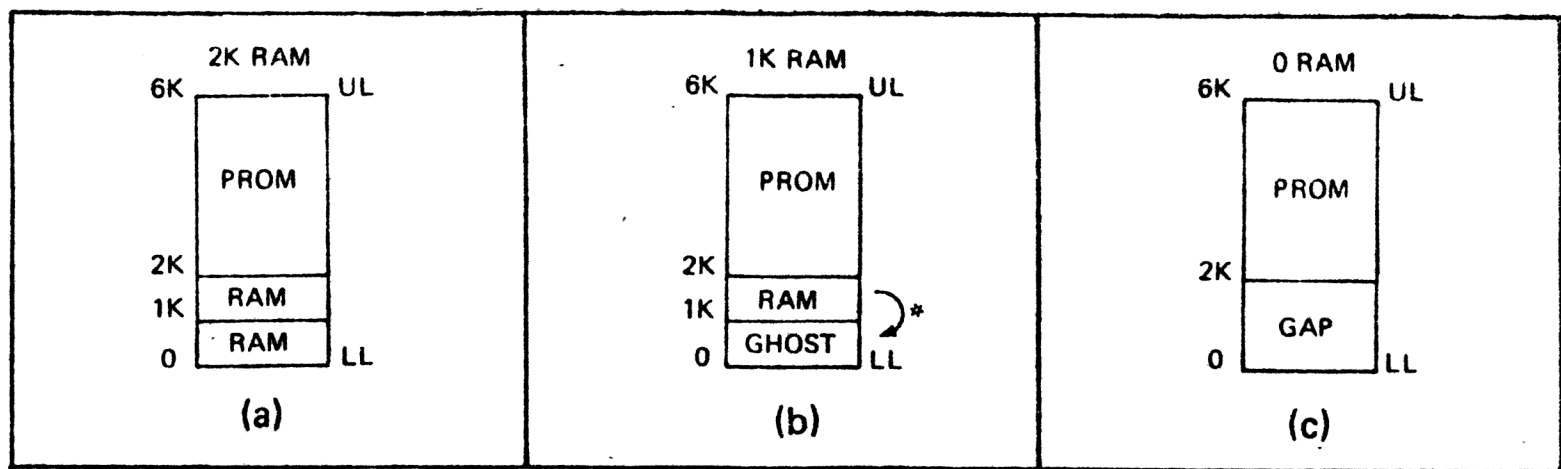
The following general rules apply:

1. Always set S1 (lower limit) 2K below the beginning address of PROM, regardless of the amount of RAM on the board.



* RAM response inhibited (S2-7 and S2-8).

Figure 3. Memory Allocation - Other Than First Memory



* S1-8 causes RAM response to both 1K and 2K of address.

Figure 4. Memory Allocation - First Memory

- Set S2 (upper limit) to the nearest address above PROM that is evenly divisible by 1K.

Figure 3a shows a RAM/PROM memory having 2K of RAM with the lower limit falling at the first RAM address. With memories having less than 2K of RAM, rule 1 results in a gap at the beginning of memory. To eliminate this gap, the memory can be inhibited from responding to the first 1K or 2K addresses within its boundaries by switches S2-7 and S2-8. This is shown in figure 3b (1K RAM) and figure 3c (0 RAM). The gap, in each case, is covered by the overlap from the preceding memory.

Figure 4a shows a RAM/PROM memory with 2K RAM installed as the first memory board in the system. Address 0 falls at first RAM address. A memory having 1K of RAM can use a "ghost memory" feature, selected by S1-8 in which the RAM responds to both the first and second 1K of address (figure 4b). The 1K of RAM can be portioned any way the programmer wishes. He can, for instance, use the first 0.5K words of RAM for addresses zero through 0.5K and the second 0.5K for address 1.5K through 2K. How the 1K of RAM is portioned depends upon programming.

NOTE

With the ghost memory feature, each location in RAM responds to two different addresses 1K apart, care must be taken to avoid accidentally writing over previously stored RAM data.

If a PROM-only board (no RAM) is installed as the first memory, there is an unavoidable gap from 0 to 2K (figure 4c).

1.5 MIXING RAM/PROM AND CORE MEMORIES

RAM/PROM memories and core memories can be mixed. Any core memory preceded by (further from the processor than) a RAM/PROM automatically has a start address immediately following the end address of the RAM/PROM. The start address of a RAM/PROM having 2K of RAM must be greater than the size of the preceding memory. With RAM/PROM cards having zero or 1K of RAM, the start address is overlapped by the upper 1K or 2K addresses of the preceding memory (see figure 5).

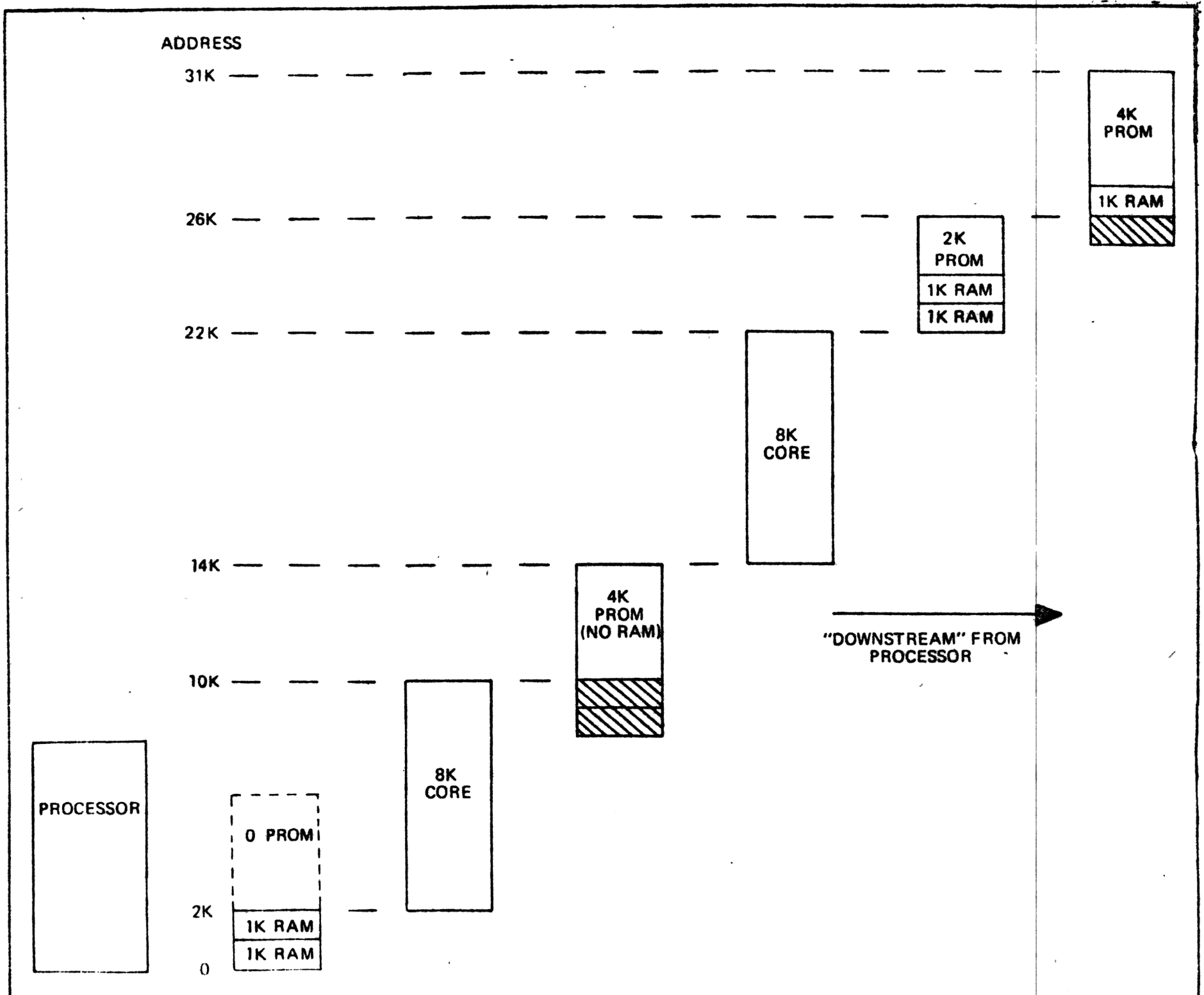


Figure 5. Example-Intermixed Memory Types

Memory gaps appear when the end address of the preceding memory is less than the manually-programmed start address of the following RAM/PROM or when the RAM/PROM end address is not an even multiple of 1K.

1.6 INVALID DATA DETECT (IDD)

All RAM/PROM memories which include RAM are equipped with invalid data detect logic which senses low voltage conditions that could cause loss of data from RAM. When RAM power drops below a safe level, an internal memory flag is set which causes the RAM to respond to a read command with all zeros on the data bus (NOP's). Read commands to PROM are not affected. A subsequent write command to any memory location in the system resets the IDD flag and normal operation follows--if power is restored to normal. This feature assures that, where the RAM/PROM is in the first memory position and following a power failure and restoration of power, execution will begin with the first PROM location and not in RAM.



1.7 AUTOMATIC START-UP (ASU)

The PROM can be used in place of the optional autoload ROM in the processor to store an autoload program. To do this, the processor must be equipped with the power fail/restart (PF/R) option. The RAM/PROM memory that contains the autoload program sequence in its first PROM locations must be in the first memory position or the first memory must contain a jump to the module containing the autoload program.

PROM is preprogrammed with the desired autoload program. When an autoload command is received (console AUTO switch or option card external autoload signal), the internal IDD flag is set to disable RAM. The PF/R or ASU option starts the computer running at location zero.

RAM addresses respond to read commands with all zeros (NOP's) causing the program counter to "ripple through" to the first PROM location. When PROM is reached, the autoload program is read out and executed.

The ASU Autoload feature can be disabled by switch S1-1:

ASU	S1-1
Disabled	On
Active	Off

For the ASU autoload (from PROM) feature to be operative, the standard autoload option (processor option) must not be installed. In addition, the motherboard must be strapped as follows: a strap from A133 to A116 (processor slot).

Note that when PROM Autoload is used, execution of the autoload program begins at the first location in PROM, as does a power-up restart condition. The two conditions are indistinguishable to the memory.

1.8 DATA RETENTION

1.8.1 Battery Backup Option (BBU)

The BBU option consists of an on-board 6-volt rechargeable nickel-cadmium battery, voltage regulator, and charging circuits. During a short-term loss of power, the battery takes over to prevent the RAM from losing data. The battery enables the RAM to retain data for a minimum of two minutes in a fully-populated RAM board. During normal operation, the battery automatically charges from the 12-volt supply. From full discharge, the battery fully charges in 12 hours. The battery supplies power only to the RAMs and associated circuits. Therefore, the computer is not operative on battery power. Only the on-board battery is charged by the BBU charging circuits.



Following a power failure, if BBU is installed and the PF/R or ASU option is present in the processor, execution begins normally at location zero and a RAM-resident power-up routine can be executed. If the battery discharged and RAM contents became invalid, the IDD feature takes over to cause the RAM to be skipped and the first PROM location to be executed when power is restored.

If the autoloader feature is used along with BBU, initiating autoloader causes the RAM to be skipped and the first PROM location to be executed. RAM contents remain valid and can be accessed following the first write command to any location in memory.

1.8.2 External Batteries

An external 6-volt battery, capable of retaining RAM data for at least 3 days, can be connected to a two-lug connector on the memory board. The battery, typically rack mounted, must supply 2 amps for boards having 2K of RAM and 1.2 amps for boards having 1K of RAM.

The BBU circuitry and the external battery connectors are arranged so that uninterrupted power is maintained on the RAMs even while the off-card source is being connected or disconnected, and whether or not the BBU option is installed or sufficiently charged.