



PART II

LSI-2/40 PROCESSOR

The LSI-2/40 processor is a higher speed version of the LSI-2/20 processor, built on a single, standard full card. The options available on the LSI-2/20 option card are standard features on the LSI-2/40, incorporated directly on the processor board. Differences in operation and installation between the LSI-2/20 and the LSI-2/40 are described here. For all other information, refer to the appropriate section in Part I of this manual.

1.1 OPERATIONAL CHARACTERISTICS

The LSI-2/40 is hardware and software compatible with systems designed around the LSI-2/20. However, software timing loops written for the LSI-2/20 must be changed to take into account the faster operation of the LSI 2/40. Because instruction cycle time is unpredictable in systems using a cache, use of software timing loops should be avoided, unless wide latitude is permissible. Unconditional I/O operations, i.e., operations that assume a device is ready at a given time in an instruction execution cycle, must also be reviewed in the light of faster LSI-2/40 operation. A representative set of instruction execution times for the LSI-2/40 in different system configurations is provided at the end of this part of the manual.

In addition to faster operation, the LSI-2/40 differs from the LSI-2/20 in the means of implementing the AutoLoad sequence. In the LSI-2/40, the AutoLoad sequence is entirely firmware controlled. The LSI-2/40 does not use memory fetch cycles to access the AutoLoad ROM and the instructions are not placed on the MAXI-BUS® interface. Instead, instructions are fetched from the AutoLoad ROM and placed in the instruction register via an internal data bus.

NOTE

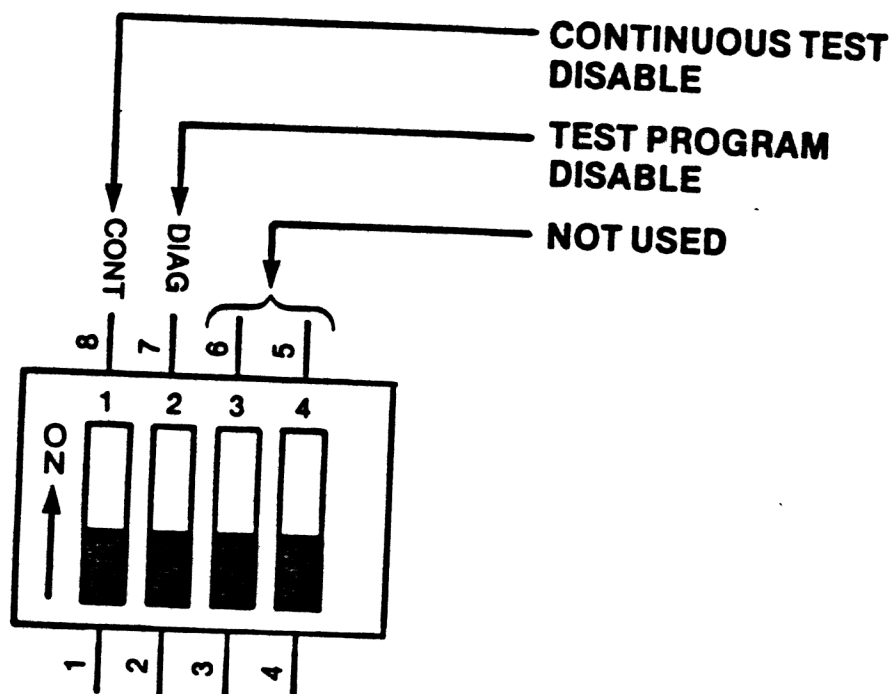
The ability to examine the contents of the AutoLoad ROM by mapping through location 7800 does not exist in the LSI-2/40. In addition, executing undefined op codes may produce different results in the LSI-2/40 than in the LSI-2/20. This is particularly important in that the LSI-2/40 only supports the following instructions at interrupt locations: IMS, JMP, JST, NOP and the Automatic I/O instructions. The HLT instruction is not supported at an interrupt location.



1.2 TEST PROGRAM/AUTOLOAD OPERATING SEQUENCES

The LSI-2/40 is provided with a test program option built into a ROM that can be installed on board. The test program can be enabled to run on power-up, followed by an AutoLoad/ AutoStart sequence, or enabled to run continuously until manually terminated via a switch on the board. The test program can also be disabled, in which case the processor enters the AutoLoad or AutoStart sequence, depending on the jumpering of the J1 connector. The connector jumpering procedure is identical with that for the LSI-2/20.

The test program operating sequence is determined by the setting of a switch on the board, designated SW1. The switch has two active elements. The test program is enabled if SW1-2 is in the OFF position. If running the test program is enabled, placing switch element SW1-1 in the OFF position causes the test program to run continuously. If SW1-1 is placed in the ON position, the test program cycles for two seconds and terminates. The relationship between the switch elements and the functions controlled is shown in Figure 1-1. The location of SW1 is shown in Figure 1-2. Table 1-1 shows the results produced by all combinations of switch settings. If the test program ROM is not installed, both switches must be placed in the ON (disable) position. Failure to do so results in undefined operation.



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Figure 1-1. Switch Block 1 Functions

The LSI-2/40 is equipped with an on board LED to indicate the result of running the test program. The LED lights when the test program ROM is accessed. The LED remains lit if the test program fails to run to completion, indicating a defective board. If the program is successfully completed, the LED is automatically turned off. The location of the LED is shown in Figure 1-2.



Table 1-1. Test Program Switch Settings

SW1-1	SW1-2	OPERATION
OFF	OFF	Test program runs continuously.
OFF	ON	Test program runs for two seconds.
ON	ON	Test program disabled.
ON	OFF	Test program disabled.

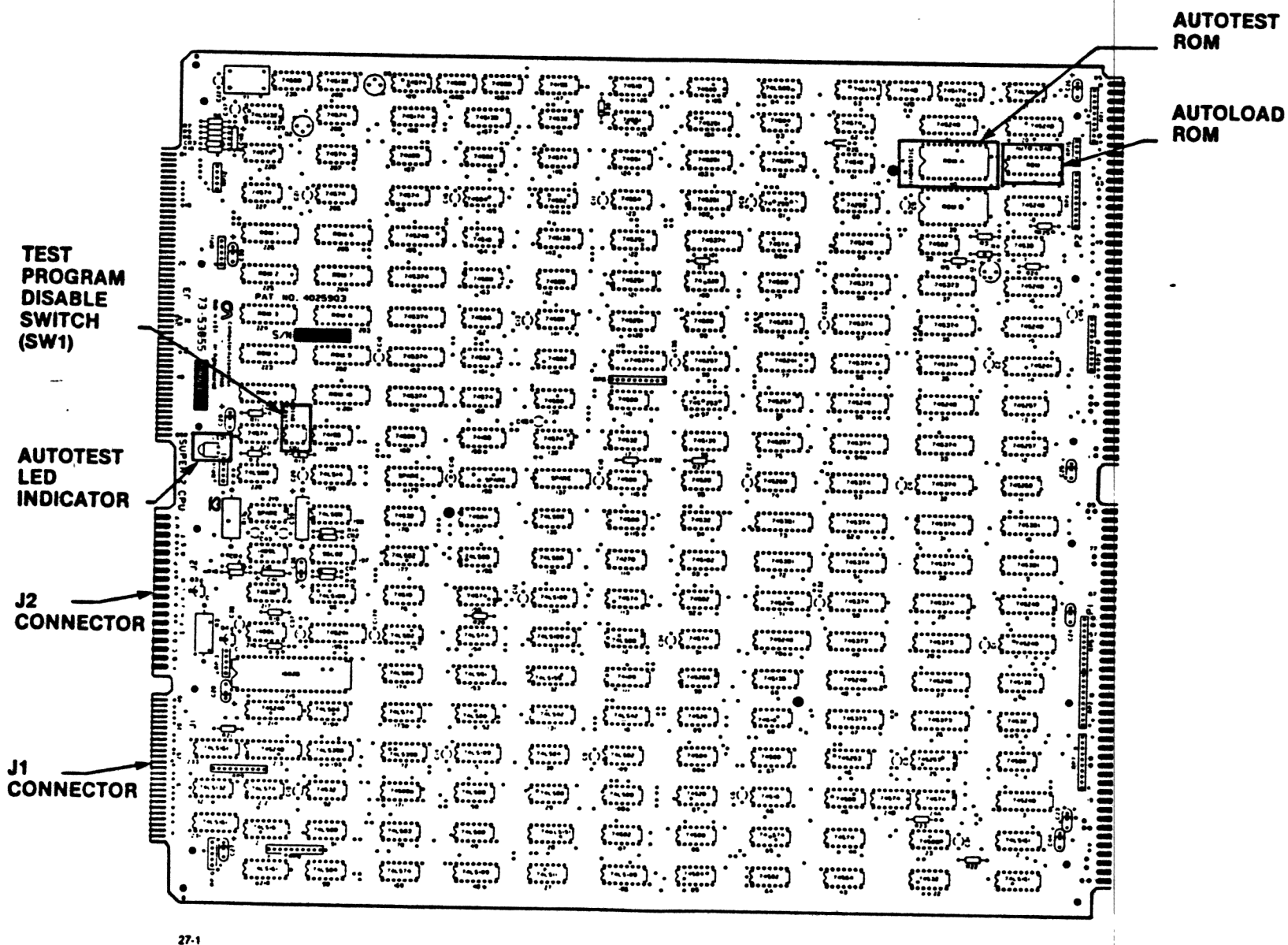


Figure 1-2. LSI-2/40 Board Layout



1.3 REAR-EDGE CONNECTORS

Rear-edge connectors J1 and J2 correspond to the same connectors on the LSI-2/20 Option Pack and are used for the same functions. The amount of clearance between the board edge connector and J1 requires that the cable connector used at J1 not have ears. Existing connectors can be modified or use a Viking 3VH25/1JN12 50-pin connector or equivalent.

1.4 INSTRUCTION EXECUTION TIMES

The LSI-2/40 processor implements the same instruction set used by the LSI-2/20 processor. Operation of the LSI-2/40 however, is faster. The difference in operation time between the processors, as well as the absolute operating times of the LSI-2/40, is highly system dependent. A representative listing of LSI-2/40 operating times in various system configurations is given in Table 1-2. Representative execution times for individual instructions are given in Table 1-3.

1.5 ELECTRICAL CHARACTERISTICS

The electrical characteristics of the LSI-2/40 processor MAXI-BUS® interface differ slightly from those of the LSI-2/20 processor. The LSI-2/40 MAXI-BUS® interface driver, receiver, and pull-up circuits are summarized in Table 1-4.

Table 1-2. Representative LSI-2/40 Operating Times
EXECUTION TIME IN NANOSECONDS

OVERHEAD OR OPERATION	2/40 WITH 1200 NS CORE	2/40 WITH 550 NS RAM	2/40 WITH CACHE & HIGH PERFORMANCE RAM (CACHE OFF)	2/40 WITH CACHE & HIGH PERFORMANCE RAM (CACHE ON)
ADDRESSING MODE OVERHEAD FOR SINGLE WORD MEMORY REFERENCE INSTRUCTIONS IN WORD MODE				
RELATIVE FORWARD	0	0	0	0
RELATIVE BACKWARD	0	0	0	0
INDEXED	0	0	0	0
SCRATCHPAD	0	0	0	0
INDIRECT RELATIVE FORWARD	1200	750	850	500
INDIRECT RELATIVE BACKWARD	1200	750	850	500
INDIRECT INDEXED	1200	750	850	500
INDIRECT SCRATCHPAD	1200	750	850	500
ADDRESSING MODE OVERHEAD FOR SINGLE WORD MEMORY REFERENCE INSTRUCTIONS IN BYTE MODE				
RELATIVE FORWARD	0	0	0	0
INDEXED	0	0	0	0
SCRATCHPAD	0	0	0	0
INDIRECT RELATIVE FORWARD	1200	650	750	400
INDIRECT INDEXED	1200	650	750	400
INDIRECT SCRATCHPAD	1200	650	750	400



Table 1-3. Representative LSI-2/40 Instruction Execution Times

INSTRUCTION MNEMONIC	INSTRUCTION EXECUTION TIMES IN NANOSECONDS			
	1200 NS CORE	550 NS RAM	HIGH PERFORMANCE RAM - CACHE OFF	HIGH PERFORMANCE RAM - CACHE ON
ADD	2400	1450	1550	800
ADDB	2400	1400	1450	1050
SUB	2400	1450	1550	800
SUBB	2400	1400	1450	1050
AND	2400	1450	1550	800
ANDB	2400	1400	1450	1050
IOR	2400	1450	1550	800
IORB	2400	1400	1450	1050
XOR	2400	1450	1550	800
XORB	2400	1400	1450	1050
LDA	2400	1450	1550	800
LDAB	2400	1400	1450	1050
LDX	2400	1450	1550	800
LDXB	2400	1400	1450	1050
STA	2400	1450	1350	900
STAB	2400	1400	1600	1250
STX	2400	1450	1350	900
STXB	2400	1400	1600	1250
EMA	3600	2150	2150	1300
EMAB	3600	2150	2400	2050
JMP	1200	850	900	500
JST	2400	1400	1300	900
IMS (WITH NO SKIP)	3600	2150	2100	1300
(WITH SKIP)	3600	2150	2100	1300
SCM (FIND MATCH IMMED)	3600	2700	2800	1700
SCMB (FIND MATCH IMMED)	3600	2550	2700	1850
CMS (NO SKIP)	2400	1650	1750	1000
(ONE SKIP)	2400	1750	1850	1100
(TWO SKIPS)	2400	1850	1950	1200
CMSB (NO SKIP)	2400	1650	1700	1200
(ONE SKIP)	2400	1750	1800	1300
(TWO SKIPS)	2400	1850	1900	1400
DVD (DIRECT)	11500	10400	10700	9500
(INDIRECT)	12600	10950	11300	9650
MPY (DIRECT)	9600	8600	8750	7600
(INDIRECT)	10600	9150	9350	7750
NRM (DIRECT)	6100	3750	3950	2400
(INDIRECT)	7200	4300	4550	2550
ADDRESSING MODES FOR STACK INSTRUCTIONS				
DIRECT	0	0	0	0
INDEXED	0	0	0	0
AUTO-PREDECREMENT	1200	700	550	450
AUTO-POSTINCREMENT	1200	700	550	450
ADDS	4800	2700	3300	1700
SUBS	4800	2700	3300	1700
ANDS	4800	2700	3300	1700
IORS	4800	2700	3300	1700
XORS	4800	2700	3300	1700



Table 1-3. Representative LSI-2/40 Instruction Execution Times (Continued)

INSTRUCTION MNEMONIC	INSTRUCTION EXECUTION TIMES IN NANOSECONDS			
	1200 NS CORE	550 NS RAM	HIGH PERFORMANCE RAM - CACHE OFF	HIGH PERFORMANCE RAM - CACHE ON
EMAS	6000	3400	3850	2150
LDAS	4800	2700	3300	1700
LDXS	4800	2700	3300	1700
STAS	4800	2700	3050	1800
STXS	4800	2700	3050	1800
CMSS (NO SKIP)	4800	2900	3400	1850
(ONE SKIP)	4800	3000	3500	1950
(TWO SKIP)	4800	3050	3600	2050
IMSS (NO SKIP)	6000	3400	4050	2050
(SKIP)	6000	3400	4050	2050
JMPS	3600	2100	2600	1450
JSTS	4800	2700	3050	1750
SLAS	3600	2200	2200	1500
AAI	1200	700	800	400
AXI	1200	700	800	400
SAI	1200	700	800	400
SXI	1200	700	800	400
CAI (NO SKIP)	1200	900	950	600
(SKIP)	1200	1000	1100	700
CXI (NO SKIP)	1200	900	950	600
(SKIP)	1200	1000	1100	700
LAP	1200	700	800	400
LXP	1200	700	800	400
LAM	1200	700	800	400
LXM	1200	700	800	400
JOC (NO SKIP)	1200	700	800	400
(SKIP)	1200	800	900	500
ARA (ONE SHIFT)	1200	1000	1100	700
ARX	1200	1000	1100	700
ALA	1200	1000	1100	700
ALX	1200	1000	1100	700
LRA	1200	1000	1100	700
LRX	1200	1000	1100	700
LLA	1200	1000	1100	700
LLX	1200	1000	1100	700
RRA	1200	1000	1100	700
RRX	1200	1000	1100	700
RLA	1200	1000	1100	700
RLX	1200	1000	1100	700
EACH ADDITIONAL SHIFT	100	100	100	100
LLL	1300	1100	1150	800
LLR	1300	1100	1150	800
LRL	1400	1250	1250	900
LRR	1300	1100	1150	800
EACH ADDITIONAL SHIFT	200	200	200	200
ZAR	1200	900	1000	600
ARP	1200	900	1000	600
ARM	1200	900	1000	600
CAR	1200	900	1100	700
NAR	1200	900	1000	600



Table 1-3. Representative LSI-2/40 Instruction Execution Times (Continued)

INSTRUCTION MNEMONIC	INSTRUCTION EXECUTION TIMES IN NANOSECONDS			
	1200 NS CORE	550 NS RAM	HIGH PERFORMANCE RAM - CACHE OFF	HIGH PERFORMANCE RAM - CACHE ON
IAR	1200	900	1000	600
DAR	1200	900	1000	600
ZXR	1200	900	1000	600
XRP	1200	900	1000	600
XRM	1200	900	1000	600
CXR	1200	900	1000	600
NXR	1200	900	1000	600
IXR	1200	900	1000	600
DXR	1200	900	1000	600
SOV	1200	900	1000	600
ROV	1200	900	1000	600
COV	1200	1000	1100	700
BAO (SAO)	1200	1000	1100	700
BAO (LAO)	1200	1000	1100	700
BXO (SXO)	1200	1000	1100	700
BXO (LXO)	1200	1000	1100	700
EACH ADDITIONAL SHIFT	100	100	100	100
ZAX	1200	900	1000	600
AXP	1200	900	1000	600
AXM	1200	900	1000	600
TAX	1200	900	1000	600
TXA	1200	900	1000	600
EAX	1200	900	1000	600
ANA	1200	900	1000	600
ANX	1200	900	1000	600
NRA	1200	900	1000	600
NRX	1200	900	1000	600
CAX	1200	900	1000	600
CXA	1200	900	1000	600
NAX	1200	900	1000	600
NXA	1200	900	1000	600
IAX	1200	900	1000	600
IXA	1200	900	1000	600
IPX	1200	900	1000	600
DAX	1200	900	1000	600
DXA	1200	900	1000	600
BCA	1200	900	900	650
BCX	1200	900	900	650
BSA	1200	900	900	650
BSX	1200	900	900	650
EIX	1400	1350	1400	1100
ICA	2200 *	2000 *	2000 *	1700 *
ICX	2200 *	2000 *	2000 *	1700 *
ISA	2200 *	2000 *	2000 *	1700 *
ISX	2200 *	2000 *	2000 *	1700 *
OCA	2000 *	1800 *	1850 *	1500 *
OCX	2000 *	1800 *	1850 *	1500 *
NOP	1200	800	900	500



Table 1-3. Representative LSI-2/40 Instruction Execution Times (Conclusion)

INSTRUCTION MNEMONIC	INSTRUCTION EXECUTION TIMES IN NANOSECONDS			
	1200 NS CORE	550 NS RAM	HIGH PERFORMANCE RAM - CACHE OFF	HIGH PERFORMANCE RAM - CACHE ON
SIN	2100	1900	1950	1600
SIA	2400	2200	2250	2100
SIX	2400	2200	2250	2100
SOA	2200	2000	2000	1700
SOX	2200	2000	2000	1700
EIN	1200	800	900	500
DIN	1500	1300	1400	1300
CIE	2000 *	1800 *	1850 *	1500 *
CID	2000 *	1800 *	1850 *	1500 *
PFE	2000 *	1800 *	1850 *	1500 *
PFD	2000 *	1800 *	1850 *	1500 *
TRP	2000 *	1800 *	1850 *	1500 *
SEL	2000 *	1800 *	1850 *	1500 *
SEA	2000 *	1800 *	1850 *	1500 *
SEX	2000 *	1800 *	1850 *	1500 *
SEN (NO SKIP)	1600 *	1400 *	1450 *	1100 *
(SKIP)	1700 *	1500 *	1550 *	1200 *
SSN (NO SKIP)	1600 *	1400 *	1450 *	1100 *
(SKIP)	1700 *	1500 *	1550 *	1200 *
INA	2200 *	2000 *	2000 *	1700 *
INAM	2200 *	2000 *	2000 *	1700 *
INX	2200 *	2000 *	2000 *	1700 *
INKM	2200 *	2000 *	2000 *	1700 *
OTA	2000 *	1800 *	1850 *	1500 *
OTX	2000 *	1800 *	1850 *	1500 *
OTZ	2100 *	1900 *	1950 *	1600 *
RDA	2200 *	2000 *	2000 *	1700 *
RDAM	2200 *	2000 *	2000 *	1700 *
RDX	2200 *	2000 *	2000 *	1700 *
RDXM	2200 *	2000 *	2000 *	1700 *
WRA	1900 *	1700 *	1800 *	1400 *
WRX	1900 *	1700 *	1800 *	1400 *
WRZ	1900 *	1700 *	1800 *	1400 *
IBA	2300 *	2100 *	2100 *	1800 *
IBAM	2300 *	2100 *	2100 *	1800 *
IBX	2300 *	2100 *	2100 *	1800 *
IBXM	2300 *	2100 *	2100 *	1800 *
RBA	2300 *	2100 *	2100 *	1800 *
RBAM	2300 *	2100 *	2100 *	1800 *
RBX	2300 *	2100 *	2100 *	1800 *
RBXM	2300 *	2100 *	2100 *	1800 *
SBM	1200 *	800 *	900 *	500 *
SWM	1200 *	800 *	900 *	500 *
AIN	8000 *	5200 *	5300 *	4000 *
AOT	7900 *	5100 *	5300 *	3600 *
AIB	8000 *	5200 *	5450 *	4200 *
AOB	7900 *	5100 *	5300 *	4250 *
* AMOUNT OF I/O STRETCH MUST BE ADDED TO THESE TIMES				



Table 1-4. MAXI-BUS® Interface Load, Drive and Termination Summary
for the LSI-2/40

SINGLE	PIN	MOTHER-BOARD DEVICE TYPE (S) (REFER TO NOTE 1)						
		CPU	MEMORY	I/O CONT	DMA CONT	CONSOLE	BUFFER	OPT PK
GND	1							
GND	2							
+12V	3							
+12V	4							
+12V	5							
+12V	6							
-12V	7							
-12V	8							
DPIN	9				5			
DPOT-	10		J	J	4		*	
EBSEL-	11							
	12							
+5V	13							
+5V	14							
MST-	15	1,6	5		1	5	5	5
ALSP-	16							
MACK-	17	5,7	2		5		2	2
RD-	18	1,6	5		2		5	
SLB-	20	1,6	5		1		5	2
PFD-	21	5,6			5		*	
MDIS-	22	8	5				5	
AB08-	23	1,6	5		1		5	
AB09-	24	1,6	5		1		5	
AB10-	25	1,6	5		1		5	
AB11-	26	1,6	5		1		5	5
GND	27							
GND	28							
AB12-	29	1,6	5		1		5	5
AB13-	30	1,6	5		1		5	5
AB14-	31	1,6	5		1		5	5
AB15-	32	1,6	5		1		5	
DB16-	33				5,6			
DB17-	34							
STOP-	35	5,6			2		2	
SACK-	36	3			5		5	
MBIN-	37		5					
MBOT-	38	4	4	J	J		*	
DB00-	39	1,5,6	1,5	2,5	1,5	2,5	1,5	1,2,5
DB01-	40	1,5,6	1,5	2,5	1,5	2,5	1,5	1,2,5
DB02-	41	1,5,6	1,5	2,5	1,5	2,5	1,5	1,2,5
DB03-	42	1,5,6	1,5	2,5	1,5	2,5	1,5	1,2,5
+5V	43							
+5V	44							
DB04-	45	1,5,6	1,5	2,5	1,5	2,5	1,5	1,5
DB05-	46	1,5,6	1,5	2,5	1,5	2,5	1,5	1,5
DB06-	47	1,5,6	1,5	2,5	1,5	2,5	1,5	1,5
DB07-	48	1,5,6	1,5	2,5	1,5	2,5	1,5	1,5
DB08-	49	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB09-	50	1,5,6	1,5	2,5	1,5	2,5	1,5	1



Table 1-4. MAXI-BUS® Interface Load, Drive and Termination Summary
for the LSI-2/40 (Continued)

MOTHER-BOARD		DEVICE TYPE(S) (REFER TO NOTE 1)						
SIGNAL	PIN	CPU	MEMORY	I/O CONT	DMA CONT	CONSOLE	BUFFER	OPT PK
DB10-	51	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB11-	52	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB12-	53	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB13-	54	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB14-	55	1,5,6	1,5	2,5	1,5	2,5	1,5	1
DB15-	56	1,5,6	1,5	2,5	1,5	2,5	1,5	1
EXEC-	57	1,6		5	1,5	5	5	5
IN-	58	1,6		5				
GND	59							
GND	60							
IOCL-	61	3,6		5	5	5	5	5
OUT-	62	1,6		5	1,5	5	5	5
CLK-	63	3,6		5	5	5		
SER-	64	5,6		2	2		2	2
IUR-	65	5,6		2	2		2	2
IL1-	66	5,6		2	2		2	
IAR-	67	1,6		5	5	5	5	5
IL2-	68	5,6		2	2		2	
RST-	69	2,5,6		5	5	2,5	2	5
IUA-	70	1,6		5	5		5	
PLSE-	71	1,7		5	5	5	5	5
ECHO-	72	1,6		5	5		5	
+5V	73							
+5V	74							
AB03-	75	1,6	5	5	1,5	5	5	5
AB04-	76	1,6	5	5	1,5	5	5	5
AB05-	77	1,6	5	5	1,5	5	5	5
AB06-	78	1,6	5	5	1,5	5	5	5
AB07-	79	1,6	5	5	1,5	5	5	5
AB00-	80	1,6	5	5	1,5	5	5	5
AB01-	81	1,6	5	5	1,5	5	5	5
AB02-	82	1,6	5	5	5			5
PRIN-	83		J	5	4		*	4
PROT-	84	4						
GND	85							
GND	86							

NOTES:

1. DEVICE TYPES ARE AS FOLLOWS:
 - 1) TRI-STATE DRIVER, 32-mA (8835 or EQUIV)
 - 2) 32-mA OPEN-COLLECTOR DRIVER (7438 or EQUIV)
 - 3) 32-mA TTL DRIVER (7437 or EQUIV)
 - 4) 16-mA TTL DRIVER (7400 or EQUIV)
 - 5) TTL RECEIVER (7404 or EQUIV)
 - 6) PULL-UP RESISTOR (1Ω)
 - 7) PULL-UP RESISTOR (300Ω)
 - 8) 100 mA OPEN-COLLECTOR DRIVER W/PULL-UP

2. THESE PINS CARRY SPECIAL SIGNALS ON SLOT A100 AND ARE RESERVED FOR FUTURE EXPANSION ON THE REMAINING 100 and 200 SERIES CONNECTORS.
3. EDSEL-, PIN 211, IS USED FOR TEST ONLY.