

BUS MONITOR REFERENCE MANUAL

53718-91

MAY 1981



**Engineering Reference Number
91-53718-00B0**

NAKED MINI® Division

**HERTFORD HOUSE
DENHAM WAY, MAPLE CROSS
RICKMANSWORTH, HERTFORDSHIRE WD3 2XD**

Telephone Rickmansworth 71211 Telex 922654

Printed in U.S.A.

REVISION HISTORY

<u>Revision</u>	<u>Issue Date</u>	<u>Comments</u>
A0	Aug. 1978	Original Issue
B0	May 1981	Incorporates miscellaneous text revisions.

WARNING: This equipment generates, uses, and can radiate radio-frequency energy and, if not installed and used in accordance with the instructions manual, may cause interference with radio communications. As permitted temporarily by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

Computer Automation, Inc., reserves the right to make changes in specifications at any time and without notice. The information furnished by Computer Automation, Inc., in this publication is believed to be accurate and reliable. However, no responsibility is assumed by Computer Automation, Inc., for its use; nor for any infringements of patents or other rights of third parties resulting from its use. No license is granted under any patents or patent rights of Computer Automation, Inc.

Computer Automation, Inc., welcomes comments and suggestions for improvements to our manuals. Should difficulty be encountered with the information in the manual or if you have a suggestion for manual improvement, please send the comments or suggestions to Computer Automation, Inc., Technical Publications, Department 11-0770, 18651 Von Karman, Irvine, California, 92713. Please provide as much information as possible to help evaluate the comment or suggestion.

PREFACE

The Bus Monitor Reference Manual contains a description of the module used to monitor the LSI-2, LSI-3/05 and NAKED MINI® 4 Family computers.

In addition to the system functional description, programming and installation sections are included. The programming section describes separately the LSI series and the NAKED MINI® 4 Family I/O instructions used to communicate with the Bus Monitor. The installation section includes information on system configuration, and device address and interrupt address selection.

The Bus Monitor Reference Manual assumes a familiarity with the applicable Computer Automation, Inc., Computer Reference Manuals and the MAXI-BUS® interface.

Related Documents:

20400-91	<u>LSI-2 Series Minicomputer Handbook</u>
10005-91	<u>LSI-3/05 Series Millicomputer Handbook</u>
20990-91	<u>LSI-4/10 Computer Reference Manual</u>
20991-91	<u>LSI-4/30 Computer Reference Manual</u>
20945-91	<u>LSI-4/90 Computer Reference Manual</u>
93015-90	<u>NAKED MINI® 4 Debugging Monitor Reference Manual</u>

CONTENTS

SECTION 1	GENERAL DESCRIPTION	
1.1	SYSTEM DESCRIPTION	1-1
1.2	SPECIFICATIONS	1-3
SECTION 2	FUNCTIONAL DESCRIPTION	
2.1	OPERATING VARIABLES	2-1
2.1.1	Skip Counter	2-1
2.1.2	Mode Logic	2-3
2.1.3	Compare Register	2-3
2.1.4	Run/Stop Latch	2-4
2.2	THE MONITORING OPERATION	2-4
2.2.1	Signal Stabilizer	2-4
2.2.2	Comparators	2-4
2.2.3	Control Decode	2-4
2.2.4	Interrupt or Reset	2-4
2.3	BUS MONITOR MEMORY	2-5
2.4	SYNCHRONIZING OUTPUTS	2-5
SECTION 3	PROGRAMMING	
3.1	INPUT/OUTPUT COMMAND USAGE	3-1
3.2	INPUT/OUTPUT COMMAND DESCRIPTION (LSI-2 and LSI-3/05)	3-2
3.2.1	Select Instruction	3-2
3.2.2	Output Instruction	3-2
3.2.3	Input Instruction	3-3
3.2.4	Programming Examples	3-6
3.3	INPUT/OUTPUT COMMAND DESCRIPTION (NAKED MINI® 4)	3-6
3.3.1	Select and Present Instruction	3-8
3.3.2	Output Instruction	3-8
3.3.3	Input Instruction	3-9
3.3.4	Sample Program	3-10
SECTION 4	INSTALLATION	
4.1	SYSTEM CONFIGURATION	4-1
4.2	ADDRESS ASSIGNMENTS	4-1
4.2.1	Device Address Assignments	4-1
4.2.2	Interrupt Vector Address	4-5
4.3	SKIP COUNTER SWITCH SETTING	4-6
4.4	J-2 CONNECTOR	4-6

4.5	TIMING CONSIDERATIONS	4-7
4.5.1	External Inputs	4-7
4.5.2	Comparison and Interrupt or Reset Considerations	4-7

FIGURES

Figure		Page
1-1	System Overview	1-2
2-1	Functional Diagram Bus Monitor	2-2
3-1	Mode Register Bit Configuration	3-4
3-2	Programming Example	3-7
3-3	Programming Example	3-11
4-1	Photograph of the Bus Monitor	4-2
4-2	Device Address Bit Assignments	4-3
4-3	Interrupt Vector Address Location Bit Assignment	4-5
4-4	Timing Considerations for the Bus Monitor	4-8

TABLES

Table		
4-1	Device Address Switch Settings	4-4
4-2	Skip Counter Select Switch Settings	4-6
4-3	J-1 Pin Mnemonics	4-5

SECTION 1

GENERAL DESCRIPTION

The Bus Monitor is used in conjunction with other troubleshooting aids to monitor the operation of the LSI-2, LSI-3/05 series, and NAKED MINI® 4 Family computers.

The Bus Monitor can monitor any or all memory addresses on the MAXI-BUS® interface. Every address monitored is simultaneously compared to each of three preset values; the CPU can be interrupted or the system reset upon detection of valid comparisons. The Bus Monitor can store a running history of the 80 most recent memory accesses monitored, the state of five MAXI-BUS® interface control lines, and three external inputs sampled in conjunction with memory access timing.

Used in conjunction with debugging programs, the Bus Monitor aids in analyzing and displaying software and hardware problems. For convenience, the Bus Monitor provides four oscilloscope synchronization signals keyed to valid comparisons and the state of the interrupt-reset signals.

1.1 SYSTEM DESCRIPTION

The Bus Monitor can monitor selectively any memory access on the MAXI-BUS® interface, whether originated by the I/O controller or CPU. Since the Bus Monitor communicates through the MAXI-BUS® interface, the Bus Monitor follows all the general MAXI-BUS® interface protocol.

When a device makes a memory access, the Bus Monitor samples the MAXI-BUS® interface at the beginning of the memory access cycle. This allows the Bus Monitor to perform its function in conjunction with the memory access cycle timing.

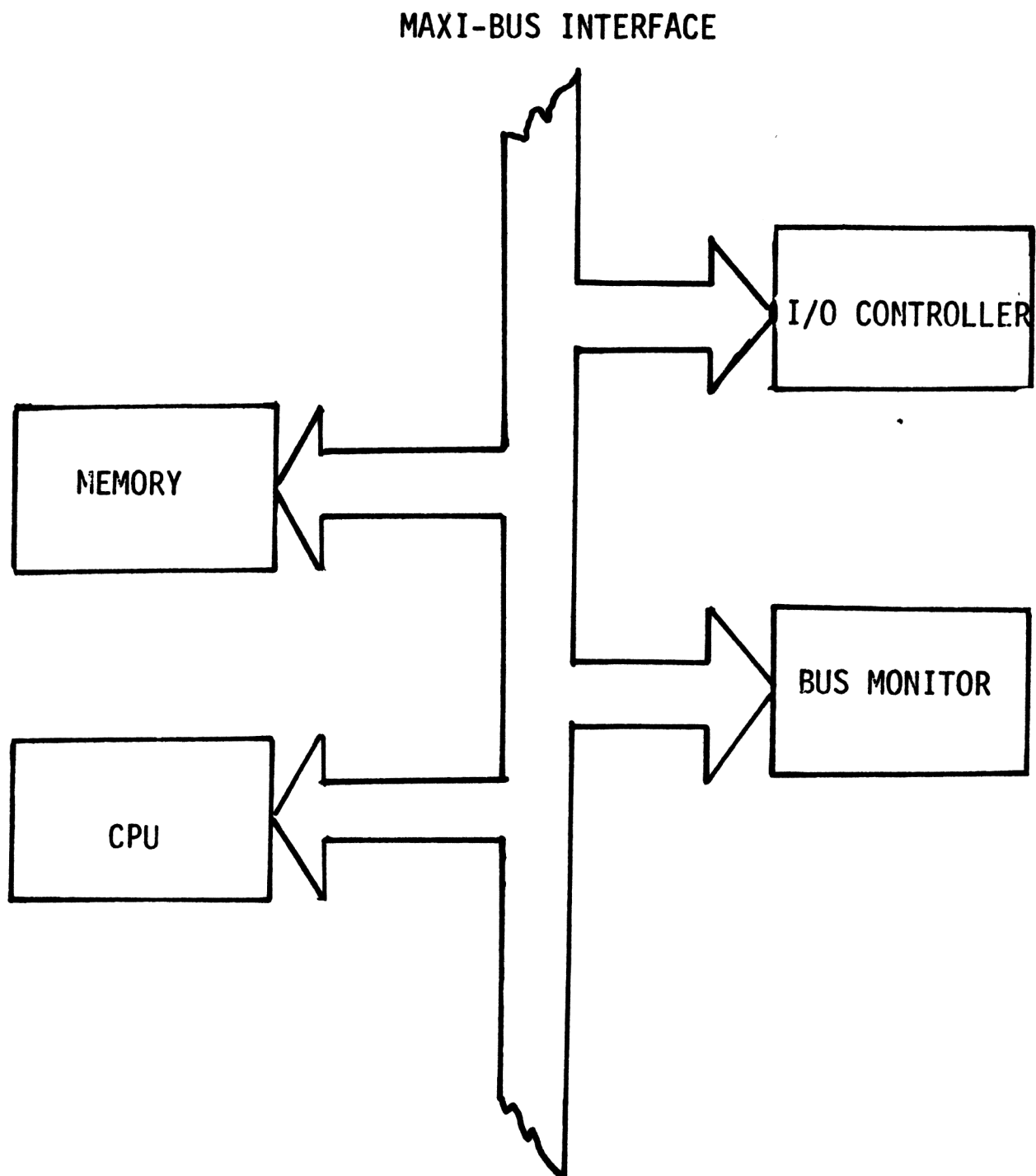


Figure 1-1. System Overview

1.2 SPECIFICATIONS

Power Requirements

+5 Vdc		1.2 A
-12 Vdc		0.3 A

Environment

Operating Temperature Range (Degrees Celsius)	. .	0 to +50
Non-operating Temperature Range (Degrees Celsius)		-20 to +100
Relative Humidity (Percent, Non-condensing)	. . .	10 to 90

Physical

Length		42.89 cm (16.886 in.)
Width		18.90 cm (7.480 in.)

Operational

Recommended Device Address		:16
Recommended Interrupt Address		:96

SECTION 2

FUNCTIONAL DESCRIPTION

The primary function of the Bus Monitor is to store the 80 most recent sample memory accesses. The Bus Monitor memory can be accessed by the CPU at any time for reference purposes. When the CPU accesses the contents of the Bus Monitor memory, the monitoring function of the Bus Monitor is stopped by a CPU initiated input instruction. The last address read out of the Bus Monitor memory is the most recent access stored. The storing of each selected memory access on the Bus Monitor is initiated at the beginning of the memory access cycle. When the Bus Monitor stores a memory access, a comparison is made and the present access is compared to preset values defined by stored operational variables.

The CPU stores a set of operational variables on the Bus Monitor to define the Bus Monitor operation. Under CPU control, the Bus Monitor is initialized to start or stop monitoring. The Bus Monitor then samples the MAXI-BUS® interface under the control of the operating variables. The monitoring and storage of memory addresses by the Bus Monitor is performed independent of the CPU.

Figure 2-1 illustrates the functional block diagram for the Bus Monitor.

2.1 OPERATING VARIABLES

The operating variables specify a set of operating parameters to control the operation of the Bus Monitor when the Bus Monitor is independently monitoring the system operation.

2.1.1 Skip Counter

The skip counter provides a manually-specified delay of the monitoring function of the Bus Monitor. The delay is caused by a value placed in the skip counter of up to 15 skip read memory operations. The value for the skip count is set manually at the time the Bus Monitor is installed into the system chassis. (Refer to Section 4)

The skip counter is loaded and the skip function is enabled when the Bus Monitor receives an instruction to start monitoring, which sets the Run/Stop latch to run. The skip counter then is incremented each time a read memory operation occurs. During the skip function, all write memory operations are ignored by the Bus Monitor. When the prescribed number of skip Read Memory instructions has been satisfied, the Bus Monitor proceeds to monitor the MAXI-BUS® interface under the control of the operational variables.

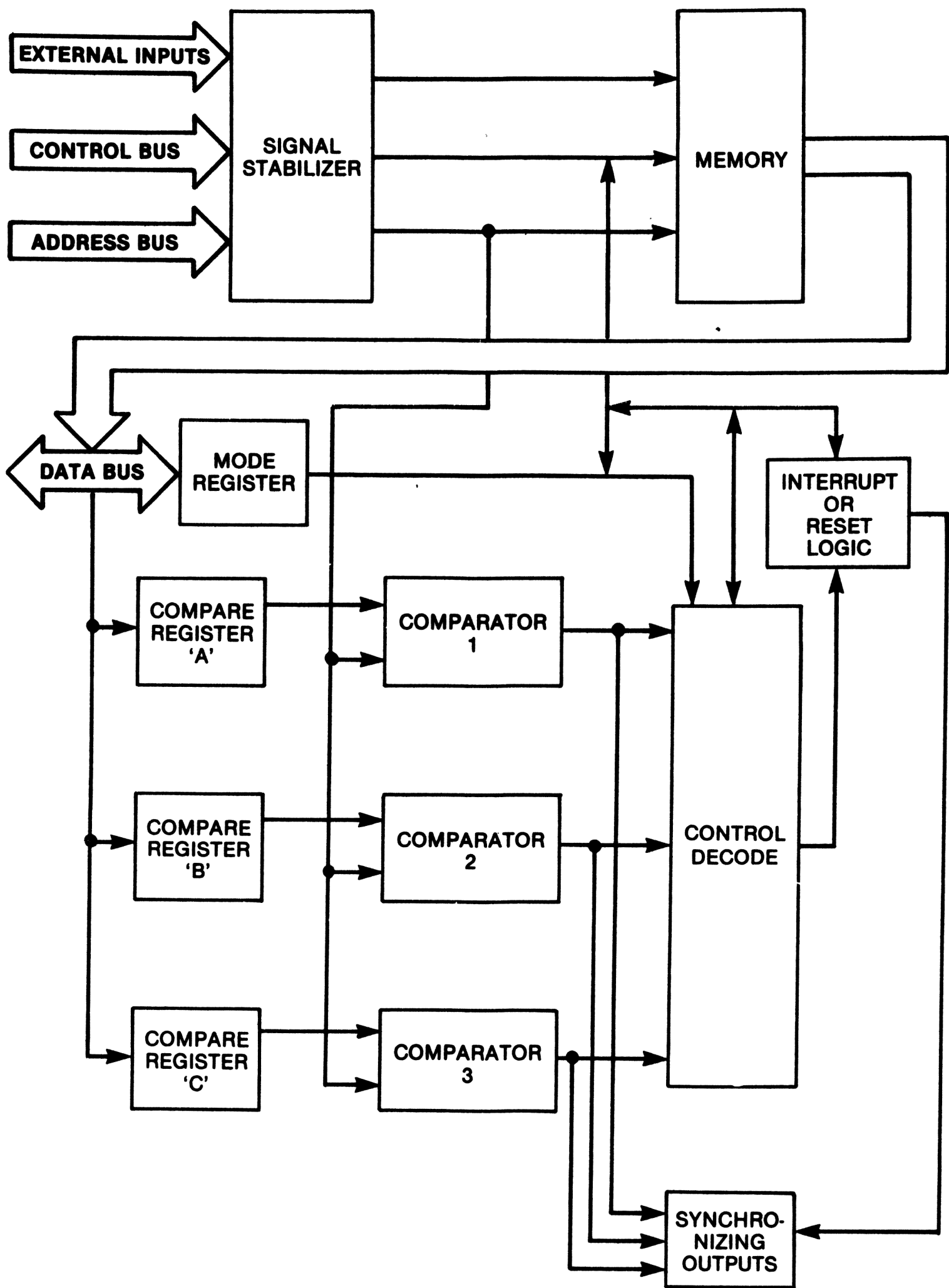


Figure 2-1. Functional Block Diagram

2.1.2 Mode Logic

The mode logic consists of a register and the related logic. The mode logic is used to control the comparators and associated logic through operational variables issued under program control.

Data is loaded into the mode register before the main body of the program is executed. This allows the selection of the action to be performed when a valid comparison is made. The mode register is loaded by the CPU using the output instruction. There are 16 mode register bits available of which 10 bits are used; bits 11 through 15 and bit 2 are non-selectable.

- Bits 0, 1 and 3 determine the type of memory access to be monitored in any combination.
- Bits 4 through 8 select the type of comparison to be performed.
- Bits 9 and 10 are used to determine the action to be taken upon a valid compare.

2.1.3 Compare Register

The Bus Monitor contains three compare registers loaded individually under program control. The compare registers are loaded prior to starting the main body of the program to specify the address used for comparison with the address bus. The compare registers are accessed by the comparators at the beginning of each memory access cycle.

2.1.4 Run/Stop Latch

The Run/Stop Latch is used to enable or disable the operation of the Bus Monitor.

The Run/Stop Latch is placed to stop when any of the following events occur.

- The Bus Monitor is initialized by receiving a select initialize instruction.
- The Bus Monitor detects a valid comparison.
- The Bus Monitor receives an input instruction to access the contents of the Bus Monitor's memory.
- The Bus Monitor receives a select stop instruction.

The Run/Stop Latch is placed to Run when the Bus Monitor receives a Select Run instruction.

2.2 MONITORING OPERATION

The monitoring and storage of memory addresses by the Bus Monitor is performed independent of the CPU. The Bus Monitor samples the MAXI-BUS® interface under the control of the operating variables stored in the Bus Monitor.

2.2.1 Signal Stabilizer

The signal stabilizer is a holding register which temporarily holds the contents of the address bus, five control signals from the C-Bus, and three external inputs.

While being held by the signal stabilizer, the contents of the address bus are available for use by the comparators.

The five control signals from the C-Bus are: stop acknowledge (SACK), select least significant byte (SLB), address bus bit 15 (AB15), interrupt request (IUR), and read (RD).

2.2.2 Comparators

The Bus Monitor includes three comparators to separately compare the address bus information in the signal stabilizer to the three compare registers. The comparator is controlled by the operational variables stored in the mode register. At the beginning of each memory access cycle, the comparisons are made and the result presented to the control decode logic.

2.2.3 Control Decode

Based on the inputs from the comparators, the control decode logic determines if a valid compare is present. The control decode logic then ignores the results of the compare, interrupts the CPU, or resets the CPU, depending on the action specified by the operating variables. This takes place during each memory access cycle being monitored.

2.2.4 Interrupt or Reset

The interrupt or reset logic determines when the Bus Monitor interrupts the computer or resets the system. The interrupt or reset logic is enabled by a 1 in bit 9 or 10 of the mode register with bit 9 specifying the reset and bit 10 the interrupt. The actual interrupt or reset is then generated in response to the signal from the control decode indicating a valid comparison was made.

2.3 BUS MONITOR MEMORY

The Bus Monitor contains a 24-bit wide, 80-word memory used to store the monitored memory addresses. The memory stores the 80 most recent accesses subject to the controls specified in the operating variables. Along with the memory address, the Bus Monitor memory stores five of the control bits from the MAXI-BUS® interface and external inputs.

The Bus Monitor accepts external inputs, for storage in the Bus Monitor memory. The inputs are located on the J-2 connector. Any TTL level signal (0 volts DC to +5 volts DC) stable at memory start time may be input on the user specified inputs.

2.4 SYNCHRONIZING OUTPUTS

The Bus Monitor provides four synchronizing outputs for an oscilloscope display. The synchronizing outputs are located on the J-2 connector. The signals are from the three compare registers and the interrupt or reset signal.

SECTION 3

PROGRAMMING

The Bus Monitor conforms to the general I/O programming philosophy presented in the computer reference manuals for the LSI-2, LSI-3/05 and the NAKED MINI® 4 Family of computers. The select instructions direct the operation of the Bus Monitor, while input and output instructions perform the required data transfers.

The detailed programming and operations information in the following subsections describes separately the I/O commands for the ALPHA LSI Family and the NAKED MINI® 4 Family used to communicate with the Bus Monitor.

NOTE

The Bus Monitor fully decodes the instructions detailed in the following subsections. Other instructions, output with the Bus Monitor device address, may be partially decoded and the resulting operation is unpredictable.

3.1 INPUT/OUTPUT COMMAND USAGE

All I/O commands issued to the Bus Monitor must be accompanied by the device address (DEVAD in the following descriptions) assigned to the Bus Monitor. Once a device address is selected on the Bus Monitor board (refer to Section 4), the same device address must be established in software. The EQU directive can be used to establish the assigned device address as a conveniently used mnemonic.

DEVAD	EQU	Address determined from system installation information
-------	-----	---

Assuming the standard device address :16, then:

DEVAD	EQU	:16%3	(or :B0)
-------	-----	-------	----------

This directive shifts the device address left three places to align the device address properly for use with the I/O instructions.

Some small assemblers do not recognize the shift directive. An alternate to the (%) shift directive is a (*) multiply. The directive would then be:

```
DEVAD    EQU        :16*8    (or :00B0)
```

In the same manner, the interrupt address must be established in software. The EQU directive can be used to establish the assigned interrupt address as a conveniently used mnemonic.

```
INTAD    EQU                    Address determined from system installation
                                   information
```

Assuming the standard interrupt address :96 then:

```
INTAD    EQU        :96
```

3.2 INPUT/OUTPUT INSTRUCTION DESCRIPTION (LSI-2 and LSI-3/05)

The I/O command descriptions are presented in assembly language format for easy use. The label (if used), mnemonic, and operands with appropriate function codes appear for each command. The following instructions are used to communicate with the Bus Monitor.

SEA	Select
OTA	Output A Register
OTX	Output X Register
INA	Input A Register
INX	Input X Register

3.2.1 Select Instruction

The Select instruction is used to initialize the Bus Monitor, start monitoring, and stop monitoring. Three function codes are used with the select instructions. The register specification in the following instructions serves to maintain a syntactically correct operand structure. The Bus Monitor ignores the contents of the register.

The Select initialize instruction is used by software to clear the mode register and the interrupt logic, and to set the RUN/STOP latch to STOP.

To Select initialize, use function code 4 in the form

```
SEA      A,DEVAD+4
```

The Select start instruction is used to initiate the monitoring operation. This instruction sets the RUN/STOP latch in RUN, and loads the preset switch settings into the Skip Counter.

To Select start, use function code 0 in the form

```
SEA      A,DEVAD+0
```

The Select stop instruction halts the monitoring function of the Bus Monitor and sets the RUN/STOP latch to STOP.

To Select stop, use function code 1 in the form

SEA A,DEVAD+1

3.2.2 Output Instruction

The OTA or OTX instructions load the contents of the A and X register into the specified compare register or the mode register. Four function codes are used with the output instruction to load the registers of the Bus Monitor.

Function code 1 is used to load the contents of the A or X register into the A compare register. The initialize instruction does not change the content of the A register.

To load the Bus Monitor A register, use function code 1 in the form

 OTA DEVAD+1
or
 OTX DEVAD+1

Function code 2 is used to load the contents of the A or X register into the B compare register. The initialize instruction does not change the contents of the B register.

To output to the Bus Monitor B register, use function code 2 in the form

 OTA DEVAD+2
or
 OTX DEVAD+2

Function code 3 is used to load the contents of the A or X register into the C compare register. The initialize instruction does not change the contents of the C register.

To load the Bus Monitor C register, use function code 3 in the form

 OTA DEVAD+3
or
 OTX DEVAD+3

Function code 4 is used to load the contents of the A or X register into the mode register. The initialize instruction does not change the contents of the mode register. The configuration of the Bus Monitor mode register is shown in Figure 3-1.

To load the Bus Monitor mode register, use function code 4 in the form

 OTA DEVAD+4
or
 OTX DEVAD+4

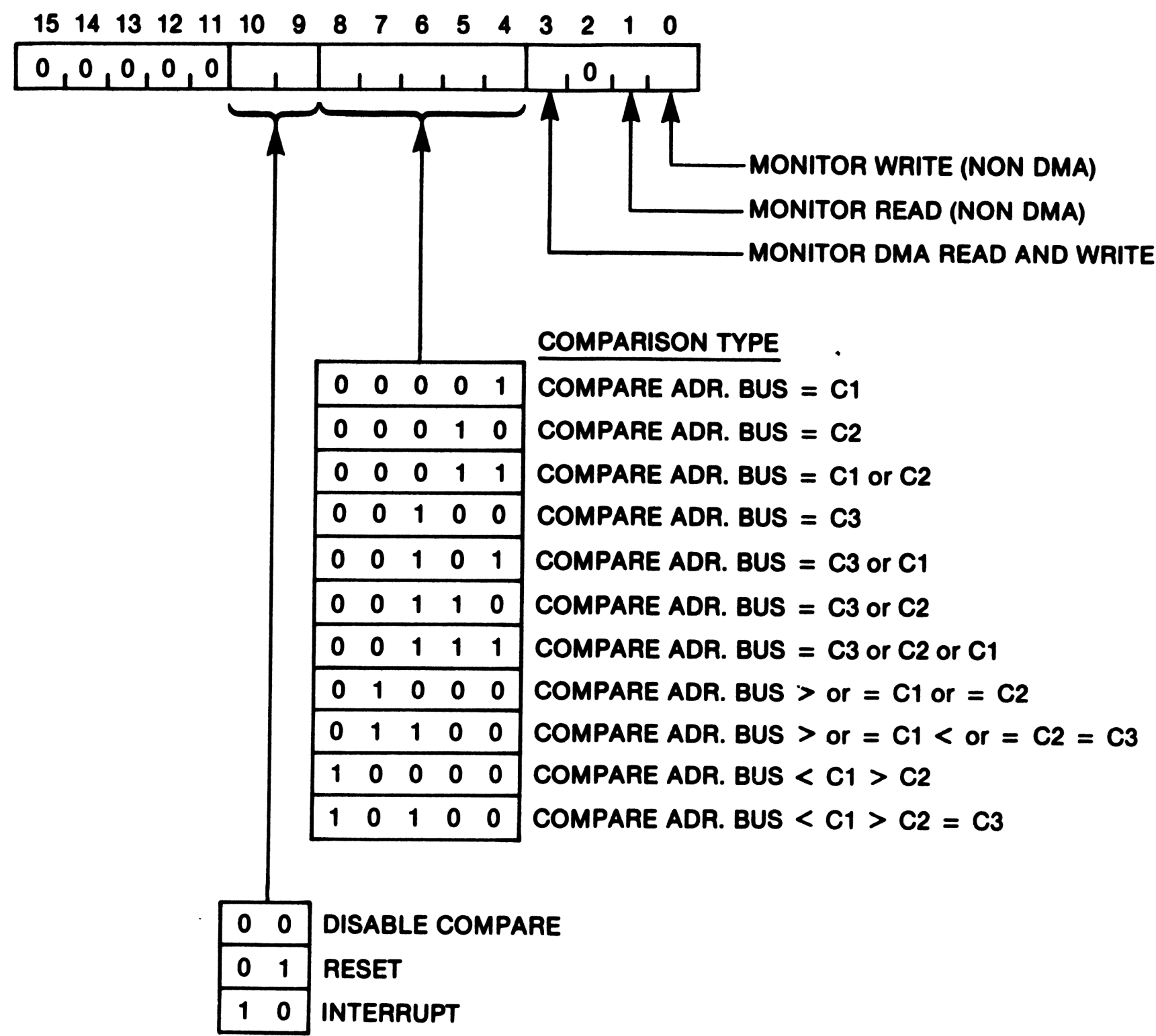


Figure 3-1. Mode Register Bit Configuration

3.2.3 Input Instruction

The INA or INX instruction loads information from the Bus Monitor memory into the A or X register. The first INA or INX instruction halts the monitoring operation of the Bus Monitor and places the Run/Stop latch in a Stop. Four function codes are used in conjunction with the input instruction.

An input instruction with a function code 0 places the 16 least significant bits of a word in the Bus Monitor memory into the specified register. The 16 least significant bits of each Bus Monitor word form a complete system memory address. Function code 0 also increments the Bus Monitor memory address.

To input from the 16 least significant bits of a word in the Bus Monitor memory to the A or X register, use the function code 0 in the form of

	INA	DEVAD+0
or	INX	DEVAD+0

An input instruction with a function code 1 places the 8 most significant bits of a word in the Bus Monitor memory into the specified register. The 8 most significant bits of each Bus Monitor word consist of the five MAXI-BUS® interface control signals and the three external inputs. Function code 1 also increments the Bus Monitor memory address.

To input from the 8 most significant bits of a word in the Bus Monitor memory to the A or X register use the function code 1 in the form of

	INA	DEVAD+1
or	INX	DEVAD+1

An input instruction with a function code 2 places the 16 least significant bits of a word in the Bus Monitor memory into the specified register. The 16 least significant bits of each Bus Monitor form a complete System memory address. Function code 2 does not increment the Bus Monitor memory.

To input from the 16 least significant bits of a word in the Bus Monitor memory to the A or X register, use the function code 2 in the form of

	INA	DEVAD+2
or	INX	DEVAD+2

An input instruction with a function code 3 places the 8 most significant bits of a word in the Bus Monitor memory into the specified register. The 8 most significant bits of each Bus Monitor word consist of the five control signals from the C-bus and the three external inputs. Function code 3 does not increment the Bus Monitor memory address.

To input from the 8 most significant bits of a word in the Bus Monitor memory to the A or X register, use the function code 3 in the form of

	INA	DEVAD+3
or	INX	DEVAD+3

To fully transfer the contents of a word in the Bus Monitor memory to main computer memory requires two separate input instructions. The first input instruction must use a function code that does not increment the Bus Monitor memory address. The second input instruction would use the companion function code that does increment the Bus Monitor memory address. When fully transferred into the main computer memory, the contents of the Bus Monitor memory occupies 160 words of memory.

3.2.4 Programming Examples

For an example of how to initialize the Bus Monitor and to access the contents of the Bus Monitor memory, a sample program is provided in Figure 3-2.

There are two subroutines that can easily be inserted into the main body of a program. The values of the comparators should be established prior to the loading of the program.

3.3 INPUT/OUTPUT COMMAND DESCRIPTION (NAKED MINI® 4)

The I/O command descriptions are presented in assembly language format for easy use. The label (if used) mnemonic and operand with the appropriate function code appears with command. The commands used to communicate with the Bus Monitor are the following:

SELP	Select and Present
OUT	OUTPUT From Register
IN	INPUT To Register

```

DEVAD EQU      :16X3      BUS MONITOR DEVICE ADDRESS
*
* INITIALIZE BUS MONITOR
*
INIT   ENT      $
      DIN              DISABLE INTERRUPTS
      SEA      DEVAD+4  INITIALIZE BUS MONITOR
      LDA      C1
      OTA      DEVAD+1  LOAD BUS MONITOR A REGISTER
      LDA      C2
      OTA      DEVAD+2  LOAD BUS MONITOR B REGISTER
      LDA      C3
      OTA      DEVAD+3  LOAD BUS MONITOR C REGISTER
      LDA      MODE
      OTA      DEVAD+4  LOAD BUS MONITOR MODE REGISTER
      FIN
      SEA      DEVAD+0  START BUS MONITOR
      RTN      INIT     DONE

*
C1     DATA    0        C1 VALUE (BUS MONITOR A REGISTER)
C2     DATA    0        C2 VALUE (BUS MONITOR B REGISTER)
C3     DATA    0        C3 VALUE (BUS MONITOR C REGISTER)
MODE   DATA    0        BUS MONITOR MODE REGISTER
*
* READ BUS MONITOR FIFO INTO MEMORY
*
READ   ENT      $
      LDX      =BUFFER  START ADDRESS OF BUFFER
      LAM      80
      STA      COUNT    INITIALIZE COUNTER
LOOP   EQU      $
      INA      DEVAD+3  GET HIGH ORDER 8 BITS FROM BUS MONITOR
      STA      @0       SAVE IN BUFFER
      INA      DEVAD+0  GET LOW ORDER 16 BITS FROM BUS MONITOR
      STA      @1       SAVE IN BUFFER
      AXI      2        BUMP BUFFER POINTER
      IMS      COUNT    BUMP LOOP COUNTER
      JMP      LOOP     CONTINUE UNTIL DONE
      RTN      READ     DONE

*
COUNT DATA    0        LOOP COUNTER
      LPOOL

BUFFER EQU      $        BUFFER TO HOLD BUS MONITOR FIFO CONTENTS
      RES      160,0     HOLDS 80 24-BIT WORDS
      END

```

Figure 3-2. Programming Example

3.3.1 Select and Present Instruction

The Select and Present instruction is used to initialize the Bus Monitor, start monitoring, and stop monitoring. Three function codes are used with the Select and Present instruction. The register specification in the following instructions serves only to maintain syntactically correct operand structures. The registers contents are ignored by the Bus Monitor.

The Select and Present initialize instruction is used by software to clear the mode register and the interrupt logic, and to set the RUN/STOP latch to STOP.

To Select and Present initialize, use the function code 4 in the form

SELP R,DEVAD+4 (R=A,X,Q or Y register)

The Select and Present start instruction is used to initiate monitoring, set the RUN/STOP latch to RUN, and load the preset value into the skip counter.

To Select and Present start, use the function code 0 in the form

SELP R,DEVAD+0 (R=A,X,Q or Y register)

The Select and Present instruction to stop monitoring sets the RUN/STOP latch to STOP.

To Select and Present stop, use the function code 1 in the form

SELP R,DEVAD+1 (R=A,X,Q or Y register)

3.3.2 Output Instruction

The output instruction loads the contents of the specified register into one of the three compare registers or the mode register. There are four function codes used to load the specified registers on the Bus Monitor.

The function code 1 is used to load the contents of the specified register into the A compare register. The initialize instruction does not change the contents of the register.

To load the Bus Monitor A register, use function code 1 in the form

OUT R,DEVAD+1 (R=A,X,Q, or Y Register)

The function code 2 is used to load the contents of a specified register into the B compare register. The initialize does not change the contents of the register.

To load the Bus Monitor B register, use the function code 2 in the form

OUT R,DEVAD+2 (R=A,X,Q, or Y Register)

The function code 3 is used to load the contents of a specified register into the C compare register. Initialize does not change the contents of the register.

To load the Bus Monitor C register, use function code 3 in the form

OUT R,DEVAD+3 (R=A,X,Q, or Y Register)

The function code 4 is used to load the contents of a specified register into the mode register. Initialize does not change the contents of the register. The mode bits are shown in Table 3-1.

To load the Bus Monitor mode register, use function code 4 in the form

OUT R,DEVAD+4 (R=A,X,Q, or Y Register)

3.3.3 Input Instruction

The input instruction places information from the Bus Monitor memory into the specified register. The first input instruction halts the monitoring operation of the Bus Monitor and places the Run/Stop latch in a Stop. There are four function codes used in conjunction with the input instruction.

An input instruction with a function code 0 loads the 16 least significant bits of the Bus Monitor into the specified register. The 16 least significant bits of each Bus Monitor memory word form of a complete system memory address. Function code 0 also increments the Bus Monitor memory address.

To input from the 16 least significant bits of a word in the Bus Monitor memory into the specified register, use a function code 0 in the form of

IN DEVAD+0,R (R=A, X, Q, or Y registers)

An input instruction with a function code 1 loads the 8 most significant bits of a word in the Bus Monitor memory word being accessed by the CPU. The 8 most significant bits of the Bus Monitor memory word consist of the five MAXI-BUS® interface control signals and the three external inputs. Function code 1 also increments the Bus Monitor memory address.

To place the 8 most significant bits of a word in the Bus Monitor memory in the specified register, use the function code 1 in the form of

IN DEVAD+1,R (R=A, X, Q, or Y register)

An input instruction with a function code 2 loads the 16 least significant bits of a word in the Bus Monitor memory into a specified register. The 16 least significant bits form of a complete system memory address. Function code 2 instruction does not increment the Bus Monitor memory address.

To load the 16 least significant bits of a word in the Bus Monitor memory to the specified register use the function code 2 in the form of

IN DEVAD+2,R (R=A, X, Q, or Y register)

An input instruction with a function code 3 loads the 8 most significant bits of a word in the Bus Monitor memory into a specified register. The 8 most significant bits consist of the five MAXI-BUS® interface control signals and the three external inputs. Function code 3 does not increment the Bus Monitor memory address.

To load the 8 most significant bits of the Bus Monitor memory to the specified register, use the function code 3 in the form of

IN DEVAD+3,R (R=A, X, Q, or Y register)

To fully transfer the contents of a word in the Bus Monitor memory to the main computer memory, two separate input instructions are required. The first input instruction must use a function code that does not increment the Bus Monitor memory address. The second input instruction would use the companion function code that does increment the Bus Monitor memory address. When fully transferred into the main computer memory, the content of the Bus Monitor memory occupies 160 words of memory.

3.3.4 Sample Program

Figure 3-3 illustrates two subroutines that demonstrate the operation of the Bus Monitor and can be easily inserted into the main body of the program. The values of the comparators should be established prior to the loading of the program.

```

DEVAD      EQU      :1623      BUS MONITOR DEVICE ADDRESS
*
* INITIALIZE BUS MONITOR
*
INIT        EQU      $
          RBIT      8,S          DISABLE INTERRUPTS
          SELP      A,DEVAD+4    INITIALIZE BUS MONITOR
          COPY      C1,A
          OUT       A,DEVAD+1    LOAD BUS MONITOR A REGISTER
          COPY      C2,A
          OUT       A,DEVAD+2    LOAD BUS MONITOR B REGISTER
          COPY      C3,A
          OUT       A,DEVAD+3    LOAD BUS MONITOR C REGISTER
          COPY      MODE,A
          OUT       A,DEVAD+4    LOAD BUS MONITOR MODE REGISTER
          SBIT      8,S          ENABLE INTERRUPTS
          SELP      A,DEVAD+0    START BUS MONITOR
          RSK
          DONE

*
C1          WORD     0          C1 VALUE (BUS MONITOR A REGISTER)
C2          WORD     0          C2 VALUE (BUS MONITOR B REGISTER)
C3          WORD     0          C3 VALUE (BUS MONITOR C REGISTER)
MODE        WORD     0          BUS MONITOR MODE REGISTER
*
* READ BUS MONITOR FIFO INTO MEMORY
*
READ        EQU      $
          COPY      =BUFFER,Y    START ADDRESS OF BUFFER
          COPY      =0,X          INITIALIZE BUFFER INDEX
LOOP        EQU      $
          IN        DEVAD+3,A     GET HIGH ORDER 8 BITS FROM BUS MONITOR
          COPY      A,0(X,Y)      SAVE IN BUFFER
          IN        DEVAD+0,A     GET LOW ORDER 16 BITS FROM BUS MONITOR
          COPY      A,1(X,Y)      SAVE IN BUFFER
          ADD       =2,X          BUMP BUFFER INDEX
          CSK       X,=80         CHECK FOR END OF BUFFER
          JMP       LOOP          CONTINUE IF NOT DONE
          NOP
          RSK
          DONT

*
LPOOL

BUFFER      EQU      $
          RES       160,0
          END

```

Figure 3-3. Programming Example

SECTION 4

INSTALLATION

This section describes the installation considerations unique to the Bus Monitor. For a description of standard installation procedures, refer to the applicable computer handbook.

4.1 SYSTEM CONFIGURATION

The Bus Monitor is a single half-card device that can be inserted into any half-card slot on the Motherboard. The interrupt priority of the Bus Monitor is established by its placement in the priority chain.

Care should be exercised to assure that the priority chains between the Bus Monitor and the CPU are not broken. All cards located between the CPU and the Bus Monitor must provide propagation of the priority chains and in turn, the Bus Monitor propagates all MAXI-BUS® interface priority chains. No open slots can exist between the Bus Monitor and the CPU or the chain will be broken.

4.2 ADDRESS ASSIGNMENTS

The Bus Monitor must be assigned a device address and interrupt vector address before it is integrated physically into the system.

4.2.1 Device Address Assignments

The Bus Monitor can be assigned any device address from :01 through :1F. When assigning a device address, care must be taken to avoid assigning a device address already in use or a device address dedicated to specific peripheral or device. Refer to the applicable computer handbook for a listing of standard device address assignments and restrictions.

The Bus Monitor uses the standard 5-bit device address format used by other Computer Automation, Inc., I/O controllers. Because the I/O distributor uses a 4-bit base device address, it is necessary to check the absolute value of the Bus Monitor device address to be sure a conflict does not occur with other I/O controller device addresses. The field value of the device address is treated by software as an absolute 5-bit value.

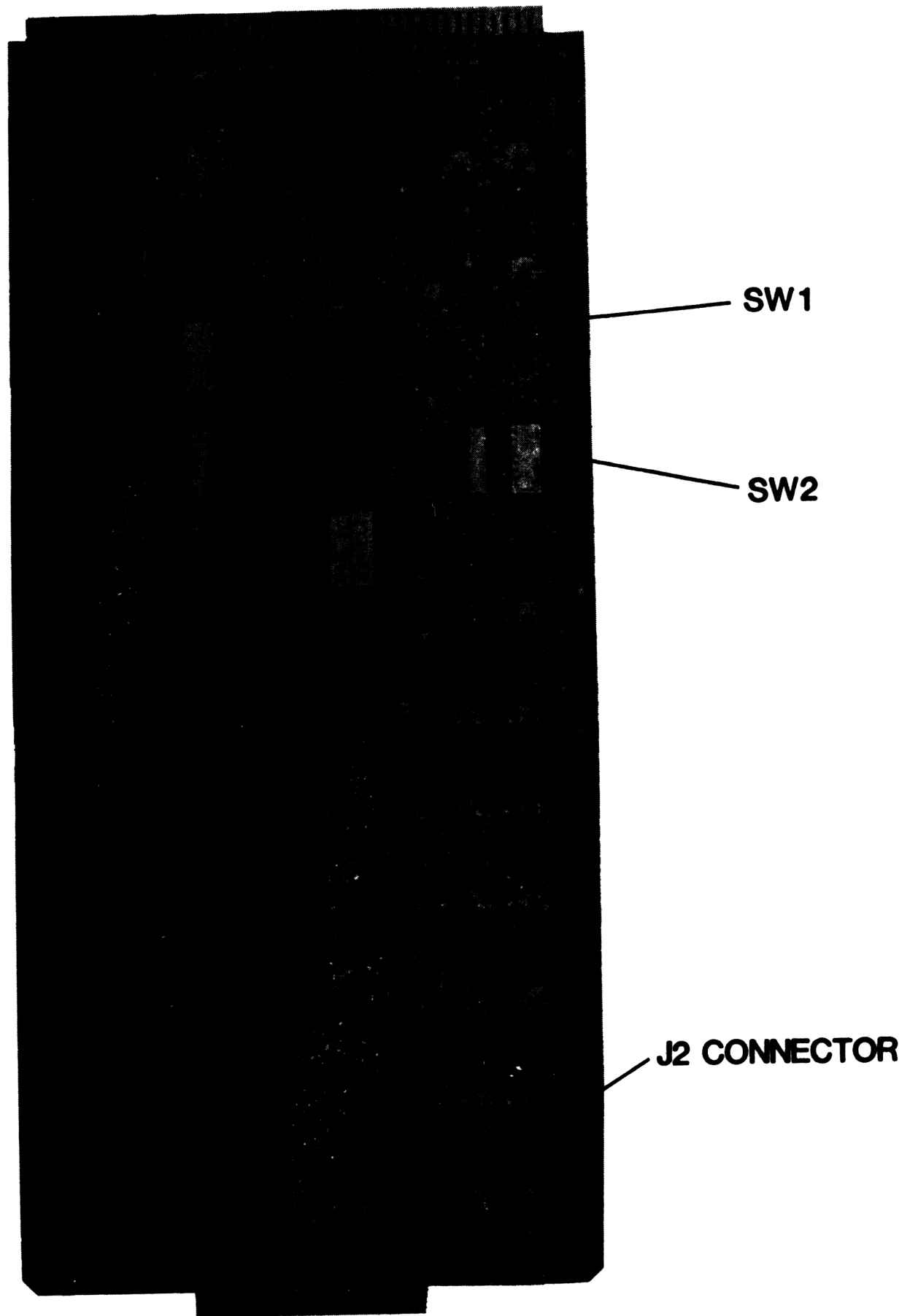


Figure 4-1. Photograph of the Bus Monitor

The device address bit assignments for switch 1 (SW1), along with the device address switch selections corresponding to the recommended device address, are shown in Figure 4-2. The switch settings for all 31 permissible device addresses are listed in Table 4-1. The table is coded for a device address bit value of 0= OFF and 1= ON. The recommended Bus Monitor device address for compatibility with Computer Automation, Inc., software is :16 and is shown shaded in Table 4-1.

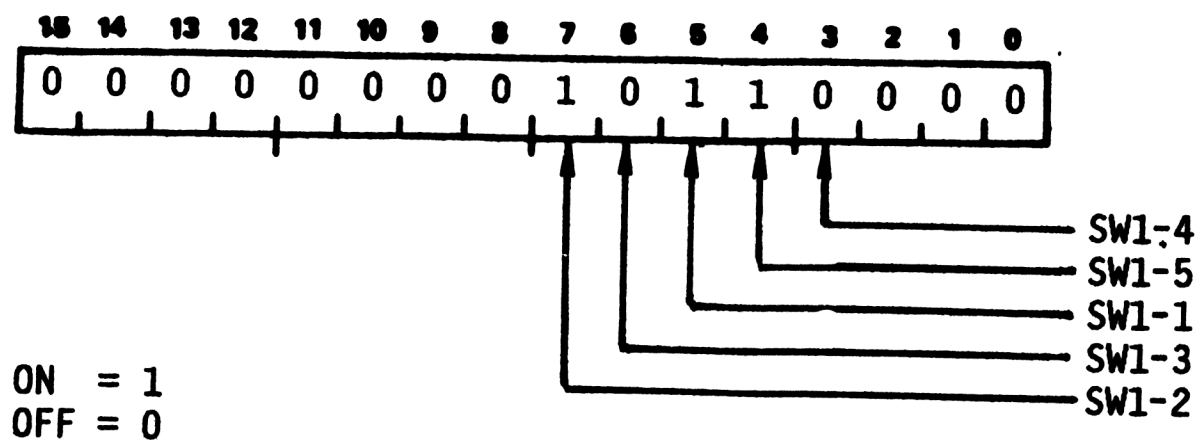


Figure 4-2. Device Address Bit Assignments

Table 4-1. Device Address Switch Settings

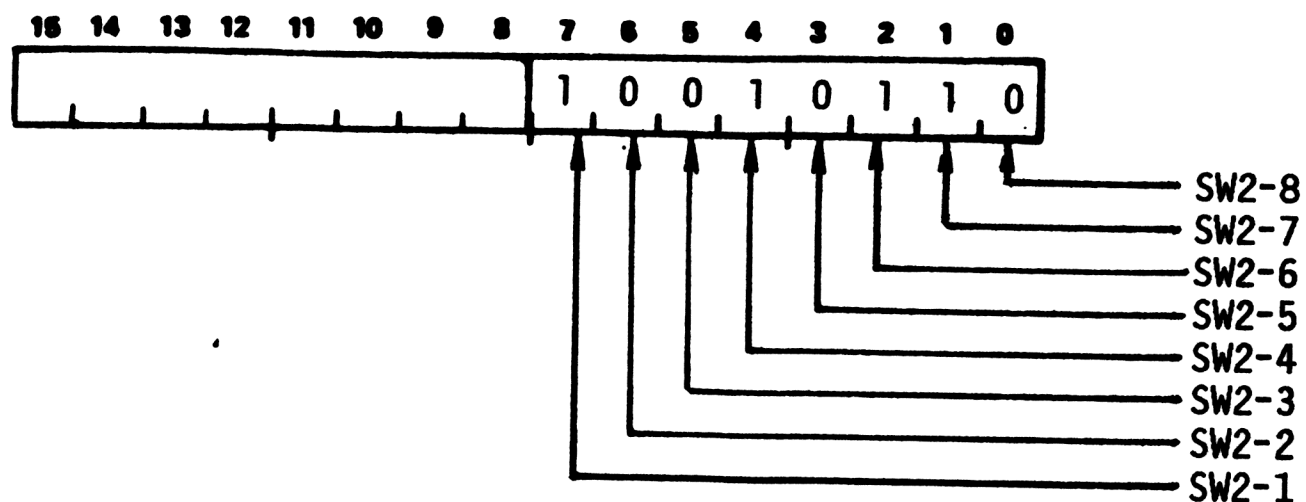
DEVICE ADDRESS	SW 1 Switch Elements					DEVICE ADDRESS	SW 1 Switch Elements				
	-2	-3	-1	-5	-4		-2	-3	-1	-5	-4
:01	0	0	0	0	1	:10	1	0	0	0	0
:02	0	0	0	1	0	:11	1	0	0	0	1
:03	0	0	0	1	1	:12	1	0	0	1	0
:04	0	0	1	0	0	:13	1	0	0	1	1
:05	0	0	1	0	1	:14	1	0	1	0	0
:06	0	0	1	1	0	:15	1	0	1	0	1
:07	0	0	1	1	1	:16	1	0	1	1	0
:08	0	1	0	0	0	:17	1	0	1	1	1
:09	0	1	0	0	1	:18	1	1	0	0	0
:0A	0	1	0	1	0	:19	1	1	0	0	1
:0B	0	1	0	1	1	:1A	1	1	0	1	0
:0C	0	1	1	0	0	:1B	1	1	0	1	1
:0D	0	1	1	0	1	:1C	1	1	1	0	0
:0E	0	1	1	1	0	:1D	1	1	1	0	1
:0F	0	1	1	1	1	:1E	1	1	1	1	0
						:1F	1	1	1	1	1
LEGEND: Switch elements set to: ON = 1 OFF = 0											

4.2.2 Interrupt Vector Address

The Bus Monitor can be assigned any interrupt vector address from :0 to :FF.

Care must be exercised when assigning the interrupt vector address to avoid assigning an interrupt vector address already in use or dedicated to a specific peripheral or device. The recommended standard interrupt vector address assignments are listed in the applicable computer reference manual.

The recommended vector address location for compatibility with Computer Automation, Inc., software is :96. Figure 4-3 illustrates the format of the interrupt vector address switch SW2. The number shown is the binary form of :96. Refer to Figure 4-1 for the location of switch SW2.



1 = OFF
0 = ON

Figure 4-3. Interrupt Vector Address Bit Assignment

4.3 SKIP COUNTER SWITCH SETTING

The skip counter is used to count the number of read memory operations and compare the number of operations to a preselected count established by the user. To preselect the count the Bus Monitor board must be removed from the CPU chassis. Switch SW1 establishes the skip count as listed in Table 4-2. The location of switch SW1 on the Bus Monitor is illustrated. Refer to Figure 4-1.

Table 4-2. Skip Counter Select Switch Settings

SW1-6	SW1-7	SW1-8	Skip Count
OFF	OFF	OFF	1
OFF	OFF	ON	3
OFF	ON	OFF	5
OFF	ON	ON	7
ON	OFF	OFF	9
ON	OFF	ON	11
ON	ON	OFF	13
ON	ON	ON	15

4.4 J-2 CONNECTOR

The J-2 connector is a standard 36 pin edge connector, used with a 36 pin CDC connector part number VPB01B18A00AIE or the equivalent. The user can connect an oscilliscope to the connector for synchronization. Table 4-3 lists the pin numbers and the signals available at the pins.

Table 4-3. J-2 Pin Mnemonics

PIN	SIGNAL DESCRIPTION
1	EX0 EX1 EX2 External Inputs
2	
3	
4	Interrupt/Reset Output Synchronizing Comparator 1 Synchronizing Output Comparator 2 Synchronizing Output Comparator 3 Synchronizing Output
5	
6	
7	
8 through 18	Not used
A through V	Ground

4.5 TIMING CONSIDERATIONS

The Bus Monitor performs functions defined by the operational variables in conjunction with the signal Memory Start (MST), a signal on the MAXI-BUS® interface. Since the primary function of the Bus Monitor is to monitor memory access, the Bus Monitor's execution timing must coincide with this time to allow the Bus Monitor to perform its functions. Figure 4-4 displays the timing consideration unique to the Bus Monitor.

4.5.1 External Inputs

The Bus Monitor provides three external inputs which can be stored in the Bus Monitor's memory. Any signal that is stable 75 nanoseconds prior to the beginning of MST can be attached to these inputs. There is an additional value of 50 nanoseconds after MST until data is actually clocked into the Bus Monitor memory.

The external input can also be used to monitor NAKED MINI® 4 console READs or WRITEs by sampling the console connector's IF- signal (pin J1-37 on the motherboard) at Bus Monitor external connector EX0 through EX2 (J2-1 through J2-3).

4.5.2 Comparison and Interrupt or Reset Considerations

The comparator synchronizing outputs are enabled 50 nanoseconds after the Bus Monitor has sampled MST.

The reset or interrupt signal is enabled 250 nanoseconds after the 50 nanosecond delay; this synchronizing output states that the Bus Monitor has found a comparison and a reset or an interrupt is to be performed.

The actual command signals that state Reset or Interrupt, defined by the operational variables, are enabled 250 nanoseconds after the 50 nanosecond delay.

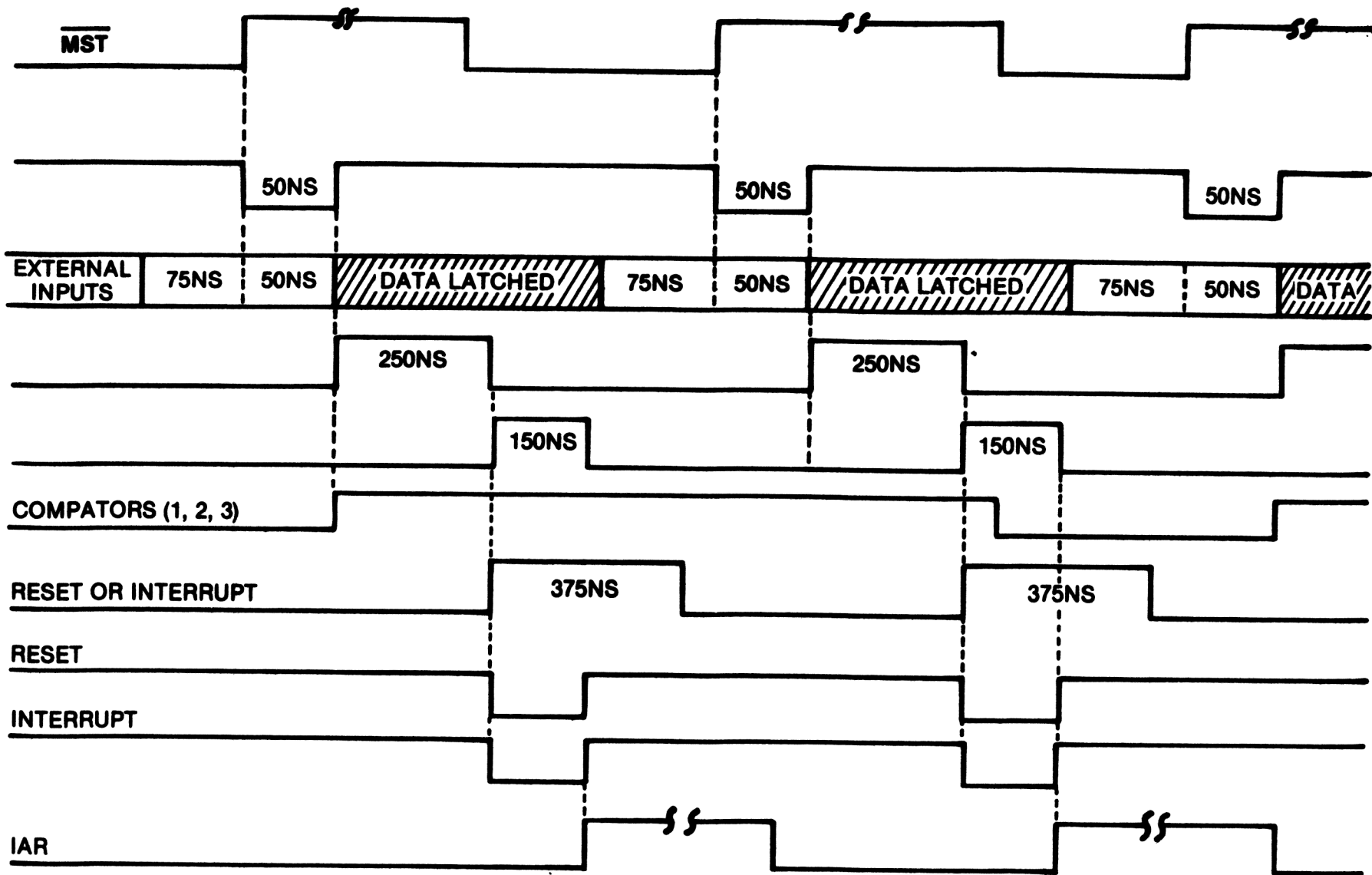


Figure 4-4. Timing Considerations for the Bus Monitor