I/O DISTRIBUTORS
USER'S MANUAL

53629-71

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ComputerAutomation®

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PREFACE

The I/O Distributors User's Manual describes the I/O Distributor models available for use with LSI Family and NAKED MINI® 4 Family computers. The I/O Distributors function as a part of the MAXI-BUS® Interface.

The manual includes functional, programming and installation information. The functional section describes both standard and DMA I/O Distributors. The programming section describes, separately, the LSI Family and the NAKED MINI® 4 Family I/O commands used to communicate with the I/O Distributor and attached Intelligent Cable. The installation section describes the basic system configuration, installation procedures, and the methods of establishing operating parameters. These include device and interrupt address assignment, baud rate, parity bit standardization and 32-64K addressability.

The I/O Distributors User's Manual assumes a familiarity with the applicable Computer Automation, Inc., computer reference manual and MAXI-BUS® Interface. The information in this manual corresponds to the following I/O Distributors:

Marketing Number	Engineering Number	Revisions
14629-14	73-53629	A, B, and C
14629-18	73-53629	A, B, and C
14674-01	73-53674	A, B, and C
53701-01	73-53701	A, B, and C
53701-02	73-53701	A and B

Descriptions of the 14629 I/O Distributors are supplied for informational purposes only. I/O Distributors 53674 and 53701 are production models. The revision levels given are the latest production levels as of the writing of this manual.

Related Documents:

20400-91 LSI-2 Series Minicomputer Handbook
10005-91 LSI-3/05 Series Millicomputer Handbook
20990-91 LSI-4/10 Computer Reference Manual
20991-91 LSI-4/30 Computer Reference Manual
20945-91 LSI-4/90 Computer Reference Manual
53629-81 Intelligent Cable User's Manual
53722-91 32-Bit General-Purpose Intelligent Cable User's Manual
53735-91 BiSync Intelligent Cable Reference Manual

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SECTION 1

GENERAL DESCRIPTION

The I/O Distributor is the central component in the Distributed I/O System. The Distributed I/O System provides multiport interface control designed to replace conventional interface controllers. The various model I/O Distributors are grouped into two operational classes: the standard models that use interrupt initiated Automatic I/O to bring about data transfer, and the models that transfer data by Direct Memory Access (DMA). Either type I/O Distributor can also transfer data via the CPU registers under direct program control.

The standard I/O Distributors come in four and eight channel versions that can operate with any mix of Intelligent Cables. DMA I/O Distributors are available in four-channel versions only, operating with any mix of Intelligent Cables. The Intelligent Cables are described in the Intelligent Cable user's manuals.

1.1 SYSTEM CONCEPT

An I/O Distributor, complete with up to four or eight Intelligent Cables, can replace the same number of independent interface controllers. The I/O Distributors observe the discipline required to communicate over the MAXI-BUS® Interface. Each I/O Distributor also develops a system clock for internal use and for use by all attached Intelligent Cables, and supplies operating power for most Intelligent Cables. The Intelligent Cables observe the discipline necessary to communicate with peripherals. The physical division of the interface controller logic into seperate units allows the I/O Distributor logic to be used on a time-shared basis. The I/O Distributor thus expands the capabilities of a port to the MAXI-BUS® interface. The block diagram for the Distributed I/O System is shown in Figure 1-1.

1.1.1 Standard I/O Distributor

The standard I/O Distributor multiplexes the Intelligent Cables to a single port on the MAXI-BUS® interface. It assigns priorities to the data service and End-of-Block service requests from the Intelligent Cables and then, in priority order, transfers these requests to the MAXI-BUS® in the form of interrupts. The standard I/O Distributor is also responsible for providing the correct interrupt vector address when the Intelligent Cable interrupt request is honored.

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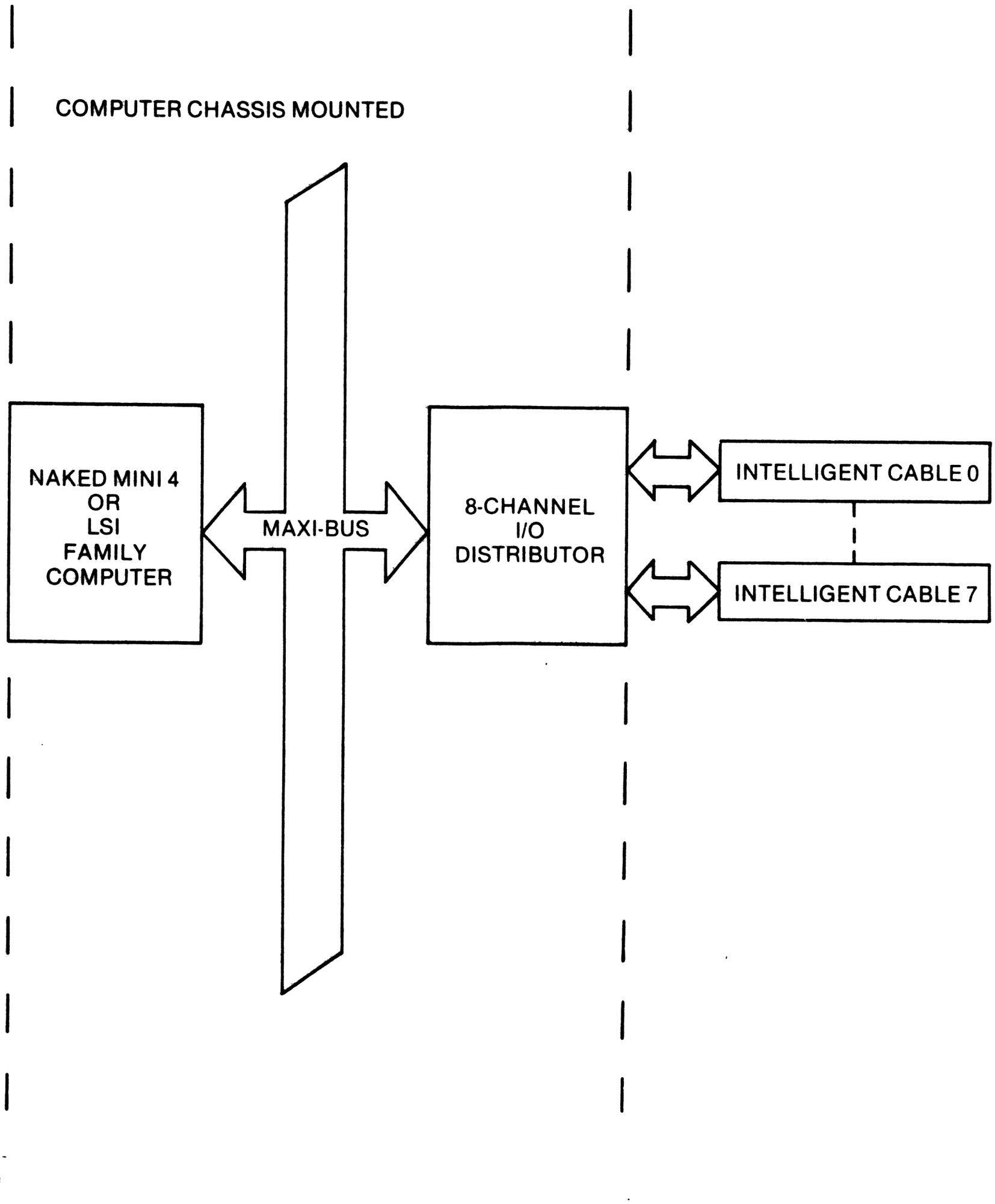


Figure 1-1. Representative Distributed I/O System Block Diagram

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1.1.2 DMA I/O Distributor

The DMA I/O Distributor multiplexes the Intelligent Cables to a single port on the MAXI-BUS® and prioritizes data transfers as in the case of standard I/O Distributors. It differs from the standard I/O Distributor in fetching, loading, and emulating execution of the Automatic I/O instructions internally. Because this is performed by the DMA I/O Distributor, the mainline program is not interrupted and data transfers are made at the memory cycle rate. The End-of-Block service requests from the Intelligent Cables are assigned an interrupt priority and then, in priority order, the DMA I/O Distributor transfers these requests to the computer as an interrupt when there are no pending data service requests.

A micro-diagnostic is provided for test purposes as part of the DMA I/O Distributor processing capabilities. The micro-diagnostic tests the data loop for any attached Intelligent Cable. The micro-diagnostic is selected and initiated by software command from the computer. Successful completion is indicated by an interrupt to the End-of-Block subroutine.

1.2 ENVIRONMENTAL

All I/O Distributors operate at an ambient temperature of from 0 to 50 degrees Celsius at 5 to 90 percent relative humidity (non-condensing).

1.3 POWER REQUIREMENTS

All I/O Distributors receive DC power from the +5V line of the computer power supply. The current usages are as follows:

	Average	Maximum
I/O Distributor 14629-14 (All revisions)	1.54A	1.79A
I/O Distributor 14629-18 " "	2.06A	2.31A
I/O Distributor 14674-01 " "	3.02A	3.81A
I/O Distributor 53701-02 " "	1.51A	1.83A
I/O Distributor 53701-01 " "	1.99A	2.38A

Refer to the appropriate computer handbook for the various power supply capacities. Be sure the total power demand does not exceed the rated power supply capacity.

1.4 BANDWIDTH

Tables 1-1 and 1-2 contain listings of the maximum transfer rate bandwidths for various combinations of processors, memories, and I/O Distributors. The listed maximums apply to a single Intelligent Cable transferring data when all other peripherals are in Idle and the software in a minimum wait loop. Table 1-1 gives the values for LSI Family computers; Table 1-2 gives the values for NAKED MINI® 4 Family computers.

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Table 1-1. Maximum Bandwidth in Kilobytes (LSI Family computers)

		MEMORY		
CPU TYPE	I/O DISTRIBUTOR TYPE	CORE 1600	CORE 1200	CORE 980
LSI-2/60	Standard	60	80	86
LSI-2/20	Standard	60	80	86
LSI-2/10	Standard	30	40	43
LSI-3/05	Standard	32	32	32
LSI Family	DMA	198	215	225

Table 1-2. Maximum Bandwidth in Kilobytes (NAKED MINI® 4 Family computers)

		MEMORY				
CPU TYPE	I/O DISTRIBUTOR	550 RAM	700 RAM	850 CORE	1200 CORE	4/10 ON BOARD RAM
4/10	Standard	30	29	30	29	30
4/30	Standard	78	74	76	71	
4/90	Standard	89	87	85	79	
NAKED MINI® 4	DMA	227	221	223	215	227

NOTE

The maximum bandwidth figures given in these tables do not allow for an interrupt recognition latency period or for device location in the priority chain.

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SECTION 2

FUNCTIONAL DESCRIPTION

The Distributed I/O System is a multi-channel system. The operational sequences of a standard I/O Distributor channel using interrupts to perform data transfers and a DMA I/O Distributor channel using Direct Memory Access to perform data transfers are described in this section. The operational sequences presented are typical of the operation of each type channel. The transfer of data under direct program control is dependent on the software and the Intelligent Cable involved and is not described. Refer to the Intelligent Cable user's manuals.

2.1 SYSTEM OPERATION

The differences in operation between the standard and the DMA I/O Distributors are virtually transparent from a software standpoint. However, a good knowledge of the operational differences will help the programmer design software that will operate on both types of I/O Distributors with maximum efficiency.

2.1.1 Preparation

Before a channel I/O operation can be carried out, the I/O Instruction for data service and the pointer to the End-of-Block subroutine must be loaded at the interrupt vector locations establised in I/O Distributor hardware. The information required in the data service interrupt location is the Automatic I/O op code and channel address, the byte count for the data transfer, and the memory buffer address pointer. The information normally stored in the End-of-Block interrupt location is a jump and store instruction (LSI Family) or a jump and stack instruction (NAKED MINI® 4 Family). These instructions are used to branch the mainline program to the End-of-Block subroutine.

The computer then loads a command word into a register specified by the user. For LSI Family computers, this may be the A or X register. For NAKED MINI® 4 Family computers, the A,Q,X, or Y registers may be used. Command words are not part of the computer instruction set but are constructed by software and used to control channel operations.

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2.1.2 Data Transfer - Standard I/O Distributors

Data transfer using standard I/O Distributors may be accomplished via the CPU registers or by an Automatic I/O sequence, leaving the CPU data registers unaltered. In the former case, a programmed I/O instruction with a function code of 0 is used to input or output data to or from a specified register. In the latter case a programmed I/O instruction with a function code of 1 is used to output a command word, previously loaded in a specified register. The command word contains control codes, retained by the I/O Distributor for use with the addressed channel, and the PICOPROCESSOR operating sequence branch address. The branch address supplied must be to an allowed entry point to the PICOPROCESSOR operating sequence. Under control of the operating sequence, the PICOPROCESSOR establishes the required line conditions for the I/O operation and sends a data service request to the I/O Distributor.

When the request becomes the priority data service request to the I/O Distributor, the request is sent to the computer as an interrupt. The computer completes the instruction in progress and then recognizes the interrupt. A recognition signal is sent to the I/O Distributor. The I/O Distributor responds by providing the address of the first word of the data service interrupt area (interrupt vector). The computer then executes the channel Automatic I/O instruction stored at the data service interrupt location.

The Automatic I/O instruction is part of the computer instruction set (refer to the applicable computer handbook). It is a three-word instruction that has the effect of an I/O subroutine. The following operations are performed as part of the Automatic I/O instruction.

- The first word of the Automatic I/O instruction is used to address the desired peripheral and the I/O Distributor to which the peripheral is connected. The first word opcode specifies an input or output operation.
- The data transfer byte count is updated and, if required, a byte count = 0 signal sent to the PICOPROCESSOR, via the I/O Distributor.
- The memory buffer address pointer is updated and used to address the I/O location in memory.

When the Automatic I/O instruction is completed, the computer continues the mainline program. On the LSI-2 Family, the computer must execute at least one mainline program instruction between interrupts; however, the NAKED MINI® 4 Family is able to service multiple consecutive interrupts. The Distributed I/O channel components drop the respective data service request and interrupt after the data transfer is completed. Additional data service requests are handled in a similar manner. The data transfer sequence chart for standard I/O Distributors is shown in Figure 2-1.

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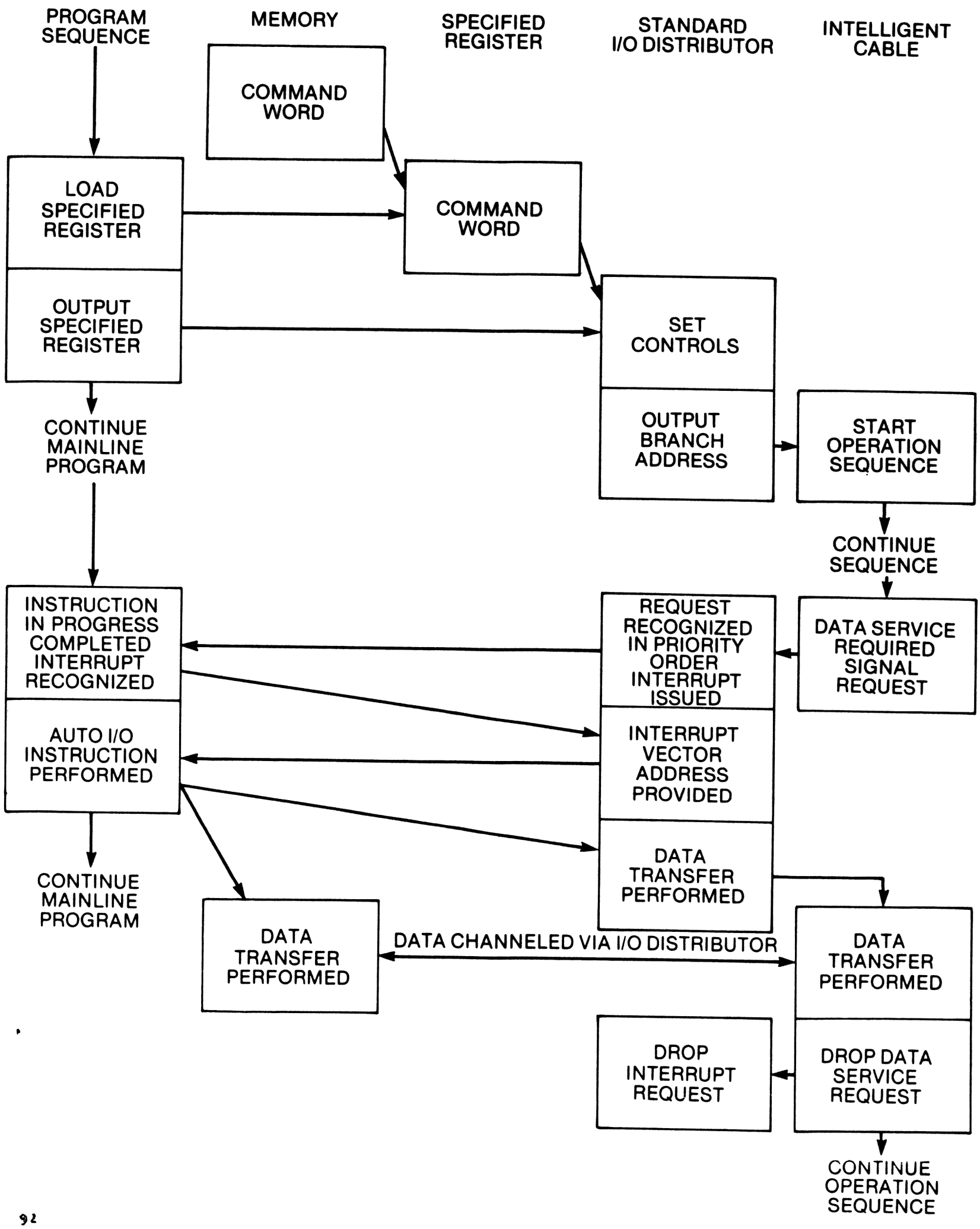


Figure 2-1. Data Transfer Standard I/O Distributors

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2.1.3 Data Transfers-DMA I/O Distributors

Data transfer using DMA I/O Distributors is accomplised using the Automatic I/O instruction word block; programmed I/O (via the CPU registers) is not feasible while the DMA feature is enabled. In addition, data transfer must take place using Automatic I/O byte instructions only; AIN and AOT must not be used when DMA is enabled. To initiate an I/O sequence, a programmed I/O instruction with a function code of 1 is used to output a command word. The DMA I/O Distributor retains the control codes but, unlike the standard I/O Distributor, does not immediately issue the operating sequence branch address to the channel PICOPROCESSOR. The DMA I/O Distributor first checks the command word to determine if DMA is disabled. If it is not, the DMA I/O Distributor carries out a fetch operation, storing the Automatic I/O opcode, byte count, and the memory buffer address pointer in registers for the addressed channel. After the fetch operation is completed, the DMA I/O Distributor outputs the branch address to the PICOPROCESSOR. The remainder of the I/O sequence is identical with that of standard I/O Distributors. The procedures differ functionally because the Automatic I/O instruction is held in the DMA I/O Distributor. The data transfer sequence chart for DMA I/O Distributors operating with DMA enabled is shown in Figure 2-2.

If DMA is disabled, the branch address and branch control signal are output to the PICOPROSSOR. The PICOPROCESSOR establishes the required line conditions and sends a data service request to the I/O Distributor. However, since the DMA I/O Distributor cannot generate an interrupt to the CPU in response to a data service request, the request remains pending. Data is transferred between the channel PICOPROCESSOR and the attached peripheral only; no direct data transfer between system memory and the PICOPROCESSOR via the I/O Distributor can take place. Data must be input or output between the CPU and the PICOPROCESSOR using programmed I/O, which transfers data via the CPU registers.

2.1.4 End-of-Block Sequence

Following the data transfer when the byte count goes to zero or when other ending conditions are detected the I/O Distributor signals the PICOPROCESSOR to inhibit any further data service requests. No further response to PICOPROCESSOR operation is required until the PICOPROCESSOR detects ending conditions and firmware steps to an instruction that sends and holds the End-of-Block service request to the I/O Distributor.

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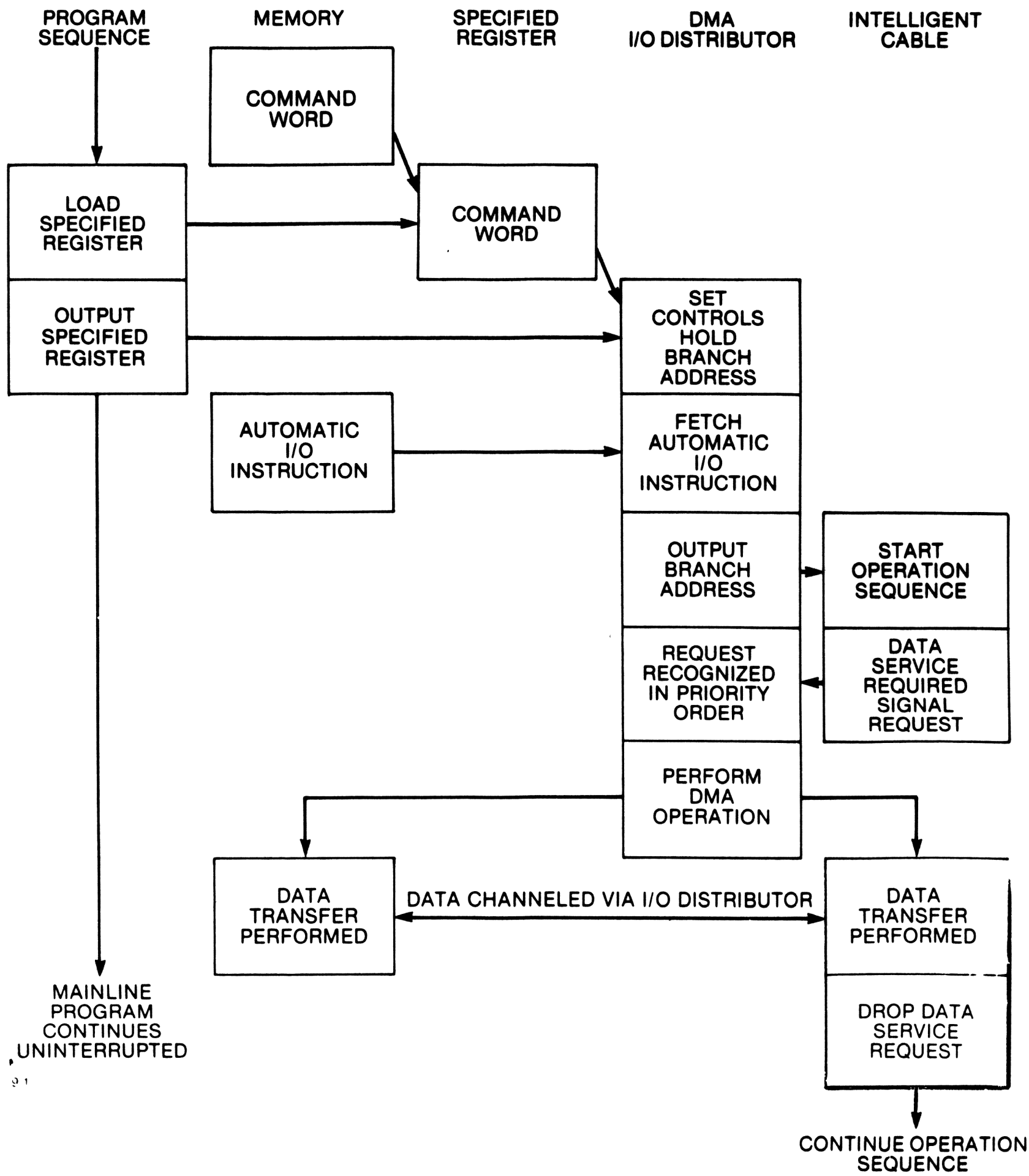


Figure 2-2. Data Transfer, DMA I/O Distributors

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2.1.4.1 Standard I/O Distributor

The End-of-Block service request is considered a lower priority request than a data service request. When the End-of-Block service request does become the priority request to the I/O Distributor, the request is sent to the computer as an interrupt. The computer completes the instruction in progress and then recognizes the interrupt by sending a recognition signal to the I/O Distributor. The I/O Distributor responds by providing the interrupt vector address for the first word of the End-of-Block interrupt area. The computer then executes the instruction stored at the End-of-Block interrupt location. The computer performs only one interrupt vectored instruction before continuing with the P register sequence so the instruction normally stored at the End-of-Block interrupt location is a Jump and Store instruction (LSI Family) or a Jump and Stack instruction (NAKED MINI® 4 Family). This instruction stores, for future use, the interrupted P count and jumps to the address stored in the second word at the End-of-Block interrupt location. The recognition of the interrupt by the computer is acknowledged by the I/O Distributor and the PICOPROCESSOR respectively dropping the interrupt and the End-of-Block service request. The PICOPROCESSOR firmware steps to idle completing the PICOPROCESSOR controlled I/O sequence. This passes full control back to the computer. At the same time, the computer is continuing the End-of-Block subroutine.

The actual instructions involved for the remainder of the End-of-Block subroutine depend on the Intelligent Cable involved and specific software needs. Normally, status is requested as part of the End-of-Block subroutine for a data transfer operation. The input register intruction is used for this operation. The register may be the A or X register for LSI Family computers, or the A,Q,X, or Y register for NAKED MINI® 4 Family computers. The computer can then examine or store for later use the contents of the input register. The End-of-Block sequence for standard I/O Distributors is shown in Figure 2-3.

2.1.4.2 DMA I/O Distributor

When an End-of-Block service request becomes the priority request, the DMA I/O Distributor first determines whether the channel operation was performed with Direct Memory Access disabled. If DMA was disabled, the End-of-Block service request is handled the same as with the standard I/O Distributor.

If Direct Memory Access was enabled during the channel function, the DMA I/O Distributor does not immediately issue the interrupt. The DMA I/O Distributor first restores the final byte count and final memory buffer address pointer to the corresponding locations within the channel data service interrupt location. The DMA I/O Distributor then signals acceptance of the End-of-Block service request to the PICOPROCESSOR. This allows the firmware to step to idle and drop the service request.

The DMA I/O Distributor then issues the interrupt and the remainder of the operation is the same as for the standard I/O Distributor. The End-of-Block routine for DMA I/O Distributors is shown in Figure 2-4.

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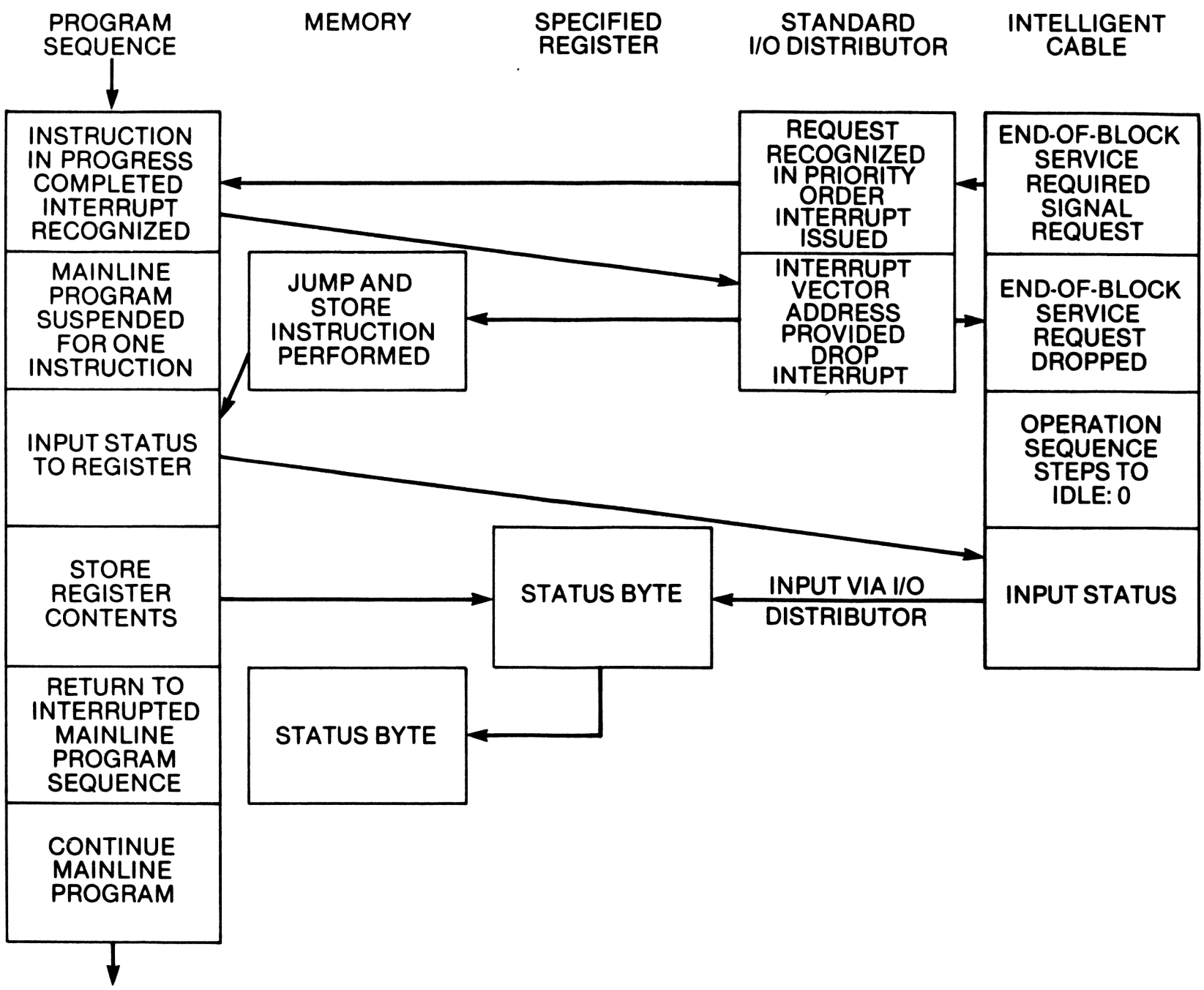


Figure 2-3. End-of-Block Sequence, Standard I/O Distributor

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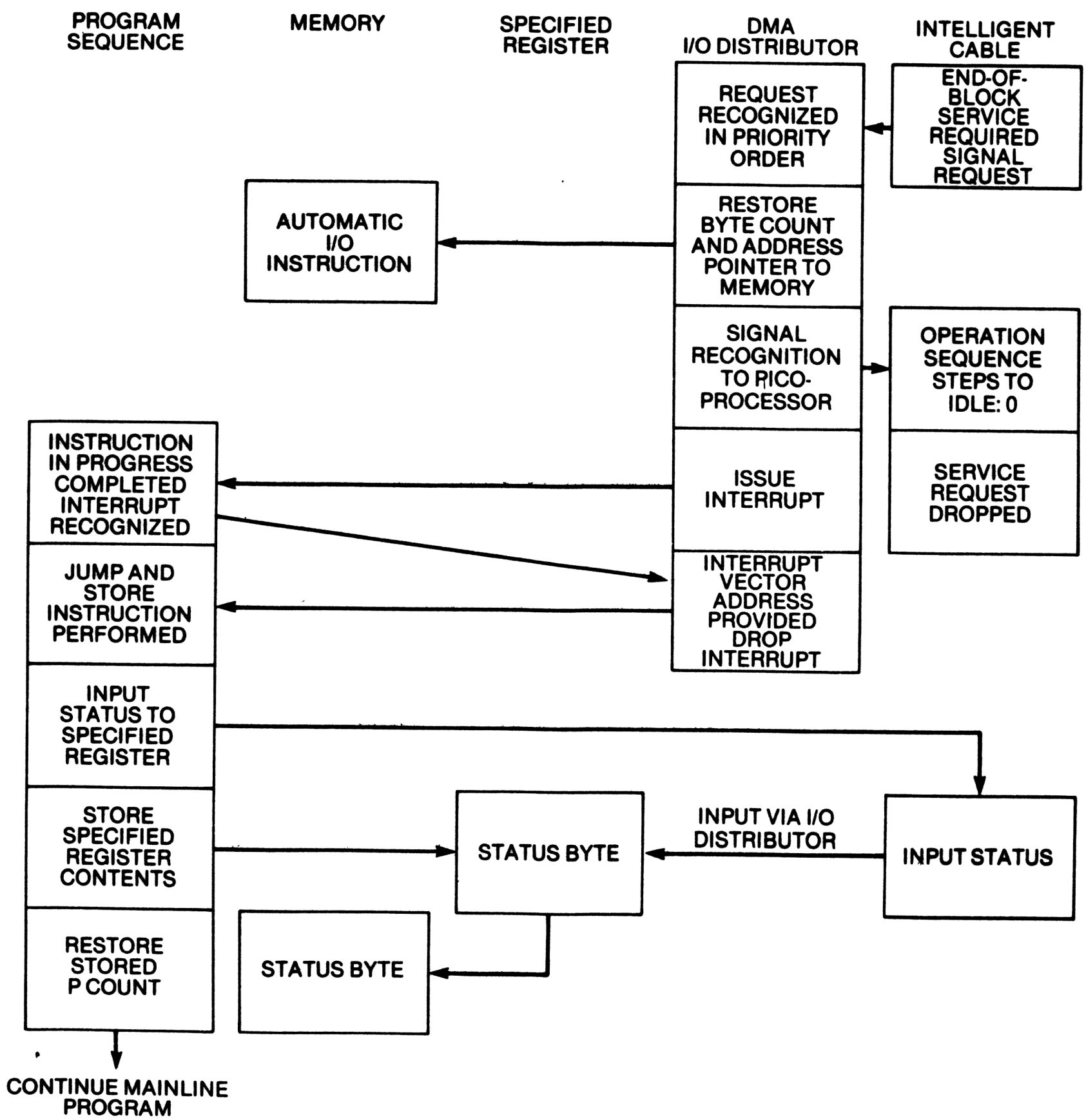


Figure 2-4. End-of-Block Sequence, DMA I/O Distributors

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SECTION 3

PROGRAMMING

The I/O Distributors conform to the general I/O programming philosophy presented in the computer reference manuals. The detailed programming and operating information in the following paragraphs describes separately the LSI and NAKED MINI® 4 Family I/O instructions used to communicate with the I/O Distributor and the Intelligent Cables. In addition to the I/O instructions, special command words are used to directly control the operation of the Intelligent Cables. The use of the command words is also described in this section.

NOTE

The specific instruction set used with a particular Intelligent Cable is described in the appropriate section of the Intelligent Cables User's Manual. The instruction set described is fully decoded by the Cable. Instructions that are not part of the instruction set for that Cable but output with the device address of that Cable, may be partially decoded and the resulting operation is unpredictable.

3.1 DEVICE ADDRESS

Each I/O Distributor is assigned a device address, referred to as the base device address. The base device address is established by a hardware setting on the I/O Distributor board (Section 4). In addition, each Intelligent Cable attached to the I/O Distributor assumes a channel assignment based on the physical channel number where the Cable is attached. These addresses should be established in software as mnemonics to facilitate possible program changes. This can be done using the EQU directive. Using ADBAS as the mnemonic for the base device address, the procedure is as follows.

```
ADBAS     EQU       Base device address determined from system
                    installation information.
```

Assuming the standard base device address :F, then

```
ADBAS     EQU  :F
```

To establish the Cable channel number as a mnemonic, assume the CRT is attached to Channel 4 (standard assignment). Then

```
CRT       EQU  :4
```

The final device address is established as a mnemonic using the EQU directive to combine the base device address and the channel assignment.

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Assuming the CRT is in use, then

```
DADCRT    EQU  ADBAS%3 + CRT%1
```

First the base device address is shifted left three bits; then the channel assignment number is added and the complete combined device address is shifted left one bit to align the device address properly with the I/O instruction format.

When using an assembler that does not recognize the % (shift) sign, the final device address is established using multiplication to accomplish the shifts, as follows:

```
DADCRT    EQU       ADBAS*8+CRT*2
```

The final, combined base address must be included in all I/O instructions.

3.2 INTERRUPT ADDRESS

When using Automatic I/O, the I/O Distributor must supply the CPU with address vectors for the Cable data service and End-of-Block routines. The base interrupt address provides the starting address for the block of data service and End-of-Block routines in system memory assigned to the I/O Distributor (3.8). Like the device address, the base interrupt address is hardware selected on the I/O Distributor board. The interrupt address for a particular Cable is a combination of the base interrupt address and the physical channel number where the Cable is attached. To simplify reprogramming if the base interrupt and/or channel number is changed, the interrupt addresses can be established as conveniently used mnemonics in a manner similar to that for the device address. Using INTBAS as the mnemonic for the base interrupt address, the procedure is as follows.

```
INTBAS    EQU       Base interrupt address determined from system
                    installation information.
```

Assuming the standard base interrupt address :C0, then

```
INTBAS    EQU       :C0
```

The channel interrupt address is established as a mnemonic using the EQU directive to combine the base interrupt address and channel assignment.

Assuming the CRT is in use, then

```
IADCRT    EQU       CRT%3 + INTBAS
```

First the channel number is shifted left three bits to align the channel number properly with the base vector address. Then the base interrupt address is added to the channel number to form the complete channel vector address. When using an assembler that does not recognize the % sign, the channel interrupt address is established using multiplication to accomplish the shifts, as follows:

```
IADCRT          EQU       CRT*8 + INTBAS
```


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3.3 I/O INSTRUCTIONS (LSI FAMILY)

The I/O instruction descriptions are presented in assembly language format for easy use. The label (if used), mnemonic, and operand with an appropriate function code appears for each instruction. The instructions used to communicate with the I/O Distributor and the addressed Intelligent Cable are:

INA	INPUT TO A REGISTER
INX	INPUT TO X REGISTER
OTA	OUTPUT A REGISTER
OTX	OUTPUT X REGISTER
AIB	AUTOMATIC INPUT BYTE
AOB	AUTOMATIC OUTPUT BYTE

3.3.1 Control Usage

Programmed I/O instructions with a function code of 1 are used to output a command word to the Distributed I/O System or request the device-dependent status word from the addressed Intelligent Cable. Function code 1 instructions must be performed in word mode.

3.3.1.1 Command Word Output

The CPU initiates a Distributed I/O System operation using the OTA or OTX instruction to output a command word from the specified register to the I/O Distributor. The required command word must be loaded into the specified register prior to the execution of the OTA or OTX instruction.

To output the contents of the A or X register as control information, use function code 1 in the form

```
OTA       DAD+1

or

OTX       DAD+1
```


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3.3.1.2 Status Determination

The CPU obtains the device dependent status word from the addressed Intelligent Cable using the INA or INX instruction. To store the Intelligent Cable status word in the A or X register, use function code 1 in the form

```
INA       DAD+1

or

INX       DAD+1
```

Status is normally requested as part of the End-of-Block subroutine.

3.3.2 Data Transfer Usage

The I/O instructions with a function code of 0 transfer data between the computer and the addressed Intelligent Cable through the I/O Distributor. The two types of data transfer sequences used with the I/O Distributors are programmed I/O (data transfer via the CPU registers) and Automatic I/O.

3.3.2.1 Programmed I/O

This means of data transfer uses the INA/INX and OTA/OTX instructions to transfer one or more data bytes between the CPU registers and a peripheral device. The data transfers take place either as part of the mainline program or as a subroutine to the main program. All data bytes output are output from the eight least significant bits of the CPU register. All data bytes input from the I/O Distributor are stored in the eight least significant bits of the CPU register.

INA or INX Instructions

The CPU inputs data to a register from the addressed Intelligent Cable through the I/O Distributor using the INA or INX instruction. To store data in the A or X register, use function code 0 in the form

```
INA       DAD+0

or

INX       DAD+0
```


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OTA or OTX Instructions

The CPU outputs data from a register to the addressed Intelligent Cable through the I/O Distributor using the OTA or OTX instruction. To output the contents of the A or X register as data, use function code 0 in the form

```
OTA       DAD+0

or

OTX       DAD+0
```

3.3.2.2 Automatic I/O

Automatic I/O uses the AOB or AIB instructions to transfer data between the CPU and a peripheral device without altering the contents of the CPU registers. The standard I/O Distributors use the AOB or AIB instructions in the conventional manner described in the computer reference manuals, i.e., to accomplish interrupt driven I/O. The DMA I/O Distributors use the AOB or AIB instructions directly to accomplish data transfer between the device and the computer memory.

The programming for the AOB and AIB instructions is the same except for the change of instruction mnemonic. The AOB instruction is shown in the following example.

To transfer data using the Automatic I/O, use function code 0 in the form

```
ABS       IAD       Data Service Interrupt Vector Address
AOB       DAD+0
DATA      $-$       Fill with negative byte count
DATA      $-$       Fill with buffer address -1
```

3.4 END-OF-BLOCK INTERRUPT

Most Intelligent Cables provide an End-of-Block routine request at the completion of a data transfer sequence. The I/O Distributors send the request to the CPU as an interrupt. When the CPU recognizes the interrupt, the I/O Distributor responds with a vector giving the address of a Jump and Store (JST) instruction. The interrupt vector address is located at the data service interrupt address plus four. The CPU then executes the End-of-Block routine stored at a convenient location in memory. The transfer of control to the End-of-Block routine is set up in the form

```
ABS       IAD+4     Channel End-of-Block interrupt vector address.
JST       *$+1
DATA      EOB       Address of End-of-Block routine.
```


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3.5 I/O INSTRUCTIONS (NAKED MINI® 4 FAMILY)

The I/O instruction descriptions are presented in assembly language format for easy use. The label (if used), mnemonic, and operand with appropriate function code appears for each instruction. The commands used to communicate with the I/O Distributor and the addressed Intelligent Cable are:

IN	INPUT TO A SPECIFIED REGISTER
OUT	OUTPUT FROM A SPECIFIED REGISTER
AIB	AUTOMATIC INPUT BYTE
AOB	AUTOMATIC OUTPUT BYTE
UIS	UPDATE INTERRUPT STATUS

3.5.1 Control Information Usage

Programmed I/O instructions with a function code of 1 are used to output a command word to the Distributed I/O System or request the device-dependent status word from the addressed Intelligent Cable. Function code 1 instructions must be performed in word mode.

3.5.1.1 Command Word Output

The CPU initiates a Distributed I/O System operation using the Out instruction to output a command word from the specified register to the I/O Distributor. The required command word must be loaded into the specified register prior to the execution of the OUT instruction.

To output the contents of the specified register as control information, use function code 1 in the form

```
Out     R,DAD+1        (R=A,Q,X, or Y register)
```

One of the A, Q, X, or Y registers must be specified.

3.5.1.2 Status Determination

The CPU obtains the device dependent status word from the addressed Intelligent Cable using the IN instruction. To store the Intelligent Cable status word in the specified register, use a function code of 1 in the form

```
IN      DAD+1,R
```

Status is normally requested as part of the End-of-Block routine.

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3.5.2 Data Transfer Usage

The I/O instructions with a function code of 0 transfer data between the CPU and the addressed Intelligent Cable through the I/O Distributor. The two types of data transfer sequences used with the I/O Distributors are programmed I/O (data transfer via the CPU registers) and Automatic I/O.

3.5.2.1 Programmed I/O

This means of data transfer uses the IN/OUT instructions to transfer a byte of data between the CPU registers and a peripheral device. The data transfers take place either as part of the mainline program or as a subroutine to the main program. All data bytes are output from the eight least significant bits of the CPU register. All data bytes input from the I/O Distributor are stored in the eight least significant bits of the CPU register.

IN Instruction

The CPU inputs data to the specified register from the addressed Intelligent Cable through the I/O Distributor using the IN instruction. To store data in the specified register, use a function code of 0 in the form

```
IN      DAD+0,R      (R=A,X,Q, or Y register)
```

OUT Instruction

The CPU outputs data from the specified register to the addressed Intelligent Cable through the I/O Distributor using the OUT instruction. To output the contents of the specified register as data, use a function code 0 in the form

```
OUT     R,DAD+0      (R=A,X,Q, or Y register)
```

3.5.2.2 Automatic I/O Operation

The Automatic I/O operation uses AOB and AIB instructions with a function code of 0 to transfer data between system memory and a peripheral device without altering the CPU registers. The programming for the AOB and AIB instructions is the same except for the instruction mnemonic. The AOB instruction is shown in the following example.

Automatic I/O instructions are always initiated by an interrupt sequence. To transfer data using Automatic I/O, the Automatic I/O instruction words must be loaded at the interrupt vector address for the specified channel. In the procedure given below, INTCNL is used as a mnemonic to represent any given channel. In practice the mnemonic for the specified channel is used. In addition, the user must specify whether the byte address is in the upper or lower 64K bytes. These operations are accomplished as follows:

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*Enter the word address in the X register.

*Enter the byte count in the Q register.

*Jump to the subroutine by entering:

```
            JST       SETUP
             .
             .
             .
SETUP       ENT
            COPY      INST,A
            COPY      A,INTCNL        SETUP AUTOMATIC I/O INSTRUCTION
            NEG       Q,Q             Q=NEGATIVE BYTE COUNT
SUB         =1,X
            SHIFT     X,LO,1          CONVERT WORD ADDRESS TO BYTE ADDRESS
            JF        OV,$+2          TEST FOR OVERFLOW.  JUMP IF ABSENT
            RBIT      15,Q            RESET BIT 15 OF THE BYTE COUNT
            ADD       =1,X            CONVERT TO BYTE ADDRESS MINUS 1
            COPY      X,INTCNL+2      STUFF IN AUTOMATIC BYTE BLOCK
            COPY      Q,INTCNL+1      SET NEGATIVE BYTE COUNT IN AUTOMATIC
                                      I/O BLOCK
            JMP       *SETUP
             .
             .
             .
INST        AOB       DEVAD+0
```

When using the stack, the following changes are made in the program:

```
JST       SETUP is replaced by JSK      SETUP     EQU     $
SETUP     ENT is replaced by SETUP
JMP       *SETUP is replaced by RSK
```

The Automatic I/O instruction consists of three words. The first word of the Automatic I/O instruction contains the opcode and the device address function code (DAFC). Bits 0-14 of the second word contain a two's compliment of the byte count. Bit 15 is used as an additional address bit to determine whether the transfer buffer byte address is in the upper or lower 64K bytes. When Bit 15 is 0, the address is in the upper 64K bytes; when Bit 15 is 1, the address is in the lower 64K bytes. The third word contains 16-bits of the byte absolute address. Bit 15 of the second word is added on by the CPU as a 17th, complimented, most significant bit to these 16 bits, to constitute the complete address of the byte. See Figure 3-1.

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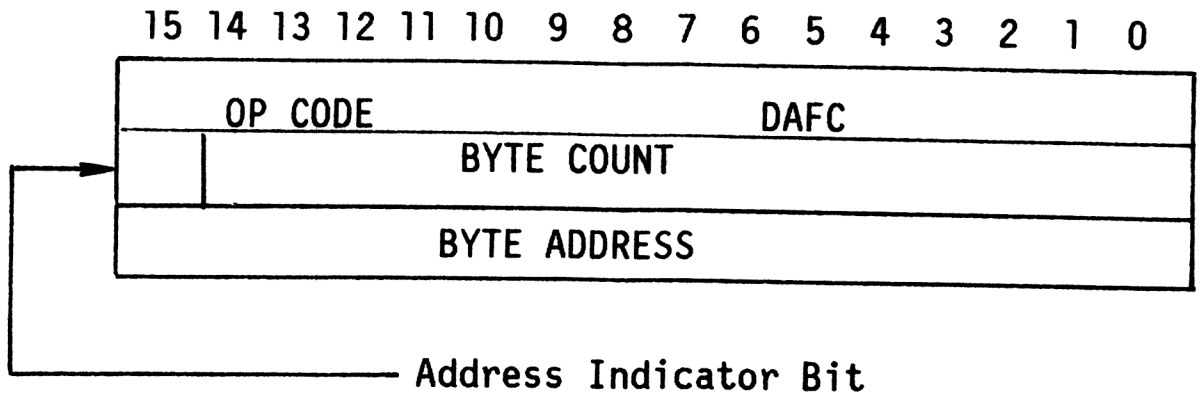


Figure 3-1. Automatic I/O Instruction Format

Negating the byte count sets Bit 15 of word two to 1 before the test for Bit 15 is made. The byte address is automatically incremented before data transfer takes place. To permit utilization of address zero, Bit 15 of word two is automatically set to 1 when the incrementation changes the absolute address value in word three from 32K to zero.

A NOP instruction must never be loaded in an interrupt vector address. The I/O Distributor does not cancel the interrupt when a NOP instruction is executed. This results in a constant interrupt to the CPU, preventing progress of the system program.

3.6 END-OF-BLOCK INTERRUPT

Most Intelligent Cables provide an End-of-Block interrupt at the completion of a data transfer sequence. The End-of-Block interrupts are vectored by the I/O Distributor to the channel data service address plus four. An appropriate End-of-Block routine must be provided at a convenient location in memory. The transfer of program control to the End-of-Block routine is set up in the form

```
        ABS     INTCNL+4        Channel End-of-Block Interrupt Vector Address
        JSK     *$+1
        DATA    EOB             Address of End-of-Block Routine
```

If the stack is not available JST must be substituted for JSK.

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3.7 UPDATE INTERRUPT STATUS (UIS) INSTRUCTION

The Update Interrupt Status Instruction outputs the CPU processor status word to all I/O devices in the system. The instruction is used to selectively enable or disable data service and EOB interrupts. Data service and EOB interrupts are disabled by setting bits 13 and 12, respectively, to 1. The processor status word is output by UIS in the assembler instruction command field. Table 3-1 summarizes the results of setting CPU status word Bits 12 and 13.

Table 3-1. Interrupt Disabling by CPU Status Word

BIT 12	BIT 13	DATA SERVICE	EOB
0	0	Enabled	Enabled
1	0	Enabled	Disabled
0	1	Disabled	Enabled
1	1	Disabled	Disabled

3.8 INTERRUPT VECTORING

Both the standard and the DMA I/O Distributors generate interrupts to the computer. Once the interrupt is recognized, the I/O Distributor must then provide a memory address to the computer for use as the next instruction address. This process is called interrupt vectoring.

Each channel of the standard I/O Distributor is able to provide two different interrupt vector addresses. One address is provided whenever data service is required and a second address is provided when the End-of-Block is encountered.

The actual addresses provided by the I/O Distributor are controlled by the I/O Distributor hardware. The following conventions determine the hardware assignment of the interrupt vector address:

- The interrupt vector addresses are assigned within a block of 64 consecutive memory addresses.
- Each channel is allocated eight consecutive memory addresses.
- An interrupt for data service is vectored to the channel low order memory address.
- An interrupt for End-of-Block service is vectored to the channel low order memory address plus four.
- The location of the 64 address block is selectable (in increments of 64 (:40) addresses) by strapping on the I/O Distributor.

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Figure 3-1 shows all the interrupt vector addresses for the 64 address block selected by the standard (factory) I/O Distributor strapping. This block starts at memory address :C0 and goes through address :FF.

Figure 3-1 also shows the format of the eight consecutive memory addresses for channel 0. The format for the remaining channels is the same. If the I/O Distributor is strapped for a different 64 address block (refer to Section 4 of this manual for details on strapping), the vector addresses would be changed. Each vector address in the new block would have the same relationship to the new low order memory address as the relationship shown in Figure 3-1.

The Distributed I/O System requires that an Automatic I/O instruction be stored in the data service area as shown. The End-of-Block subroutine is not restricted in the same manner. Normally, the form shown in Figure 3-1 is used to store the existing P count, jump to the End-of-Block subroutine, perform the subroutine, and then return to the mainline program at the stored P count address. A JST instruction is shown stored at the EOB interrupt vector location in the figure. NAKED MINI 4 Family computers normally use JSK, unless the stack is unavailable.

Channel	0	1	2	3	4	5	6	7
Data Service Vector Address	:C0	:C8	:D0	:D8	:E0	:E8	:F0	:F8
End-of-Block Vector Address	:C4	:CC	:D4	:DC	:E4	:E4	:F4	:FC

:C0	Auto I/O Op Code & Address	Data Service
:C1	Byte Count (Negated)	
:C2	Memory Buffer Pointer (Buffer-1)	
:C3	Reserve for LSI 4/10 Integrated I/O Distributor	
:C4	Jump and Store (JST * $+1)	EOB Service
:C5	EOB Subroutine Address	
:C6	Unused	
:C7	Unused	

Figure 3-2. Interrupt Vector Addresses

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3.9 DISTRIBUTED I/O SYSTEM COMMAND WORDS

The command words are used by the computer to control the operation of a Distributed I/O System channel (I/O Distributor and Intelligent Cable). The various configurations of command words used for this purpose are not part of the computer instruction set. The command words must be constructed individually and then output to the Distributed I/O System channel using an appropriate instruction word.

This section includes a description of the control significance of each command word bit followed by the descriptions of the various command configurations of the command word. Not all configurations are used with each Intelligent Cable. Refer to the Intelligent Cable User's Manual to determine the specific subset of command word configurations used.

3.9.1 Command Word Format

The eight most significant bits of the command word are the individual control bits and the eight least significant bits make up the various fields used in conjunction with specific control bits. The format of the command word is shown in Figure 3-2.

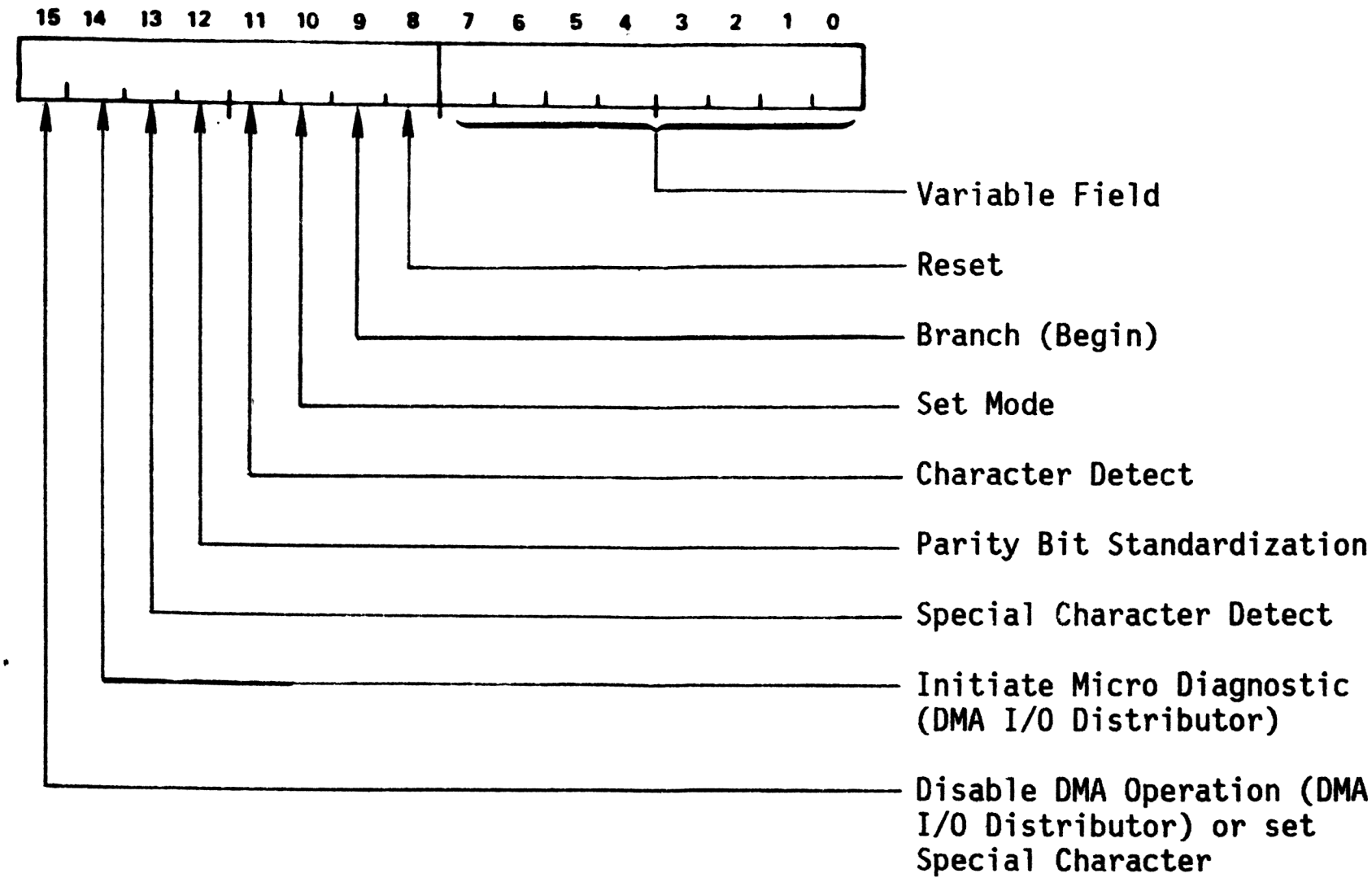


Figure 3-3. Distributed I/O System Command Word Format

3.9.1.1 Mode Field

The mode field is used in two different configurations, 4-bit and 8-bit. The field configuration is cable dependent. When limited to four bits (command word Bits 0 through 3), the mode field can share the eight least significant bits with the branch address field. The bits of the mode field are used to provide static control lines to the peripheral or control special features within the PICOPROCESSOR. Not all Intelligent Cables require mode bits and when used, the functions controlled vary depending on the type and operation of the Intelligent Cable. Refer to the appropriate Intelligent Cable user's manual.

3.9.1.2 Branch Address Field

The branch address field, Bits 4 through 7 of the command word, provides the PICOPROCESSOR firmware entry point address. The PICOPROCESSOR firmware must be in idle, firmware address :0, before the branch address is output and the branch address must be an allowed entry point to the firmware.

3.9.1.3 Special Character Field

The special character field uses Bits 0 through 7 to load a special character into the channel character-detect register. (The 14629 I/O Distributor, Revision A, does not use the special character field.)

3.9.1.4 Reset

A logical 1 in Bit 8 of the command word initiates a reset operation on the addressed channel. In the PICOPROCESSOR, the reset initializes the PICOPROCESSOR logic and, when applicable, issues a reset to the attached device.

3.9.1.5 Branch

A logical 1 in Bit 9 of the command word signals the PICOPROCESSOR to branch to the address provided in the branch field. At the same time, the I/O Distributor stores the configuration of command word Bits 11, 12, and 13 for use with the computer addressed Distributed I/O System channel.

3.9.1.6 Set Mode

A logical 1 in Bit 10 of the command word signals the PICOPROCESSOR to load the mode field bits into its mode register. A logical 0 allows the mode register configuration to remain unchanged.

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3.9.1.7 Character Detect Enable

A logical 1 in bit 11 of the command word causes the I/O Distributor to scan the channel data during the subsequent input data transfer for a predetermined character. When the character is detected, the I/O Distributor issues a byte count = 0 to the channel PICOPROCESSOR to terminate the data transfer. A logical 0 disables character detection.

Character detection in the standard I/O Distributor 14629 can detect only the 7-bits of the ASCII carriage return character (:0D).

3.9.1.8 Parity Bit Standardization

A logical 1 in Bit 12 of the command word causes the I/O Distributor to replace the most significant data bit (Bit 7) of all channel input data characters during the subsequent data transfer. The replacement occurs independent of the actual received bit value. The DMA I/O Distributor and the 53701 standard I/O Distributor can be strapped to use either a logical 1 or logical 0 as the replacement bit. The standard I/O Distributor 14629 is restricted to a logical 1 as the replacement bit. A logical 0 in Bit 12 disables parity bit standardization

3.9.1.9 Character Detect Selection

When Bit 11 is set to 1, enabling character detect, Bit 13 is used to select the character detected. When Bit 13 is 0, the channel data is scanned for the 7-bits of the ASCII carriage return character (:0D). When Bit 13=1, the channel data is scanned for the special character stored for the channel. (The 14629 I/O Distributor does not have special character detect capability.)

3.9.1.10 Initiate Micro Diagnostic (DMA I/O Distributor Only)

A logical 1 in Bit 14 of the command word causes the DMA I/O Distributor to perform the internal micro diagnostic on the addressed channel. Use of the internal micro diagnostic should be restricted and not included as part of any system programs.

3.9.1.11 Disable DMA Operation

When Bit 15 and Bit 9 (branch bit) of the command word are 1, DMA is disabled. This command is used with DMA I/O Distributors only, and cannot be combined with any other command. A logical 0 in Bit 15 allows normal operation.

3.9.1.12 Set Special Character

When Bit 15 is 1 and Bit 9 (branch bit) is 0, the DMA and 53701 standard I/O Distributors store the configuration of the special character field (command word Bits 0 through 7) as the channel special character. This command must not be combined with any other command. (The 14629 I/O Distributor does not have store special character capability.)

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3.9.2 Command Word Set

The 18 permissible configurations of the eight most significant command word bits make up the command word set of the Distributed I/O System. The operations controlled by these 18 command words are described in this section, and the hexadecimal skeleton for each command word is shown. (In the following descriptions, n is used to denote a variable field.) The complete Distributed I/O System command word set is as follows:

Reset	:0100
Branch	:0200
Set Mode	:040n or :04nn
Branch, Set Mode	:06nn
ASCII Carriage Return Detect	:0An0
ASCII Carriage Return Detect and Mode Field	:2Enn
Stored Channel Special Character Detect	:2An0
Stored Channel Special Character Detect and Set Mode	:2Enn
Load Special Character	:80nn
Branch, Parity Standardization	:12n0
Branch, Set Mode, and Parity Standardization	:16nn
Branch, Detect CR, Parity Standardization	:1An0
Branch, Set Mode, Detect CR, Parity Standardization	:1Enn
Branch and Special Character Detect	:3An0
Branch, Set Mode, and Special Character Detect	:3Enn
Branch, Disable DMA	:82n0
Branch, Set Mode, and Disable DMA	:86nn
Initiate Micro Diagnostic	:4000

3.9.2.1 Reset Command Word (:0100)

The reset command word is used to initialize the PICOPROCESSOR and peripheral on the addressed channel. In addition, any pending service requests are cancelled. Interrupts should be disabled when a reset command word is issued to avoid cancelling an interrupt in the process of being serviced. Since the reset command preempts any other operation in progress, it should be used only when necessary.

3.9.2.2 Branch Command Word (:0200)

The branch command is used to initiate all PICOPROCESSOR firmware sequences. Of the 18 permissible command words, 14 are in combination with the branch command.

3.9.2.3 Set Mode Command Words (:040n or :04nn)

The set mode commands are used to load the contents of the mode field into the PICOPROCESSOR mode register. The form of the set mode command word used depends on the Intelligent Cable for the channel. If the Intelligent Cable requires up to four mode bits, the four bit mode field must be used. If the PICOPROCESSOR requires more than four mode bits, the eight bit mode field must be used. The combining of the set mode command with any other command is restricted to those Intelligent Cables that require a maximum of four mode bits.

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3.9.2.4 Character Detect Command Words

The character detect command words are used to enable character detection for the addressed channel. The character detect command words are all combined words since the branch control bit (Bit 9) is required to effect the enabling of the feature. The mode control bit (Bit 10) can also be combined with character detect. I/O Distributor Model Number 53629 is limited to the detection of the ASCII carriage return character (enabled by Bit 11). All other I/O Distributors can detect either the ASCII carriage return character (if Bit 11 is set to 1) or the stored channel special character (enabled by setting Bits 11 and 13 to 1). It is not possible to scan for both special characters at the same time. The hexadecimal skeletons for the Character Detect Command Words are:

:0An0 - ASCII Carriage Return Detect
:0Enn - ASCII Carriage Return Detect and Mode Field
:2An0 - Stored Channel Special Character Detect
:2Enn - Stored Channel Special Character Detect and Mode Field

3.9.2.5 Load Special Character Command Word :80nn

The load special character command word is used to load the configuration of the eight least significant bits of the command word into the special character register for the addressed channel. This command must not be combined with any other command. (The 53629 I/O Distributor does not use this command word.)

3.9.2.6 Parity Standardization Command Words

The parity standardization command words are used to enable parity standardization for the addressed channel. Bit 12 is used to enable parity standardization. The parity standardization command words are all combined words since the branch control bit is required to effect the enabling of the feature. The hexadecimal skeletons for parity standardization command words are:

:12n0 - Branch Address Field

:16nn - Branch Address and Mode Field

:1An0 - Branch Address Field and ASCII Carriage Return Detect

:1Enn - Branch Address Field, Mode Field, and ASCII Carriage Return Detect

:3An0 - Branch and Special Character Detect

:3Enn - Branch Address, Mode Field, and Special Character Detect

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3.9.2.7 Disable DMA Command Words

The disable DMA command words are used to inhibit the DMA operation on the addressed channel. The disable DMA command words are all combined words since the branch control bit is required to effect the disabling of DMA. Disable DMA must not be combined with character detect or parity standardization. Disable DMA is used in the following types of operation:

- When program controlled data transfer is to be performed.
- When interrupts are to be disabled as for example, during AutoLoad.
- For program efficiency. If a data transfer will not occur (e.g., sense ready with the Magnetic Tape Intelligent Cable), the disable DMA eliminates the I/O Distributor overhead required to fetch the Auto I/O instruction from the computer memory.

To disable all DMA from an I/O Distributor, a separate disable DMA command word must be issued to each channel. Though issued separately, the disable DMA command for a channel is not totally independent. If a data service request occurs on a channel with DMA disabled, this data service request will mask any data service request on all lower priority channels, regardless of whether DMA is disabled for those channels. The hexadecimal skeletons for disable DMA command words are:

:82n0 Branch, Disable DMA

:86nn Branch, Set Mode, Disable DMA

The Branch, Disable DMA and Branch, Set Mode, Disable DMA command words do not affect the operation of the standard I/O Distributor and are treated the same as the corresponding Branch or Branch, Set Mode command words by the standard I/O Distributor.

3.9.2.8 Initiate Micro Diagnostic Command Word (:4000)

The initiate micro diagnostic command is used to initiate the DMA I/O Distributor macro diagnostic for the addressed channel. An End-of-Block interrupt indicates successful completion of the diagnostic. Use of this command should be restricted.

3.10 PROGRAMMING EXAMPLES

The following are generalized procedures for setting up I/O routines for use with Intelligent Cables attached to a standard or DMA I/O Distributor. The code shown is NAKED MINI® 4 assembler. Specific details of the routines are Cable dependent. Refer to the appropriate section of the Intelligent Cables User's Manual or individual Intelligent Cable manual.

The first section of code is the parameter equates that define a series of constants used to assemble the various routines. The first five establish the device address and interrupt vector locations. The remaining equates select Intelligent Cable operations.

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```
*
* PARAMETER EQUATES FOR THE INTELLIGENT CABLE
*
INTBAS    EQU       :C0            INTERRUPT VECTOR BASE (STRAPPED ON I/O
                                         DISTRIBUTOR)
CHAN      EQU       (specify)      INTELLIGENT CABLE IS PLUGGED INTO THIS CHANNEL
IOD       EQU       :F             ADDRESS BASE (STRAPPED ON I/O DISTRIBUTOR)
INTAD     EQU       CHAN%3+INTBAS  DATA INTERRUPT VECTOR ADDRESS FOR INTELLIGENT
                                         CABLE
ICDA      EQU       IOD%3+CHAN%1   INTELLIGENT CABLE DEVICE ADDRESS
*
SETMOD    EQU       :400           SET MODE COMMAND WORD BASE
BRANCH    EQU       :200           BRANCH COMMAND WORD BASE
OUT       EQU       :30            OUTPUT SEQUENCE ADDRESS
IN        EQU       :48            INPUT SEQUENCE ADDRESS
```

The following sections of code-interrupt vectored locations (output) and interrupt vectored locations (input) define and fill the memory locations associated with the I/O Distributor channel to which the Intelligent Cable is connected. There are six memory locations used with each of these sections of code; however, these are the same six memory locations for both sections of code since all data service and End-of-Block service interrupts for the I/O Distributor channel where the Intelligent Cable is connected are vectored to the same memory addresses. Each time the Automatic I/O operation must be switched from input to output or output to input, the interrupt vectored locations must be filled with the corresponding instruction information. When repeated input or output operations are performed, only the byte count and buffer address must be respecified at the start of the operation.

```
*
* INTERRUPT VECTORED LOCATIONS (OUTPUT)
*
          ABS       INTAD          INTERRUPT VECTORED LOCATIONS
          AOB       ICDA           AUTOMATIC OUTPUT BYTE INSTRUCTION
          WORD      -OUTCNT        NEGATIVE OF THE OUTPUT BYTE COUNT
          WORD      OUTBUF*2-1     ADDRESS OF THE OUTPUT BUFFER
          WORD      0              NOT USED
          JST       *$+1           CALL END-OF-BLOCK ROUTINE
          DATA      EOBLOC         ADDRESS OF END-OF-BLOCK ROUTINE
*
* INTERRUPT VECTORED LOCATIONS (INPUT)
*
          ABS       INTAD          INTERRUPT VECTORED LOCATIONS
          AIB       ICDA           AUTOMATIC INPUT BYTE INSTUCTION
          WORD      -INCNT         NEGATIVE OF THE INPUT BYTE COUNT
          WORD      INBUF*2-1      ADDRESS OF THE INPUT BUFFER
          WORD      0              NOT USED
          JST       *$+1           CALL END-OF-BLOCK ROUTINE
          DATA      EOBLOC         ADDRESS OF END-OF-BLOCK ROUTINE
```


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The following section of code is a subroutine used to transmit data. The subroutine must assemble the interrupt vectored locations for output. The procedure is shown in 3.5.2.2. AIB must be substituted for AOB in the code. The subroutine then issues the command word to output data to the Intelligent Cable. Once the data transmission is started, the subroutine returns to the caller. The actual data transmission continues until terminating conditions are detected, at which time the End-of-Block service is performed.

Calling sequence:

```
                JST       OUTDAT
*
*SUBROUTINE TO OUTPUT DATA
*
OUTDAT          ENT                              ENTRY POINT FOR SUBROUTINE
                 .
                 .
                 .                               ASSEMBLE AUTOMATIC I/O
                 .                                    INTERRUPT VECTOR LOCATIONS
                 .
                 .
                COPY      =SETMOD+BRANCH+OUT+WORD,A
                                                 ASSEMBLE COMMAND WORD TO START DATA
                                                      TRANSMISSION
                OUT       A,ICDA+1               SEND COMMAND WORD TO I/O DISTRIBUTOR
                SBIT      8,S                    ENABLE INTERRUPTS
                JMP       *OUTDAT                RETURN TO CALLER
*
*AUTOMATIC I/O BYTE COUNT AND BUFFER ADDRESS
*
OUTCNT          EQU       (specify)              LENGTH OF DATA TRANSMISSION
OUTBUF          EQU       (specify)              ADDRESS OF OUTPUT BUFFER
```

The following section of code is a subroutine used to accept data. The subroutine must assemble the interrupt vectored locations for input. The procedure is shown in 3.5.2.2. The subroutine then issues the command word to accept data through the Intel[illegible]ubroutine returns to the caller and data is accepted u[illegible]erminatin, conditions are detected, at which time the End-of-Block se[illegible]is performed.

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Calling sequence:

```
                JST       INDAT * *SUBROUTINE TO INPUT DATA *
INDAT           ENT                           ENTRY POINT FOR SUBROUTINE
                .         .                   ASSEMBLE INTERRUPT VECTORED
                .                                   LOCATIONS FOR INPUT
                .
                COPY      =SETMOD+BRANCH+OUT+WORD,A

                .
                .                             ASSEMBLE COMMAND WORD TO START
                .                                   DATA TRANSMISSION
                OUT       A,ICDA+1            SEND COMMAND WORD TO I/O DISTRIBUTOR
                JMP       *INDAT              RETURN TO CALLER
*
*AUTOMATIC I/O BYTE COUNT AND BUFFER ADDRESS
*
INCNT           EQU       (specify)           LENGTH OF DATA INPUT
INBUF           EQU       (specify)           ADDRESS OF INPUT BUFFER
```

After all Automatic I/O data transfers are completed, the Intelligent Cable vectors the last I/O interrupt to the End-of-Block service location. Possible uses for the subroutine called by the interrupt are to initiate processing of data transferred or perform error analysis. The demonstration code simply halts.

```
*
* END-OF-BLOCK SERVICE
*
EOBLOC          ENT                           END-OF-BLOCK ENTRY POINT
                HLT
```


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SECTION 4

INSTALLATION

This section describes the complete installation of the Distributed I/O System for both standard and DMA I/O Distributors. All strapping requirements for the Intelligent Cables are provided in the Intelligent Cables User's Manual or the appropriate individual Intelligent Cable manual. Refer to the manuals provided by the peripheral manufacturer for any special installation requirements.

The installation sequence, as presented here, is the recommended order for performing the various steps. This sequence should be followed as closely as possible.

4.1 PRIORITY AND CHANNEL SELECTION

Each Intelligent Cable, when attached to an I/O Distributor, assumes a priority level. The location of this priority level, in relation to other peripherals, is determined by a combination of the following:

- The type of I/O Distributor - standard or DMA - in use.
- The priority level of the I/O Distributor channel to which the Intelligent Cable is attached, and the number and priority levels of the I/O Distributor channels actually in use.
- The priority level of the I/O Distributor in relation to other interface controllers attached to the computer.

When configuring a system for installation of an I/O Distributor, determine the desired priority level for each system peripheral device. Then plan the I/O Distributor location within the computer and the channel assignments for the Intelligent Cables attached to each I/O Distributor. When determining priority levels, give special consideration to any special Intelligent Cable bandwidth requirements in relation to the bandwidth capabilities of the computer system used. The bandwidth specifications are listed in Section 1 of this manual.

4.1.1 I/O Distributor Channel Priority

The interrupt priority level of each Intelligent Cable attached to an I/O Distributor is determined by the channel number to which it is connected. The lowest numbered channel on an I/O Distributor has the highest priority. With the 8-channel standard I/O Distributor, the highest priority channel is Channel 0. With the 4-channel standard I/O Distributor, the highest priority channel is Channel 4. The DMA I/O Distributor is limited to four channels, either Channels 0 through 3 or Channels 4 through 7. Depending on the strapping, the priority channel is either 0 or 4.

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The I/O Distributor does not scan the channels to service interrupt request. When the I/O Distributor completes the service of an interrupt request, the highest priority interrupt request then present is serviced. All channel data service requests are assigned a higher priority by the I/O Distributor than any channel End-of-Block service request. Computer Automation software uses the standard I/O Distributor channel assignments shown in Table 4-1.

4.1.2 MAXI-BUS® Interrupt Priority

The interrupt priority level of each device attached to the computer MAXI-BUS® is determined by its relative positon in the interrupt priority chain. The device closest to the processor has the highest priority. Each additional device added to the interrupt priority chain assumes a lower priority determined by the total number of devices in the chain between it and the processor. With the Distributed I/O System, all four or eight channels of the I/O Distributor placed closest to the processor have a higher effective priority than any channel of any other I/O Distributor placed further from the processor. The priority level of an I/O Distributor is independent of the I/O Distributor address. For a detailed description of priority level assignment, consult any LSI or NAKED MINI® Family computer reference manual.

4.1.3 MAXI-BUS® DMA Priority

The DMA priority level of each DMA device attached to the computer MAXI-BUS® is determined by its relative position in the DMA priority chain. As with the interrupt priority chain, the DMA device closest to the processor (in the DMA priority chain) has the highest priority. The DMA priority level of a DMA I/O Distributor is independent of the DMA I/O Distributor address.

Some DMA controllers have the ability to transfer data in bursts of two or more characters. After each character of the burst is transferred to memory, a higher priority DMA controller can interrupt the burst. Lower priority DMA controllers must wait until the burst in completed.

In the half-card chassis, the DMA priority chain starts at the processor slot and each slot position further away from the processor is a lower priority.

In a full-card chassis, the DMA priority chain starts at the half-card processor slot, the 100 side of the top slot. The DMA prioity chain then goes to the 200 side of the top slot, down to the 200 side of the second slot, down to the 200 side of the third slot, etc. As before, each slot position further away from the processor is a lower priority.

The DMA I/O Distributor assumes a priority level in both the DMA and interrupt priority chains. Since the DMA interrupt priority level applies only to End-of-Block service, the placement of the DMA I/O Distributor in the interrupt priority chain has a minimum affect on the operation of the DMA I/O Distributor. However, the operation of standard I/O Distributors attached to the same MAXI-BUS® may be affected. Placing a standard I/O Distributor further from the processor in the interrupt priority chain than a DMA I/O Distributor makes all priority levels assigned to the standard I/O Distributor a lower priority level than the End-of-Block interrupt assigned to the DMA I/O Distributor.

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Table 4-1. Channel Assignments

I/O DISTRIBUTOR CHANNEL NUMBER	INTELLIGENT CABLE
0	Card Reader
1	Magnetic Tape
2	Modem
3	IEEE
4	TTY or CRT
5	HSPT Reader
6	HSPT Punch
7	Line Printer

4.2 STANDARD I/O DISTRIBUTOR STRAPPING

The strapping on the standard I/O Distributor is used to assign the I/O Distributor number, select the interrupt vector block of addresses, and select the baud clock rate for each channel. Figure 4-1 shows the strapping locations on the standard I/O Distributor, 14629, Revision C. Figure 4-2 shows the strapping locations on the standard I/O Distributor, 53701 (all revisions). I/O Distributor 53701, Revision B, does not have left (when viewed from the component side) edge connectors. The edge connectors are for test purposes only and this is the only functional difference between the B and C revisions. The Revision C board is shown in the figure.

4.2.1 Standard I/O Distributor Device Address Assignment

The decode logic of the standard I/O Distributor must be set to respond to the base device address provided by Bits 4-7 of the instruction word. On the 14629 Distributor board, Bits 6 and 7 are permanently set to "1." Bits 4 and 5 are selected by strapping. This provides a base address range of :C to :F. See Table 4-2.

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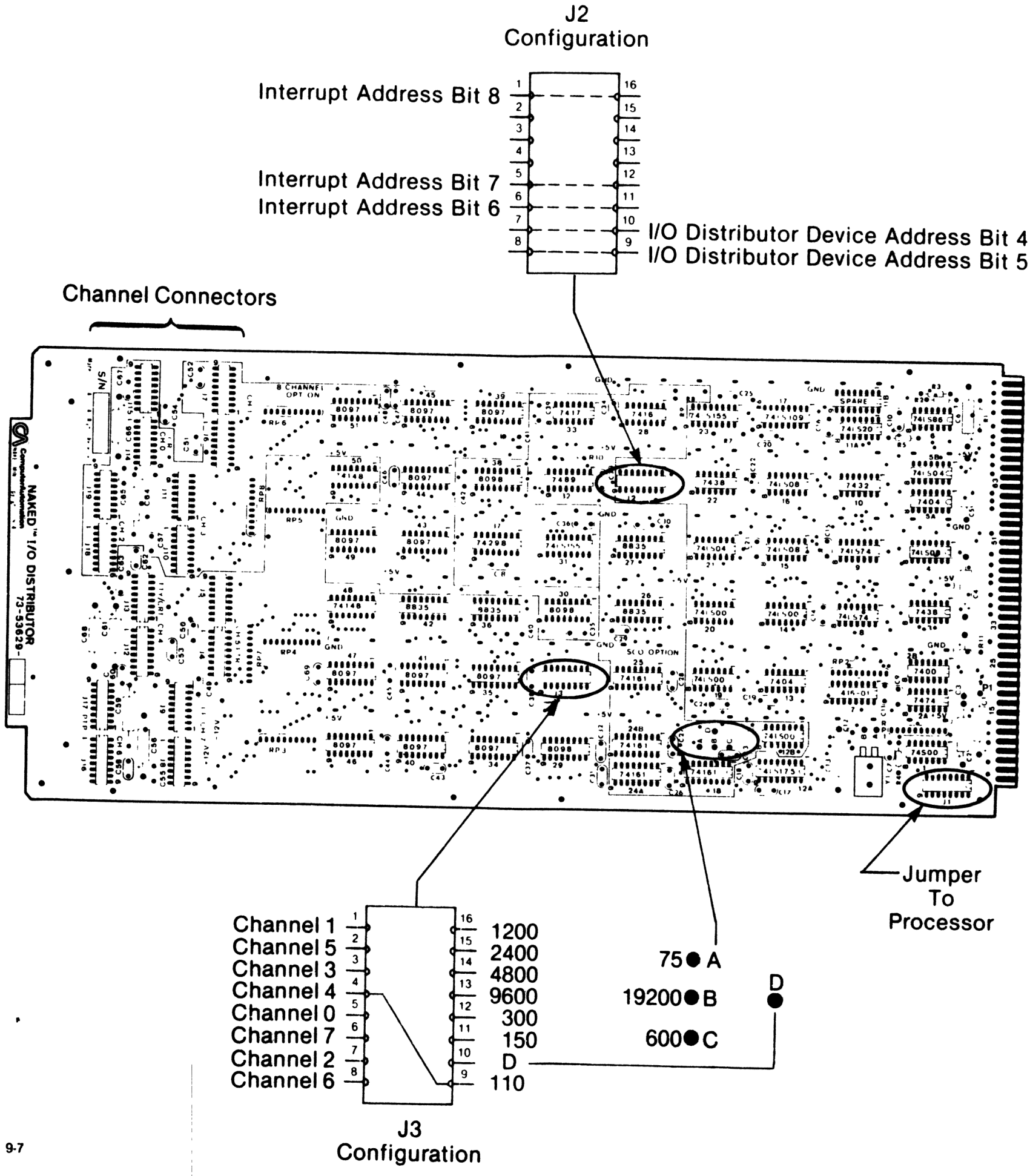


Figure 4-1. Standard I/O Distributor Board, 14629, Revision C

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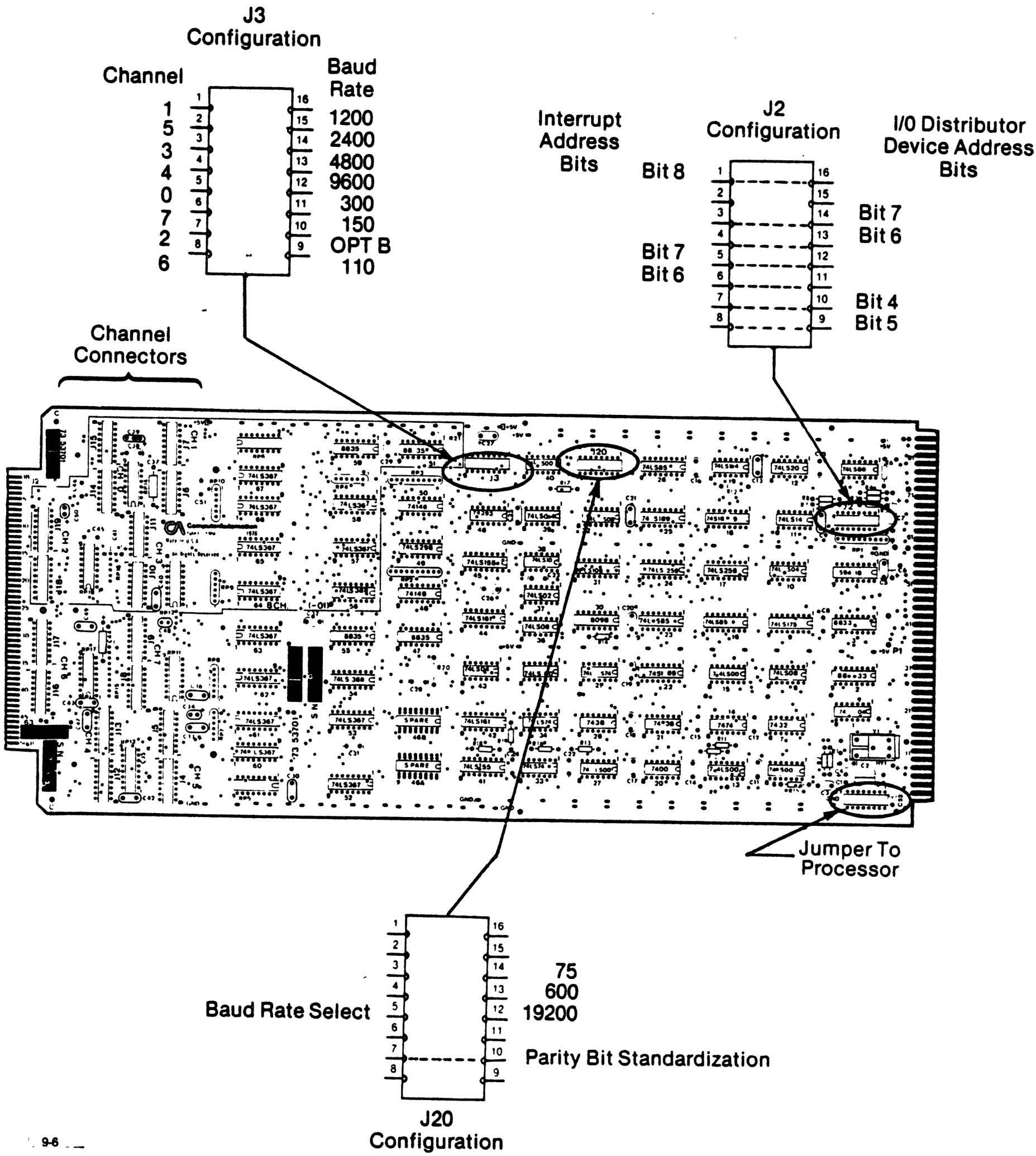


Figure 4-2. Standard I/O Distributor Board, 53701, Revision C

Table 4-2. Standard I/O Distributor 14629 Device Address Assignment

Jumper	8 To 9	7 To 10	
Bit	5	4	Address
	In	In	:C
	Open	In	:D
	In	Open	:E
	Open	Open	:F

Standard

Table 4-3. Standard I/O Distributor 53701 Device Address Assignment

Jumper	14 To 3	13 To 4	9 To 8	10 To 7	
Bit	7	6	5	4	Address
	Invalid-Dedicated				:0
	In	In	In	Out	:1
	In	In	Out	In	:2
	In	In	Out	Out	:3
	In	Out	In	In	:4
	In	Out	In	Out	:5
	In	Out	Out	In	:6
	In	Out	Out	Out	:7
	Out	In	In	In	:8
	Out	In	In	Out	:9
	Out	In	Out	In	:A
	Out	In	Out	Out	:B
	Out	Out	In	In	:C
	Out	In	Out	Out	:D
	Out	Out	Out	In	:E
	Out	Out	Out	Out	:F

Standard

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On the 53701 Distributor board (all revisions), all address bits are selected by strapping. Since :0 is a dedicated address, this provides an address range of :1 to :F for the Distributor. See Table 4-3. A base address of :F is standard for all I/O Distributors.

For both types of I/O Distributors, the required jumpers are installed on the header provided at J2 using number 24 to 28 gauge solid wire and soldered connectors. All the jumpers on J2 go straight across the header.

4.2.2 Interrupt Address Block Selection

The logic of the standard I/O Distributors must be set to provide the desired interrupt addresses. The interrupt address block consists of 64 (:40) consecutive memory positions, within which each channel is allocated eight consecutive locations. The base interrupt address is established by strapping options (Bits 6, 7 and 8) allowing the relocation of the address block in increments of :40 from base address zero to :1C0. Bits 3, 4 and 5 are provided by the channel End-of-Block service request. Bit 2 is controlled by the type of interrupt involved, data service or End-of-Block. See Table 4-4.

When a 4-channel standard I/O Distributor is used, only the 32 most significant consecutive memory addresses of an interrupt address block are used. The remaining 32 least significant memory addresses may be used for any other purpose including use by a DMA I/O Distributor as an interrupt address block. See Section 4.3 on DMA I/O Distributor Strapping for further information.

The required jumpers are installed on the header provided at J2 using number 24 to 28 gauge solid wire and soldered connections. All the jumpers on J2 go straight across the header.

Table 4-4. Standard I/O Distributor Interrupt Address Block Assignment

Interrupt Address Block	Jumper			
	1 to 16	5 to 12	6 to 11	
:00 through :3F	Open	In	In	
:40 through :7F	Open	In	Open	
:80 through :BF	Open	Open	In	
:C0 through :FF	Open	Open	Open	Standard
:100 through :13F	In	In	In	
:140 through :17F	In	In	Open	
:180 through :1BF	In	Open	In	
:1C0 through :1FF	In	Open	Open	

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4.2.3 Baud Rate Selection

Baud rate selection is required when one or more serial data format Intelligent Cables are attached to a standard I/O Distributor. Ten separate baud rates are provided. Of these, seven are directly available for use by any of the I/O Distributor channels. One of the three remaining rates, 75 baud, 600 baud, and 19,200 baud, can be selected for inclusion with the seven directly available rates, making a set of eight. Each channel can then be independently strapped to any of the available baud rates. The J3 header is factory wired to select a baud rate of 110 for Channel 4. The required jumpers are installed on the header provided at J3 using number 24 to 28 gauge insulated wire and soldered connectors. The above description applies to both the 14629 and 53701 boards. See Figures 4-1 and 4-2.

The 14629 and 53701 boards differ in the way the selectable board rates are chosen. On the 14629 board, if the 75, 600, or 19,200 baud rate is required, a jumper is installed between the D pad and the pad (A, B, or C) corresponding to the desired baud rate. The rate selected is available at pin 10 on J3. See Figure 4-1.

On the 53701 board (all revisions) the selectable baud rate desired is chosen by strapping pin 12, 13, or 14 to pin 5. The selected rate, 75, 600, or 19,200 baud, is available at pin 10 on J3. See Figure 4-2.

4.2.4 Parity Bit Standardization (Parity Bit Substitution)

On the 53701 board (all revisions) parity standardization selection is available to allow use of either a "1" or a "0" as the substitution value for the parity bit. Jumpering between pin 7 and pin 10 selects a "1", used with LSI Family computers. No jumper gives a "0" as the sutstitution value, used with NAKED MINI® 4 Family computers.

4.3 DMA I/O DISTRIBUTOR STRAPPING

The strapping on the DMA I/O Distributor is used to assign the I/O Distributor number, select the interrupt vector block of addresses, select the baud clock rate for each channel, and select the parity standardization bit value. Figure 4-3 shows the B revision of the 53674 board. The C revision of the board, which uses switches to select the parity standarization bit, is shown in Figure 4-4.

4.3.1 DMA I/O Distributor Device Address Assignment

The decode logic of the DMA I/O Distributor must be set to respond to the base device address provided by four bits of the instruction word. The two high order address bits are permanently set to "1." The two low order address bits are jumper selectable. This provides a base device address range of from :C to :F. An address of :F is standard. See Table 4-5.

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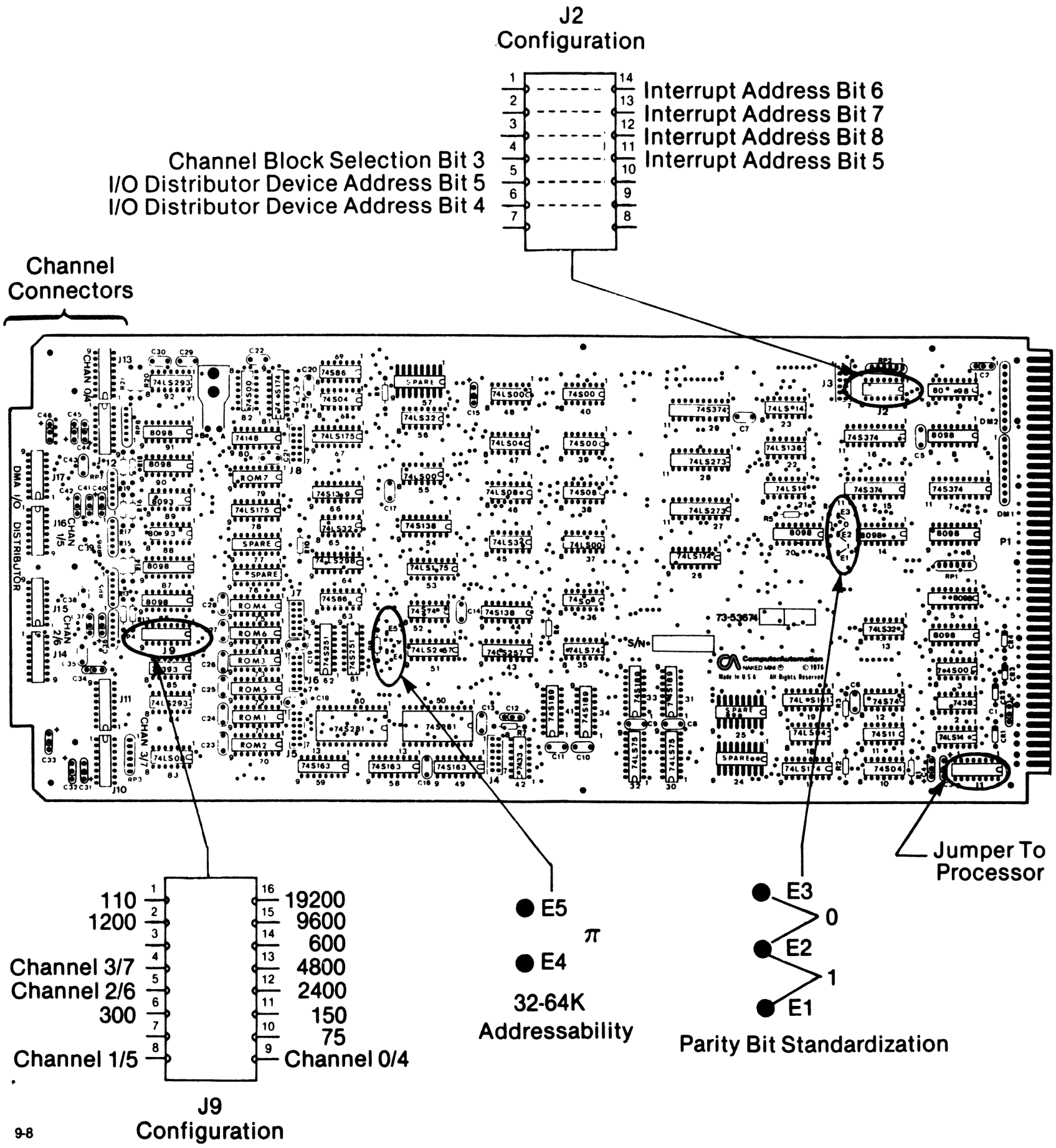


Figure 4-3. DMA I/O Distributor Board, 53674, Revision B

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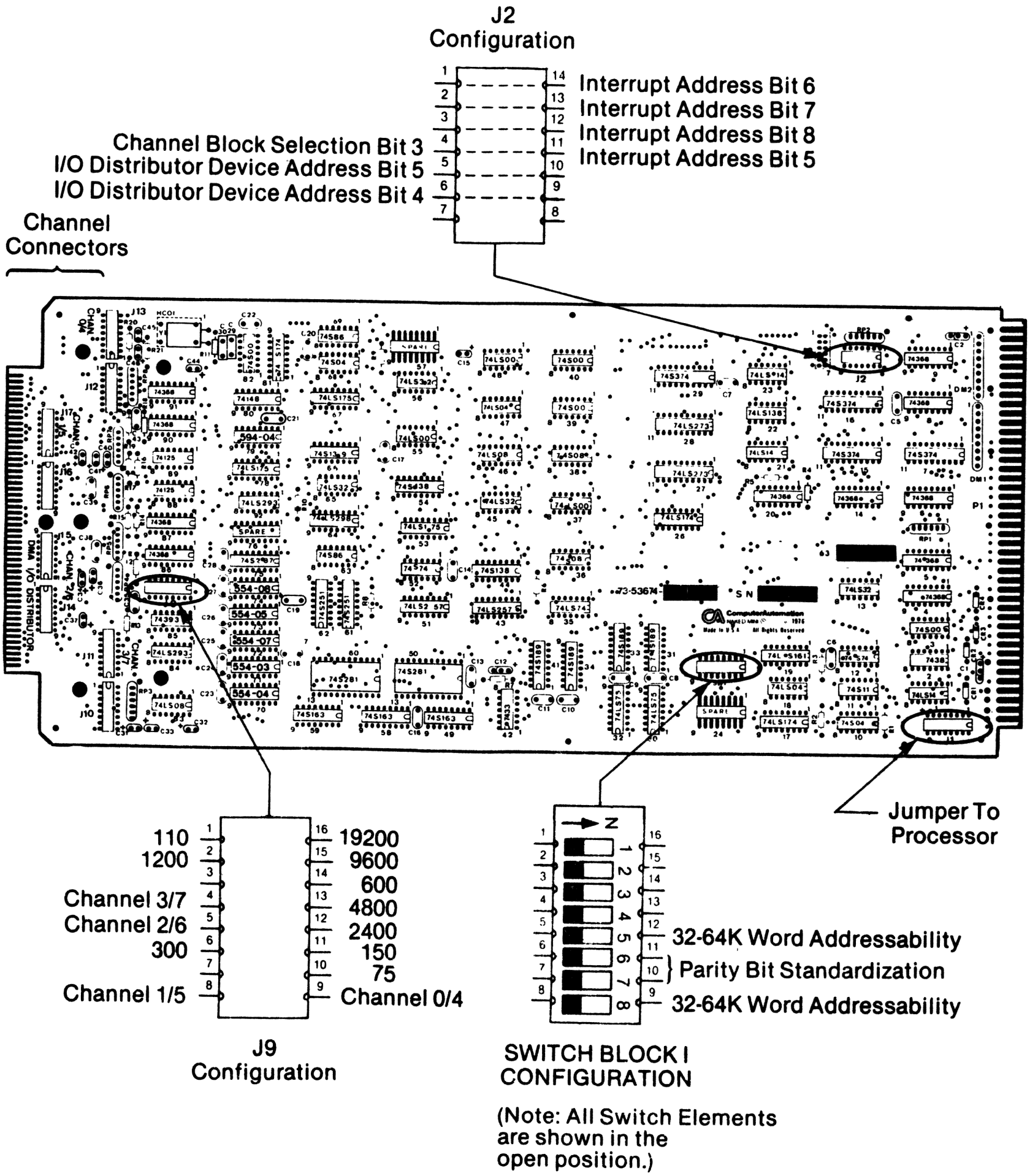


Figure 4-4. DMA I/O Distributor Board, 53674, Revision C

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Table 4-5. DMA I/O Distributor 53674 Device Address Assignment

JUMPER	5 TO 10	6 TO 9	
BIT	5	4	ADDRESS
	In	In	:C
	In	Open	:D
	Open	In	:E
	Open	Open	:F

Standard

An additional jumper at location 4-11 assigns the four DMA I/O Distributor channels as 0 - 3 or 4 - 7. Leaving the position open selects channels 4-7. Inserting a jumper selects channels 0-3. This feature allows a DMA I/O Distributor to share an interrupt address block with a 4-channel standard I/O Distributor or with another DMA I/O Distributor. When two I/O Distributors share an interrupt address block, both I/O Distributors should be assigned the same number and address. The two I/O Distributors can then be treated as a single, 8-channel I/O Distributor.

The required jumpers are installed on the header provided at J2 using number 24 to 28 gauge solid wire and soldered connections. All the jumpers on J2 go straight across the header.

4.3.2 Interrupt Address Block Selection

The logic of the DMA I/O Distributor must be set to provide the desired interrupt addresses for End-of-Block service. The addresses that correspond to the data service interrupt addresses in the standard I/O Distributor are used by the DMA I/O Distributor when the Automatic I/O instruction is fetched or restored. Refer to Table 4-6. It should be noted that jumper position 4-11, used to select channels 0-3 or 4-7, also selects interrupt address bit 5.

Table 4-6. DMA I/O Distributor 53674 Interrupt Address Block Selection

INTERRUPT ADDRESS BLOCK	JUMPER		
	3 TO 12	2 TO 13	1 TO 14
:00 through :3F	Open	In	In
:40 through :7F	Open	In	Open
:80 through :BF	Open	Open	In
:C0 through :FF	Open	Open	Open
:100 through :13F	In	In	In
:140 through :17F	In	In	Open
:180 through :1BF	In	Open	In
:1C0 through :1FF	In	Open	Open

Standard

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The interrupt address block consists of 64 consecutive memory positions, within which each channel is allocated eight consecutive locations. The base interrupt address is established by strapping options which allow relocating the address block in increments of :40 from base address zero to :1C0. On the A revision of the board, interrupt address Bits 6, 7, and 8 are selected by strapping and Bits 3, 4, and 5 are provided by the channel End-of-Block service request. On the B and C revisions the four high order interrupt address bits are selected by strapping. The DMA I/O Distributor only interrupts for End-of-Block service so Bit 2 is always a 1 for the interrupt. (Bit 2 is a 0 for the fetch and restore operation.)

The DMA I/O Distributor is limited to four channels and only 32 consecutive memory addresses of the block of 64 are used. If the DMA I/O Distributor is strapped for channel 0 through 3, the 32 least significant memory addresses in the block are used. If the DMA I/O Distributor is strapped for channels 4 through 7, the 32 most significant memory addresses in the block are used. The remaining 32 memory addresses in the block may be used for any other purpose including use by another DMA I/O Distributor or a 4-channel standard I/O Distributor as an interrupt address block.

A 4-channel standard I/O Distribtor and a DMA I/O Distributor can share the same block of 64 interrupt addresses. The standard I/O Distributor must use channels 4-7 and the 32 most significant memory addresses, requiring the DMA I/O Distributor to use channels 0-3 and the 32 least significant memory addresses. The result of such device address and interrupt block sharing appears to the software as a single I/O Distributor.

The required jumpers are installed on the header provided at J2 using number 24 to 28 gauge solid wire and soldered connections. All the jumpers on J2 go straight across the header.

4.3.3 Baud Rate Selection

Baud rate selection is required when one or more serial data format Intelligent Cable/peripheral pairs are attached to a DMA I/O Distributor. The ten separate baud rates provided are all directly available for use by any of the DMA I/O Distributor channels. Refer to Figures 4-3 and 4-4.

The required jumpers are installed on the header provided at J9 using number 24 to 28 gauge insulated solid wire, and soldered connections.

4.3.4 Parity Bit Standardization (Parity Bit Substitution)

Parity standardization selection is available to allow use of either a "1" or a "0" as the substitution value for the parity bit. Revisions A and B are factory strapped for "1" as the substitution value. To select the "0," remove the jumper between E1 and E2. Install a jumber between E2 and E3 using number 24 to 28 gauge solid wire soldered connections. See Figure 4-3.

Revision C uses two switch elements on the SWI switch block to select the parity standarization bit. Parity 0 is selected by closing position 7-10 and opening position 6-11. The reverse procedure gives parity 1. Other combinations (i.e., both open or both closed), give unpredictable results. The NAKED MINI® Family use parity 0. The LSI Family uses parity 1. See Figure 4-4 and Table 4-7.

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Table 4-7. Parity Bit Substitution Value Selection, Revision C Boards

PARITY BIT SUBSTITUTION VALUE	SWITCH POSITION 7-10	SWITCH POSITION 6-11	COMPUTER FAMILY
0	Closed	Open	NAKED MINI® 4
1	Open	Closed	LSI
Invalid (Unpredictable Results)	Open	Open	
	Closed	Closed	

4.3.5 32-64K Addressability

On the A and B Revisions of the board, insertion of a jumper between positions E4 and E5 gives 64K addressability, selected for NAKED MINI® 4 Family computers. LSI Family computers use 32K word addressability. See Figure 4-3.

The Revision C Board uses switch elements at positions 8-9 and 5-12 on the SWI switch block to determine 32-64K word addressability. Both switches are closed for NAKED MINI® 4 Family computers, giving 64K addressability, and open for LSI Family computers, giving 32K. See Figure 4-4 and Table 4-8.

4.4 I/O DISTRIBUTOR INSTALLATION

The installation of the I/O Distributor involves several operations. The type of I/O Distributor and the chassis used determines the specific operations required. This section describes the installation of both the DMA and standard I/O Distributor into the half-card chassis. The procedures for joining two half-cards together and the installation of both I/O Distributors into a full-card chassis are also described.

Table 4-8. 32-64K Addressability, Revision C Boards

ADDRESSABILITY	SWITCH POSITION 8-9	SWITCH POSITION 5-12	COMPUTER FAMILY
64K	Closed	Closed	NAKED MINI® 4
32K	Open	Open	LSI
Invalid (Unpredictable Results)	Open	Closed	
	Closed	Open	

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4.4.1 Standard I/O Distributor; 14629, Revision A Half-Card Chassis

The standard I/O Distributor installation kit for a half-card chassis includes an Intelligent Cable retainer/strain relief and the necessary mounting hardware. Refer to Figure 4-5. Prepare the standard I/O Distributor for installation as follows.

1. Install both circuit card ejectors on the I/O Distributor using the split pins provided. Position the ejectors so the short arms extend beyond the sides of the circuit card.

2. Install the stiffener so the raised portion is closest to the outer edge of the circuit card. Attach the stiffener with the hardware provided.

3. Plug the I/O Distributor end of the Intelligent Cables into the desired channel connectors.

4. Ensure that the ribbon cables on the outer row of Intelligent Cables are flat and smooth from the connector to the stiffener and that the ribbon cables on the inner row of Intelligent Cables are flat and smooth from the connector, across the outer row of connectors to the stiffener.

5. Place the cable retainer over all the Intelligent Cables so that all five holes in the cable retainer align with the mating holes in the mounting blocks or stiffener. Attach the cable retainer with the hardware provided. The standard I/O Distributor is now ready for installation in a half-card chassis.

4.4.2 Standard I/O Distributor, 14629, Revisions B and Above, Half-Card Chassis

The standard I/O Distributor, 14629, Revisions B and above use a bar rather than a flap-type cable retainer. The installation procedure is the same as that described above, except that the retainer bar is attached to the stiffener bar only using two screws. The bar is attached with the edge-flap facing forward. See Figure 4-6.

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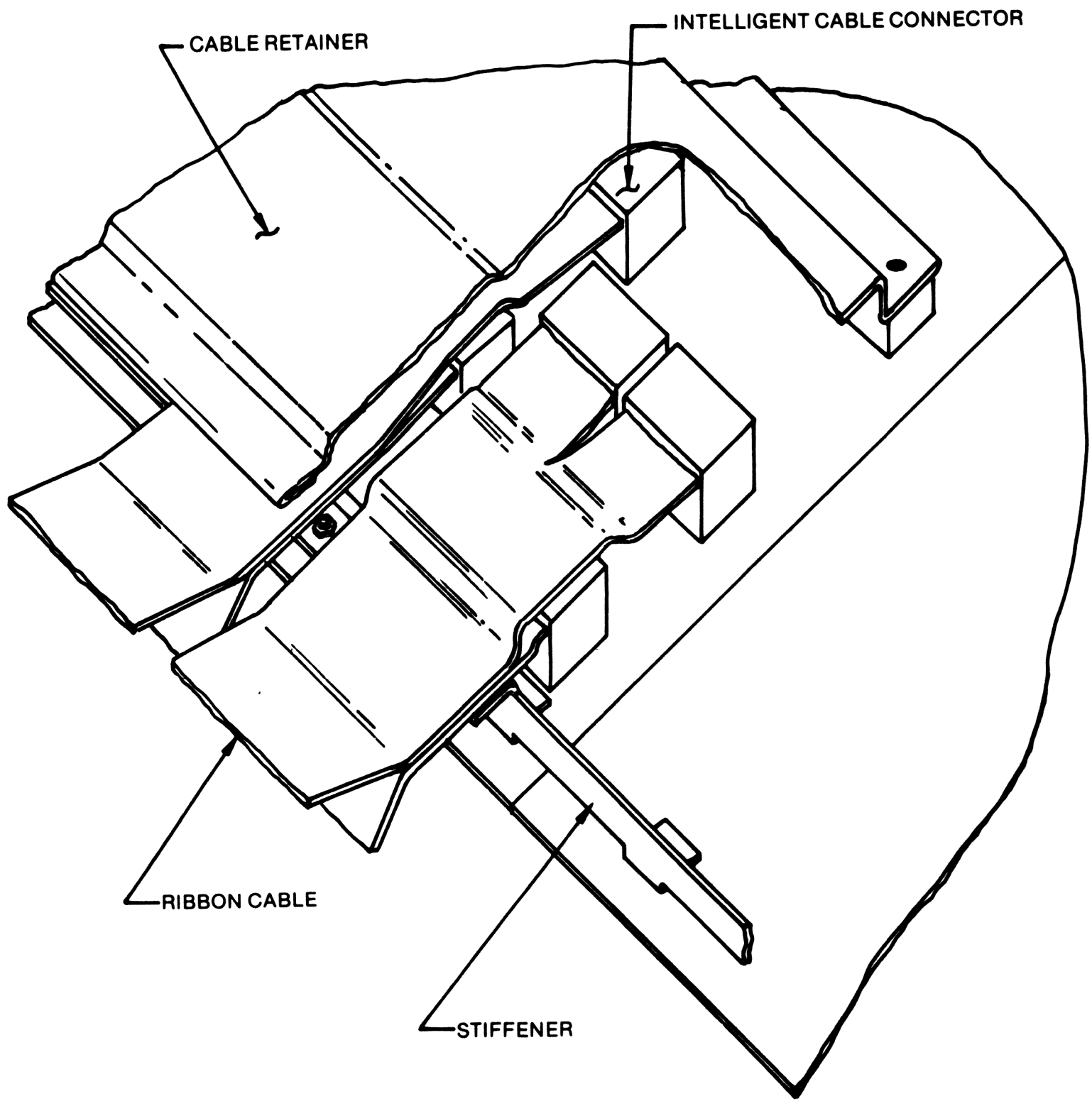
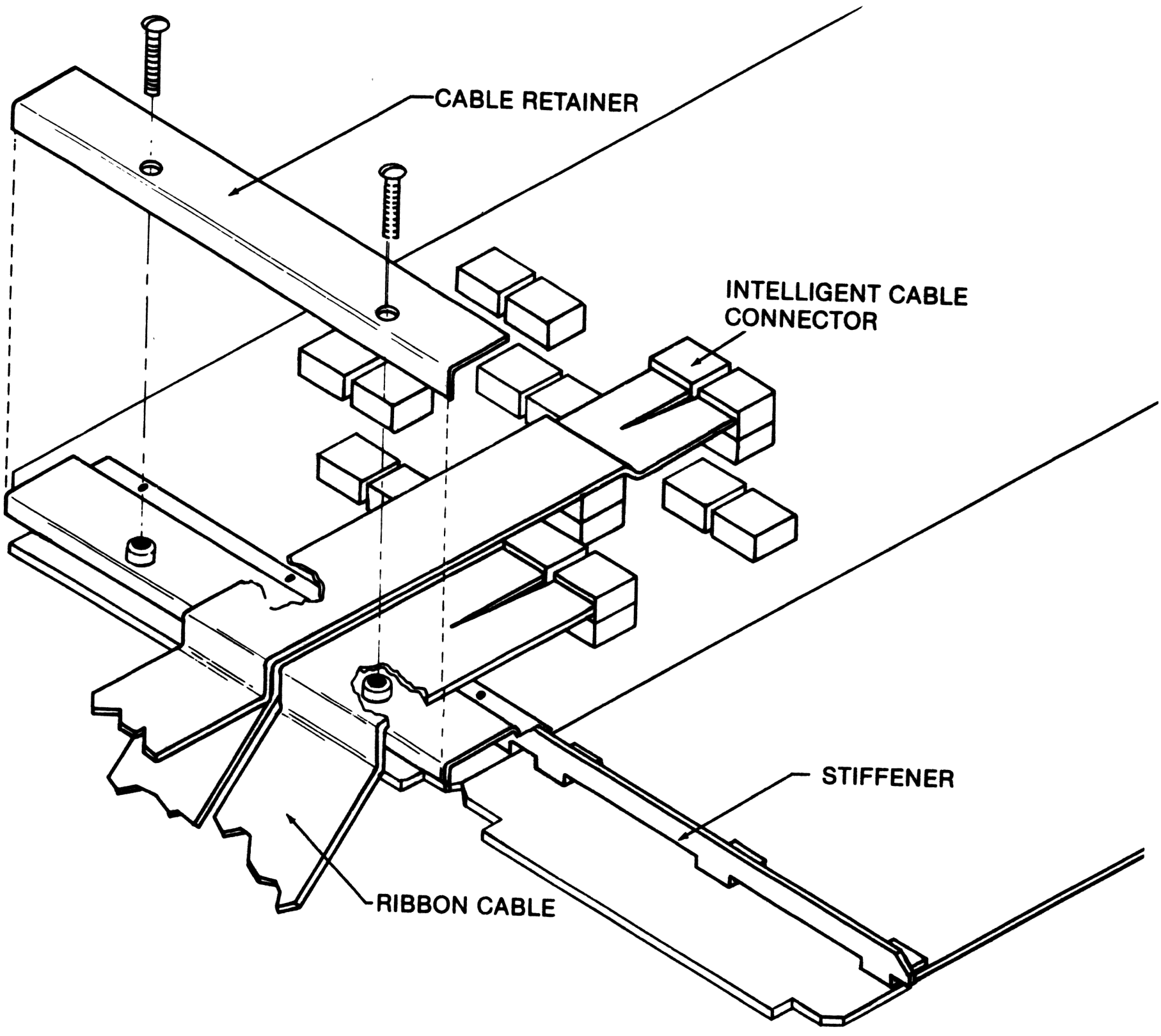


Figure 4-5. Cable Retainer, Standard I/O Distributor 14629, Revision A (shown joined to another half-card)

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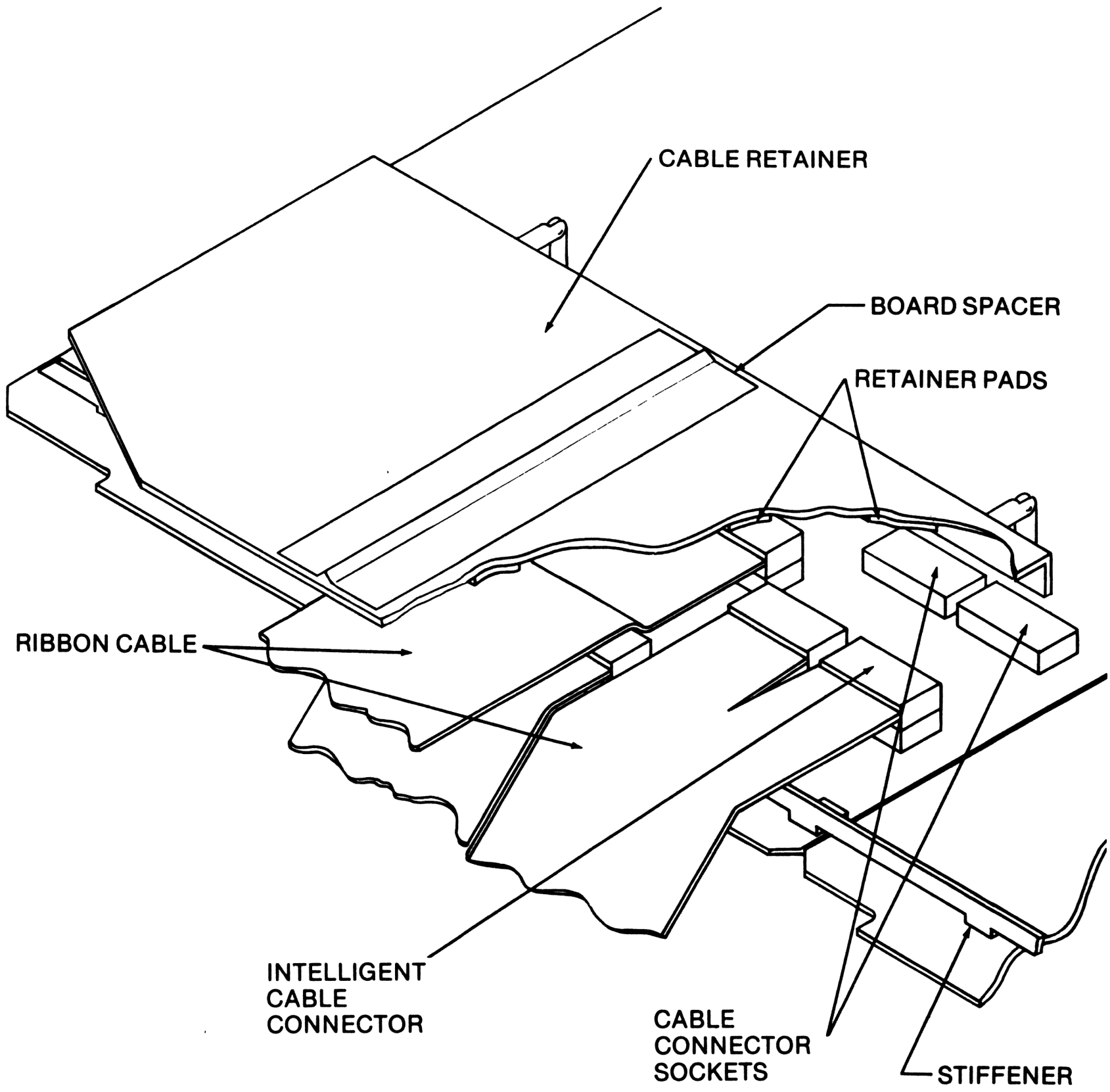


9-11

Figure 4-6. Cable Retainer, Standard I/O Distributor 14629, Revisions B and above

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9-12

Figure 4-7. Cable Retainer, Standard I/O Distributor, 53701

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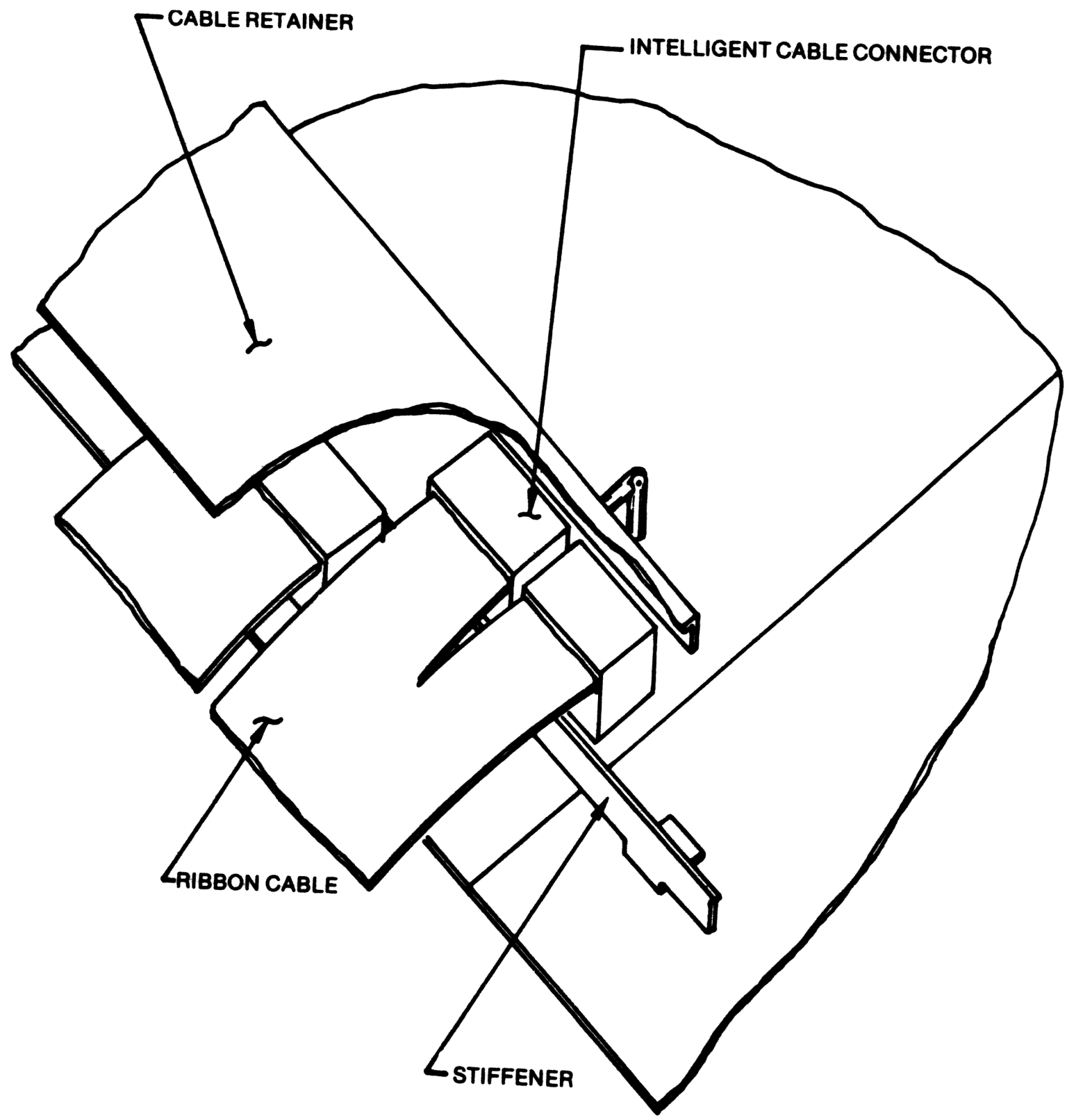


Figure 4-8. Cable Retainer, DMA I/O Distributor, 14674 (shown joined to another half-card)

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4.4.3 Standard I/O Distributor, 53701, and DMA I/O Distributor, 14674, Half-Card Chassis

The DMA I/O Distributor and the standard I/O Distributor, 53701, are both shipped with a hinged cable retainer assembled to the circuit card. Refer to Figures 4-7 and 4-8, respectively. These I/O Distributors are prepared for installation as follows.

1. Remove the screw securing the outer edge of the cable retainer. Pivot the cable retainer on the hinges to expose the channel connectors.

2. Install two circuit card ejectors on the I/O Distributor (if required) using the split pins provided. Position the ejectors so the short arms extend beyond the sides of the circuit board.

3. Plug the I/O Distributor end of the Intelligent Cables into the desired channel connectors.

4. Pivot the cable retainer down over the Intelligent Cable connectors. Replace the screw removed in Step 1. The I/O Distributor is now ready for installation in a half-card chassis.

NOTE

On the 53701 I/O Distributor, the front foam blocks inside the retainer cover must be removed when one cable is passed on top of a cable mounted in front of it.

4.4.4 I/O Distributor Location, Full-Card Chassis

When the I/O Distributor is installed in a full card chassis, the half-card width I/O Distributor must be joined to another half-card device or a filler half-card to produce the required full-card width. The chassis location and choice of mating device must also conform to the requirements listed here.

- Any I/O Distributor can be joined, as the 200 side, to a half-card processor. The assembled full-card must be installed in slot A of the computer (not expansion) chassis.

- The standard I/O Distributors can be joined, as the 100 side, to a half-card memory, DMA controller, or DMA I/O Distributor. The assembled full-card can be installed in any slot except A in the computer chassis or any slot in the expansion chassis.

- The DMA I/O Distributors can be joined, as the 200 side, to a standard I/O Distributor or filler half-card. The assembled full-card can be installed in any slot except slot A in the computer chassis or any slot in the expansion chassis. In D revision level motherboards and above, the DMA I/O Distributors can be inserted in the 100 side, provided the 200 side is completely filled.

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- The standard I/O Distributor, 14629, (all revisions) can be joined to either side of a filler half-card. The 14629 standard I/O Distributor cannot be joined to another 14629 I/O Distributor. A stiffener bar for this purpose is not available. The 14629 I/O Distributor can be joined to a 53701 standard I/O Distributor, or, as noted above, a DMA I/O Distributor. The assembled full-card can be installed in any slot except slot A in the computer chassis or any slot in the expansion chassis.

- The standard I/O Distributor, 53701, can be joined to either side of a filler half-card, DMA, or other standard I/O Distributor, 53701 or 53629. The assembled full-card can be installed in any slot except slot A in the computer chassis or any slot in the expansion chassis.

4.4.5 Standard I/O Distributor, 14629, Revision A, Full-Card Chassis

The standard I/O Distributor installation kit for a full-card chassis is a universal kit. It allows assembly of the full-card with the standard I/O Distributor on either the 100 or 200 side of the chassis. This kit contains all necessary hardware for joining two half-cards together, including two combination stiffener bars. One end of each bar is combined with an Intelligent Cable retainer/strain relief. Prepare the standard I/O Distributor for installation as follows:

1. Determine to which side of the standard I/O Distributor the second half-card is to be attached. To this side of the standard I/O Distributor, attach the tapped plastic mounting blocks using the nylon screws. Do not fully tighten these screws. The mounting blocks must be on the component side of the circuit card.

2. Select one of the stiffener bars provided. Attach this stiffener bar to the component side of the standard I/O Distributor at the channel connector end with the hardware provided. Do not fully tighten these screws. The portion of the stiffener bar attached to the standard I/O Distributor must be the end with the Intelligent Cable retainer/ strain relief. The unattached end of the stiffener bar must be on the same side of the circuit card as the plastic mounting blocks.

3. Attach the second half-card to the mounting blocks (nylon screws) and the stiffener bar. Fully tighten all screws.

4. Install the two circuit card ejectors at the outside edges of the assembled full-card using the split pins provided. Position the ejectors so the short arms extend beyond the sides of the assembled full-card.

5. When the standard I/O Distributor is attached to a half-card processor, install the flat ribbon cable jumper (provided with the processor) between J1 on the standard I/O Distributor and the adjacent connector on the processor.

6. Plug the I/O Distributor end of the Intelligent Cables into the desired channel connectors.

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7. Ensure that the ribbon cables on the outer row of Intelligent Cables are flat and smooth from the connector to the stiffener and the ribbon cables on the inner row of intelligent cables are flat and smooth from the connector, across the outer row of connectors, to the stiffener.

8. Place the cable retainer over all the Intelligent Cables so that all five holes in the cable retainer align with the mating holes in the mounting blocks or stiffener. Attach the cable retainer with the hardware provided. The standard I/O Distributor is now ready for installation in a full-card chassis.

4.4.6 Standard I/O Distributor, 14629, Revisions B and Above, Full-Card Chassis

The standard I/O Distributor installation kit for a full-card chassis comes with a left-handed and right-handed stiffener bar, allowing the Distributor to be placed in the 200 or 100 side of the chassis, respectively. Prepare the Distributor for installation as follows:

1. Determine to which side of the I/O Distributor the second half-card is to be attached.

2. Select the appropriate stiffener bar and attach the horizontal side to the component side of the I/O Distributor board and the vertical side to the filler card. Position the stiffener bar with the raised portion of the horizontal side, containing the threads for the retainer bar, in front.

3. Install the two circuit card ejectors at the outside edges of the assembled full-card using the split pins provided. Position the ejectors so the short arms extend beyond the sides of the assembled full-card.

4. When the standard I/O Distributor is attached to a half-card processor, install the flat ribbon cable jumper (provided with the processor) between J1 on the standard I/O Distributor and the adjacent connector on the processor.

5. Plug the I/O Distributor end of the Intelligent Cables into the desired channel connectors.

6. Ensure that the ribbon cables on the outer row of Intelligent Cables are flat and smooth from the connector to the stiffener and the ribbon cables on the inner row of intelligent cables are flat and smooth from the connector, across the outer row of connectors, to the stiffener.

7. Place the cable retainer over all the Intelligent Cables with the retainer bar edge-flap facing front. Align the bar over the two holes in the stiffener bar and attach with the hardware provided. The Distributor is now ready for installation in a full-card chassis.

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4.4.7 Standard I/O Distributor, 53701, and DMA I/O Distributor, 14674, Full-Card Chassis

The standard I/O Distributor, 53701, and the DMA I/O Distributor are each provided with an installation kit used to join two half-cards together. The procedures are basically identical.

1. On the I/O Distributor, remove the screw securing the outer edge of the cable retainer. Pivot the cable retainer on the hinges to expose the channel connectors.

2. To the right side of the DMA I/O Distributor, attach the tapped plastic mounting blocks using the nylon screws. On the 53701 I/O Distributor, the mounting blocks may be on either side of the board, depending on which side of the chassis the Distributor is being mounted in. Do not fully tighten these screws. The mounting blocks must be on the component side of the circuit card.

3. Attach the stiffener bar to the component side of the I/O Distributor at the channel connector end with the hardware provided. Do not fully tighten these screws. The unattached end of the stiffener bar must be on the right side of the circuit card.

4. Attach the second half-card to the mounting blocks (nylon screws) and the stiffener bar. Fully tighten all screws.

5. Install the two circuit card ejectors at the outside edges of the assembled full-card using the split pins provided. Position the ejectors so the short arms extend beyond the sides of the assembled full-card.

6. When the I/O Distributor is attached to a half-card processor, install the flat ribbon cable jumper (provided with the processor) between J1 on the DMA I/O Distributor and the adjacent connector on the processor.

7. Plug the I/O Distributor end of the Intelligent Cables into the desired channel connectors.

8. Make sure the Intelligent Cable ribbon cable is smooth from the connector to over the stiffener bar.

9. Pivot the cable retainer down over the Intelligent Cable connectors. Replace the screw removed in Step 1. The I/O Distributor is now ready for installation in a full-card chassis.

NOTE

On the 53701 I/O Distributor, the front foam blocks inside the retainer cover must be removed when one cable is passed on top of a cable mounted in front of it.

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