

ACU MULTIPLEXER USER'S MANUAL

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NAKED MINI Division

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REVISION HISTORY

<u>Revision</u>	<u>Issue Date</u>	<u>Comments</u>
A0	August 1974	Original Issue
B0	March 1978	Complete re-write incorporating NAKED MINI 4 compatibility.
B1	December 1978	Miscellaneous revisions.

PREFACE

The ACU Multiplexer Reference Manual contains a description of the controller module used to interface Automatic Calling Units to ALPHA LSI Series and NAKED MINI® 4 Family computers.

In addition to a system functional description, programming and installation sections are included. The programming section describes separately the ALPHA LSI Series and the NAKED MINI® 4 Family I/O commands used to communicate with the ACU Multiplexer. The installation section includes information on the basic system configuration, and device address and interrupt address settings.

The ACU Multiplexer Reference Manual assumes a familiarity with the applicable Computer Automation, Inc., Computer Reference Manual and the MAXI-BUS interface. The information in this manual corresponds to an ACU Multiplexer (73-53747), revision level B, and marketing number 45015. An ACU Multiplexer (73-53523) corresponds to marketing number 14523.

Related Documents:

- 20400-91 LSI-2 Series Minicomputer Handbook
- 10005-91 LSI-3/05 Series Millicomputer Handbook
- 20990-91 LSI 4/10 Computer Reference Manual
- 20991-91 LSI 4/30 Computer Reference Manual
- 20945-91 LSI 4/90 Computer Reference Manual

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Automatic Calling Unit (ACU) Multiplexer is a communications module that interfaces any NAKED MINI® 4 or ALPHA LSI Series computer to a maximum of four Automatic Calling Units. The ACU Multiplexer meets EIA and CCITT interface standards.

The ACU Multiplexer is used typically with other Computer Automation interface modules, such as Asynchronous Modem Multiplexers and Asynchronous or Synchronous Modem Controllers.

The ACU Multiplexer features:

- Full-digit buffering for each Automatic Calling Unit.
- Data Line Occupancy sensing for each Automatic Calling Unit.
- Three separate interrupt vectors for each Automatic Calling Unit.
- Programmed Input/Output or Automatic I/O operation.
- Diagnostic loop-back testing capability without an Automatic Calling Unit attached to the line.
- Simultaneous operation of up to four Automatic Calling Units.

The ACU Multiplexer is available in two models: model 45015-02 interfaces up to two Automatic Calling Units and model 45015-04 interfaces up to four Automatic Calling Units. This manual is applicable to both models.

1.2 SYSTEM DESCRIPTION

The ACU Multiplexer supports up to four Automatic Calling Units simultaneously. Any particular system can have several ACU Multiplexers in use with other communications system components. Figure 1-1 illustrates one possible system configuration with a NAKED MINI® 4 or ALPHA LSI Series computer, a Synchronous Modem Controller, and an Asynchronous Modem Multiplexer.

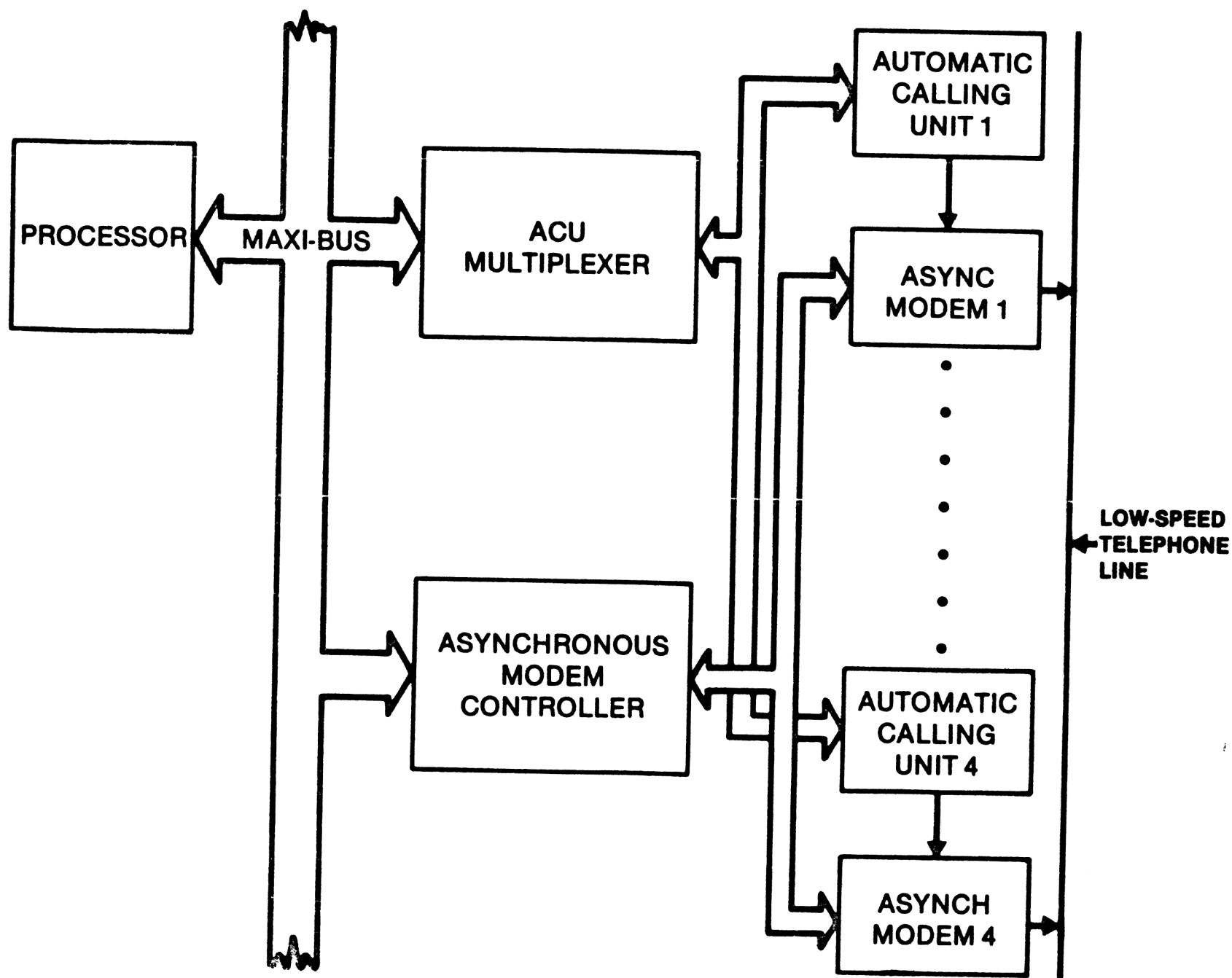


Figure 1-1. Communication's System Configuration

1.3 SPECIFICATIONS

Logic Levels

I ACU Multiplexer to or from Automatic Calling Unit . . . RS232C/CCITT V.24
Compatible

Power Requirements

+5 Vdc	1200 mA
+12 or +15 Vdc	300 mA
-12 or -15 Vdc	300 mA

Environmental Requirements

Temperature	0°C to +50°C operating -20°C to +100°C non-operating
Humidity	5% to 90% relative, non-condensing

I Standard Device Address :0C

Mating Interface Connector Viking 3VH50/1JH5
or Equivalent

SECTION 2

FUNCTIONAL DESCRIPTION

The ACU Multiplexer is a half-card device that communicates with the processor via the MAXI-BUS interface. Data output is processed under interrupt control. The ACU Multiplexer interfaces to each Automatic Calling Unit directly.

2.1 CONTROLLER MODULE

The logic of the ACU Multiplexer is comprised of the MAXI-BUS interface logic, Automatic Calling Unit control logic, interrupt logic, and digit control logic. The logic for both models of the ACU Multiplexer is very similar. Figure 2-1 shows a block diagram of model 45015-04 which interfaces up to four Automatic Calling Units.

2.1.1 Instruction Decode and Device Control

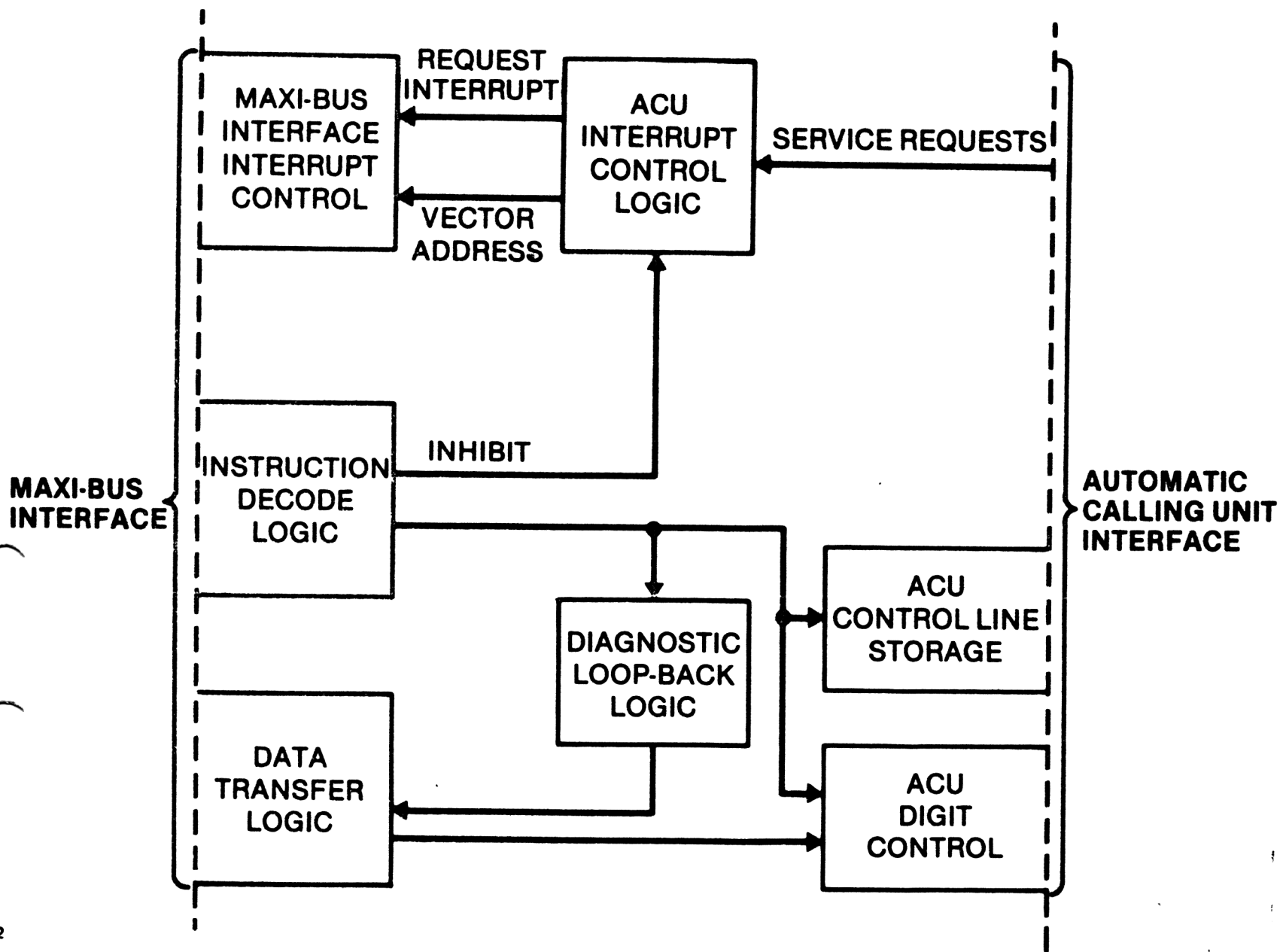
All operations of the ACU Multiplexer are directed by instructions executed by the processor. An instruction is accepted by the module when the device address, output as part of the instruction, matches the device address assigned to the controller module. The ACU Multiplexer instruction decode logic is prefigured by the wiring of the device address connector pins. Section 4 explains the selection of a device address. When the ACU Multiplexer module recognizes its device address in the device address compare logic, it decodes and stores the instruction op code and function code. The operational response of a module to each of the instruction op codes and function codes is detailed in Section 3.

NOTE

Be sure the ACU Multiplexer programming uses only the instruction set detailed in Section 3. The ACU Multiplexer fully decodes its instruction set. Other instructions, output with the ACU Multiplexer device address, may be partially decoded and the resulting operation is unpredictable.

2.1.2 Interrupt Control and Status

The ACU Multiplexer module operates under interrupt-initiated programming. Three control signals from each Automatic Calling Unit provide three different status responses: Abandon Call and Retry, Data Set Status, and Present Next Digit. These three signals cause interrupts to be requested. In addition, the Data Line Occupied signal indicates the condition of the data line.



15-2

Figure 2-1. ACU Multiplexer Block Diagram

The Abandon Call and Retry signal causes the ACU Multiplexer to generate an interrupt request which informs the processor that the timer in the selected Automatic Calling Unit has timed out. This time-out can result from various causes, such as a busy signal, no dial tone, wrong number, or no processor response to a Present Next Digit signal. The Automatic Calling Unit is strapped normally to stop timing when the Data Set Status signal becomes true.

The Data Set Status signal indicates to the ACU Multiplexer that the data set is in data mode. This causes an interrupt request to be generated. This status indicates normally that the Automatic Calling Unit has completed the dialing, an answer condition exists, and the data set is ready to transmit data.

The Present Next Digit signal causes the ACU Multiplexer to generate an interrupt request which informs the processor that the selected Automatic Calling Unit is ready to accept a digit. The processor then executes an output command to send the next digit to the ACU Multiplexer. After the ACU Multiplexer has stored this digit it signals the selected Automatic Calling Unit, via the Digit Present signal, that this digit is available to the ACU. The Digit Present signal remains on the line for at least 1.5 microseconds after the digit lines are established.

The Data Line Occupied signal is an indication to the ACU Multiplexer that the telephone line associated with the selected Automatic Calling Unit is in use, or the Automatic Calling Unit is in test mode. The status of this signal determines whether a Call Request signal can be issued for the selected Automatic Calling Unit. The ACU Multiplexer cannot generate interrupt requests unless a Call Request was initiated. Only interrupt requests relative to Automatic-Calling Units having Call Request in process are generated.

The Interrupt control and status logic of the ACU Multiplexer includes a set of vector address pin strappings to allow the assignment of interrupt vector addresses to the module. Section 4 explains the selection of these addresses. A vector address is issued to the processor in response to the processor recognizing the interrupt request of the module. The interrupt control and status logic also controls the End-of-Block operation required for compatibility with Auto I/O instructions. When terminating conditions are detected, the ACU Multiplexer disables data interrupts, increments the vector address by four, and issues an interrupt (End-of-Block) to the processor. Once the interrupt (End-of-Block) is serviced, the ACU Multiplexer does not issue any further interrupt requests for that line until interrupts for that line are re-enabled by software command.

2.1.3 Digit Control

The Digit Control logic interfaces the ACU Multiplexer data lines to the Data Bus lines on the MAXI-BUS interface. Acceptance of data from the MAXI-BUS interface is determined by the instruction decode logic. Digit Control logic is used as interim storage for transferring digits from the processor to the Automatic Calling Unit.

2.1.4 Diagnostic Loop-back

The Diagnostic Loop-back provides the capability of testing the function codes and the two most significant bits of the digit registers.

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SECTION 3

PROGRAMMING

The ACU Multiplexer conforms to the general I/O programming philosophy presented in the computer reference manuals. The ACU Multiplexer accepts the standard I/O instructions for both the ALPHA LSI and NAKED MINI® 4 Family computers. Select instructions direct the operation of the ACU Multiplexer, while Sense instructions determine the status.

The detailed programming and operating information in the following paragraphs describes separately the I/O commands for the ALPHA LSI and NAKED MINI® 4 Family used to communicate with the ACU Multiplexer. The I/O commands for ALPHA LSI Family computers are identical for models 14523 and 45015.

3.1 DEVICE AND INTERRUPT ADDRESSES

All I/O commands issued to the ACU Multiplexer must be accompanied by the device and interrupt addresses (DEVAD and INTAD in the following descriptions) assigned to the ACU Multiplexer line. Each ACU Multiplexer channel has an individual device and interrupt address determined by the base addresses assigned to the ACU Multiplexer and the line. Once the base device and interrupt addresses are selected on the controller board (refer to Section 4), the same addresses must be established in software. The EQU directive can be used to establish the assigned addresses as conveniently used mnemonics.

ADBAS EQU Device address base determined from system installation information

Assuming the standard device address :0C, then

ADBAS EQU :0C

INTBAS EQU Interrupt address base determined from system installation information

Assuming the base interrupt address :60, then

INTBAS EQU :60

In addition, each Automatic Calling Unit has a line assignment that is one less than the physical line number. The EQU directive is also used to establish the line assignment as a conveniently used mnemonic.

Assuming Automatic Calling Unit 2 is in use, then

ACLN2 EQU :1

The final device address then is established as a mnemonic using the EQU directive to combine the base device address and the line assignment.

Assuming Automatic Calling Unit 2 is in use, then

```
DEVAD EQU ADBAS%2+ACLN2%1
```

First, the base device address is shifted left two bits; then, the line assignment number is added and the complete device address is shifted left one bit to align the device address properly with the I/O instruction format.

The interrupt address is established as a mnemonic using the EQU directive to combine the base interrupt address and the line assignment.

Assuming Automatic Calling Unit 2 is in use, then

```
INTAD EQU ACLN2%3+INTBAS
```

First, the line number is shifted left three bits to align the line number properly with the vector address base. Then the line number is added to the base interrupt address to form the complete vector address.

3.2 INPUT/OUTPUT COMMAND DESCRIPTION (ALPHA LSI FAMILY)

The I/O command descriptions are presented in assembly language format for easy use. The label (if used), mnemonic, and operand with appropriate function code appears for each command. The commands used to communicate with the ACU Multiplexer are the following:

SEN	Sense and Skip on Response
SSN	Sense and Skip on No Response
SEL	Select
OTA	Output A Register
OTX	Output X Register
AOT	Automatic Output Word

3.2.1 Sense Instruction

The Sense instruction is used to determine the present status of the ACU Multiplexer. One function code is used with the Sense instruction.

To sense Data Line Occupied, use function code 0 in the form

```
SEN DEVAD+0
```

The true response (skip next instruction) indicates that the Data Line Occupied signal is on (i.e., either a call origination is in process or the Automatic Calling Unit has transferred the line to the associated data set and data transmission is in process).

The SSN instruction may be used in place of SEN, with the same function code, to invert the skip condition.

3.2.2 Select Instruction

The Select instruction is used to initialize the ACU Multiplexer line interface and to signal the appropriate Automatic Calling Unit with a Call Request. Two function codes are used with the Select instructions.

The Select initialize instruction is used by software to clear the Call Request line after an Abandon Call and Retry or Data Set Status interrupt.

To select initialize, use function code 0 in the form

SEL DEVAD+0

The Select call request instruction causes the ACU Multiplexer to signal the appropriate Automatic Calling Unit with a call request.

To select call request, use function code 1 in the form

SEL DEVAD+1

3.2.3 Output Instructions

All output data transfers must be carried out using unconditional output instructions or Auto I/O instructions under interrupt control. The Output A or Output X register (OTA or OTX) instruction is used to transfer a data word to the ACU Multiplexer which, in turn, presents the digit to the selected Automatic Calling Unit. A single function code is used with the output instruction.

To output A- or X-register contents, use function code 0 in the form

OTA DEVAD+0

or

OTX DEVAD+0

To use Auto I/O under interrupt control, use function code 0 in the form

ABS	INTAD+4	DATA SERVICE INTERRUPT VECTOR ADDRESS
AOT	DEVAD+0	
DATA	\$-\$	FILL WITH NEGATIVE TRANSFER COUNT
DATA	\$-\$	FILL WITH BUFFER ADDRESS-1

The Auto I/O routine uses the Data Set Status interrupt address as the location for the End-of-Block routine required for Auto I/O operation. The End-of-Block routine is set up in the form

ABS	INTAD+2	DATA SET STATUS INTERRUPT VECTOR ADDRESS
JST	*\$+1	
DATA	EOB	ADDRESS OF END-OF-BLOCK ROUTINE

Figure 3-1 illustrates the format of the register contents output to the ACU Multiplexer.

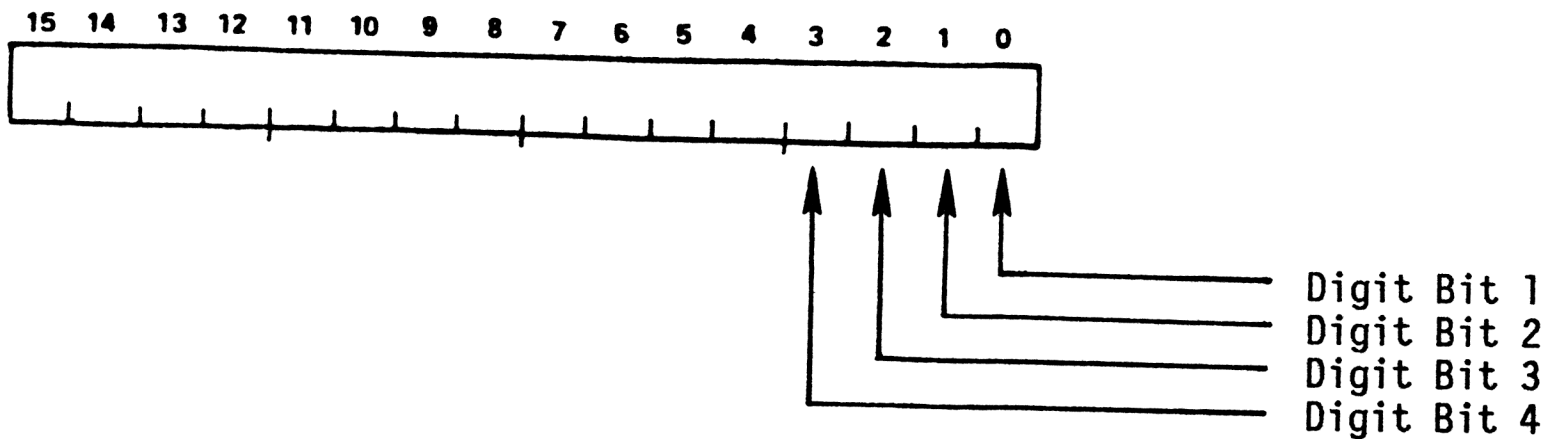


Figure 3-1. Output Data Word Format

3.3 INPUT/OUTPUT COMMAND DESCRIPTION (NAKED MINI® 4 FAMILY)

The I/O command descriptions are presented in assembly language format for easy use. The label (if used), mnemonic, and operand, with appropriate function code, appears for each command. The commands used to communicate with the ACU Multiplexer are the following:

SELP	Select and Present
SST	Sense and Skip True
OUT	Output Register
AOT	Automatic Output Word
UIS	Update Interrupt Status

3.3.1 Sense and Skip Instruction

The Sense and Skip instruction is used to determine the present status of the ACU Multiplexer. One function code is used with the Sense and Skip instruction.

To sense Data Lines Occupied, use function code 0 in the form

SST DEVAD+0

The true response (skip next instruction) indicates that the Data Line Occupied signal is on (i.e., either a call origination is in process or the Automatic Calling Unit has transferred the line to the associated data set and data transmission is in process).

3.3.2 Select and Present Instruction

The Select and Present instruction is used to initialize the ACU Multiplexer line interface and to signal the appropriate Automatic Calling Unit with a Call Request. Two function codes are used with the Select and Present instructions. The register specification in the following instructions serve to maintain syntactically correct operand structure. The register contents are ignored by the ACU Multiplexer.

The Select initialize instruction is used by software to clear the Call Request line after an Abandon Call and Retry or Data Set Status interrupt.

To select initialize, use function code 0 in the form

SELP R,DEVAD+0 (R=A,X,Q, or Y Register)

This command must precede the Select and Present instruction for Call Request.

The Select call request causes the ACU Multiplexer to signal the appropriate Automatic Calling Unit with a call request.

To select call request, use function code 1 in the form

SELP R,DEVAD+1 (R=A,X,Q,or Y Register)

3.3.3 Update Interrupt Status Instruction

The UIS instruction is used to transfer the present state of the IOI (Data) and EI (Event) status register bits to all I/O controllers in the system. These two status register bits are also presented by the processor and stored by the system I/O controllers each time an interrupt is acknowledged by the processor. The ACU Multiplexer stores the EI bit only.

In the ACU Multiplexer, when the EI bit is stored as a 0, the ACU Multiplexer interrupts are enabled; when stored as a 1, the ACU Multiplexer interrupts are disabled. The enabling and disabling of the ACU Multiplexer interrupts using the EI bit is separate from enabling and disabling of the ACU Multiplexer interrupts controlled by the command I/O block.

3.3.4 Output Instructions

All output data transfers must be carried out using Programmed I/O instructions or Auto I/O instructions under interrupt control. The Output register (OUT) instruction is used to transfer a data word to the ACU Multiplexer which, in turn, presents the digit to the selected Automatic Calling Unit. A single function code is used with the Output instruction.

To Output the contents of one of the four registers, use function code 0 in the form

OUT R,DEVAD+0 (R=A,X,Q, or Y Register)

To use Auto I/O under interrupt control, use function code 0 in the form

ABS	INTAD+4	DATA SERVICE INTERRUPT VECTOR ADDRESS
AOT	DEVAD+0	
DATA	\$-\$	FILL WITH NEGATIVE TRANSFER COUNT
DATA	\$-\$	FILL WITH BUFFER ADDRESS-1

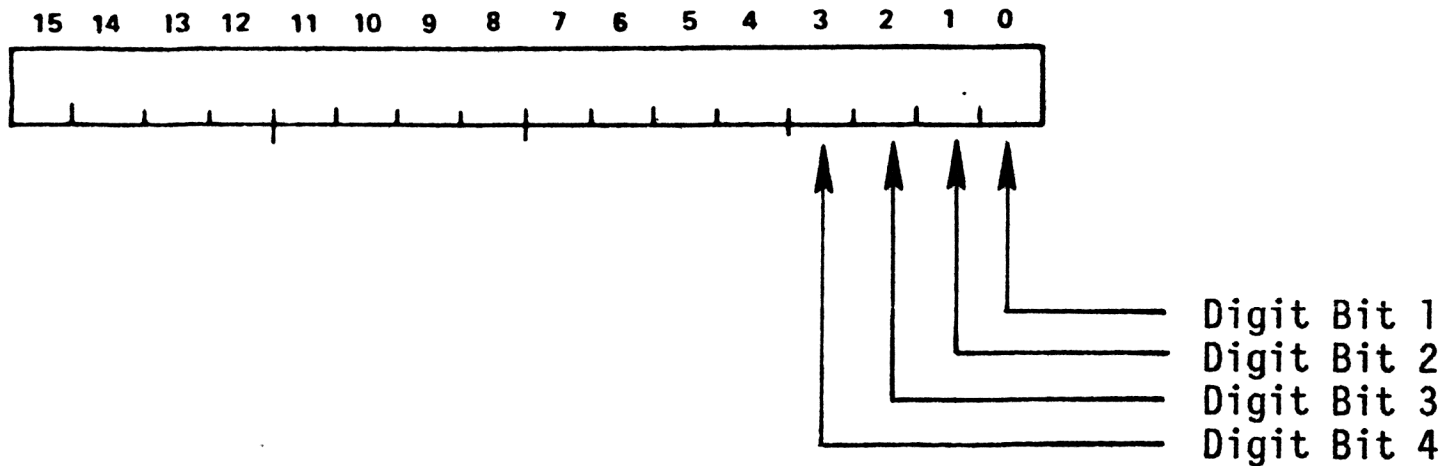


Figure 3-2. Output Data Word Format

The Auto I/O routine uses the Data Set Status interrupt address as the location for the End-of-Block routine required for Auto I/O operation. The End-of-Block routine is set up in the form

ABS	INTAD+2	DATA SET STATUS INTERRUPT VECTOR ADDRESS
JST	*\$+1	
DATA	EOB	ADDRESS OF END-OF-BLOCK ROUTINE

Figure 3-2 illustrates the format of the register contents output to the ACU Multiplexer.

3.4 INTERRUPT VECTORING

The ACU Multiplexer issues interrupt requests to the processor. Once the interrupt is recognized, the ACU Multiplexer must then provide a memory address to the computer for use as the next instruction address. This process is called interrupt vectoring.

Each Automatic Calling Unit line is able to provide three different interrupt vector addresses. The first address is provided upon the status of the Abandon Call and Retry signal. A second is provided upon the status of the Data Set Status signal, and a third address is provided when the Data Service signal is encountered.

The actual addresses provided by the ACU Multiplexer are controlled by the ACU Multiplexer hardware. The following conventions determine the hardware assignment of the interrupt vector address:

- The interrupt vector addresses are assigned within a block of 32 consecutive memory addresses.
- Each Automatic Calling Unit line is allocated eight consecutive memory addresses.
- An interrupt for Abandon Call and Retry is vectored to the line low order memory address.

- An interrupt for Data Set Status is vectored to the line low order memory address plus two.
- An interrupt for Data Service is vectored to the line low order memory address plus four.
- The location of the 32-cell address block is selectable by strapping on the ACU Multiplexer.

Figure 3-3 shows all the interrupt vector addresses for the 32-cell address block selected if four Automatic Calling Unit lines interface to the ACU Multiplexer. This block starts at memory address :60 and goes through address :7F.

Figure 3-3 shows the format of the eight consecutive memory addresses for line one. The format for the remaining lines is the same. If the ACU Multiplexer is strapped for a different vector address block (refer to Section 4 for details on strapping), the vector addresses would be changed. Each vector address in the new block would have the same relationship to the new low order memory address as the relationship shown in Figure 3-3.

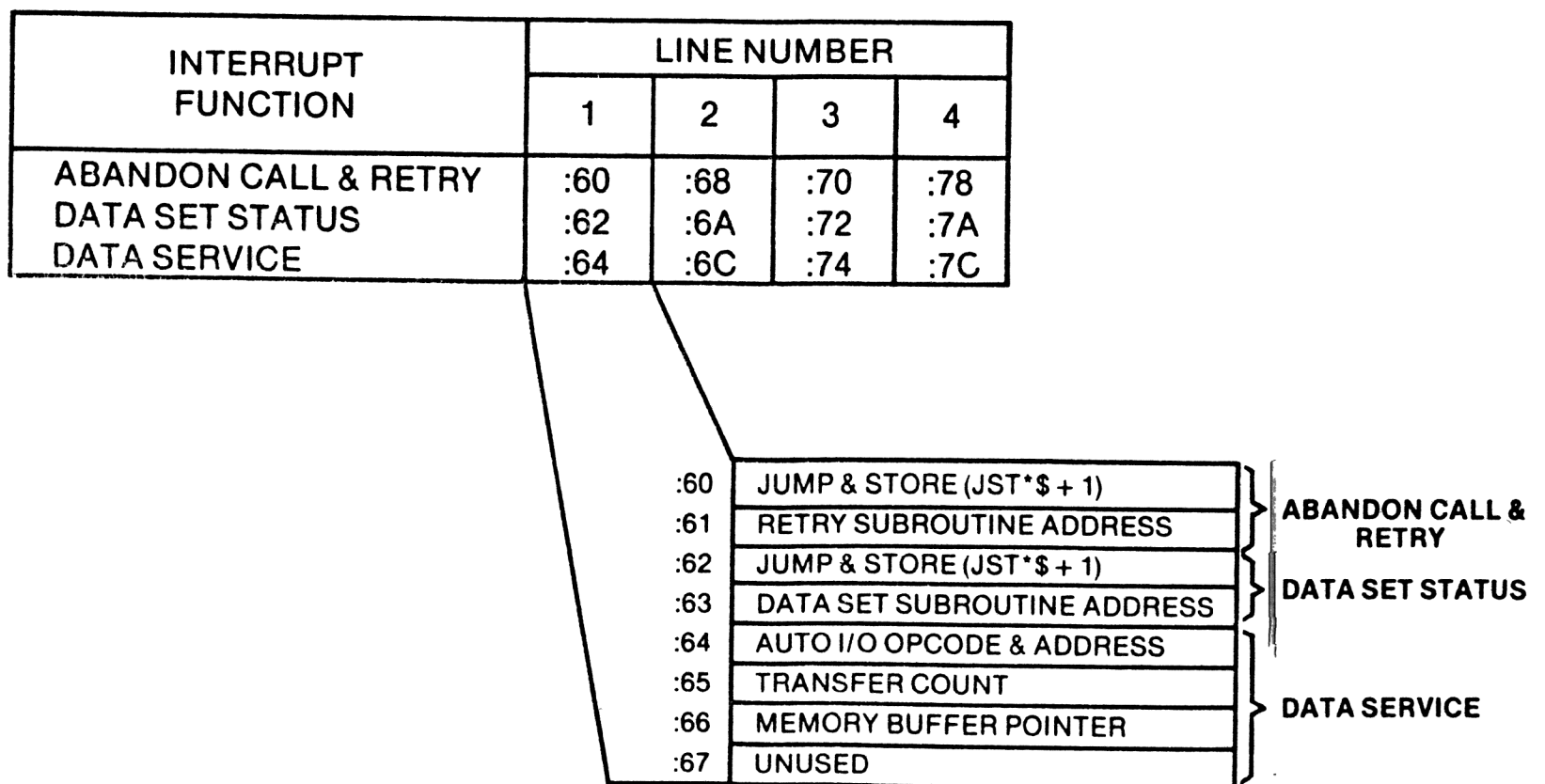


Figure 3-3. ACU Multiplexer Interrupt Vector Addresses

SECTION 4

INSTALLATION

This section describes the installation considerations unique to the ACU Multiplexer. For a description of the standard installation procedures, refer to the installation section of the appropriate computer reference manual.

4.1 SYSTEM CONFIGURATION

The ACU Multiplexer is a single half-card device that can be inserted in any half-card slot motherboard I/O connector. The interrupt priority of the ACU Multiplexer is established by the motherboard connector location.

Care should be taken to ensure that the priority chains between the ACU Multiplexer and the processor are not broken. All cards located between the processor and the ACU Multiplexer must provide propagation of the priority chains and, in turn, the ACU Multiplexer propagates all MAXI-BUS interface priority chains. No open slots can exist between the ACU Multiplexer and the processor or the chain will be broken.

4.2 ADDRESS ASSIGNMENTS

The ACU Multiplexer must be assigned both a base interrupt vector address and a base device address before it is integrated physically into the computer system. All jumper connections are made using AWG24 to 28 solid wire (metric gauge three to five) and soldered connections.

4.2.1 Device Address Assignment

The ACU Multiplexer base device address is selected by grounding a combination of pins (DA00-DA04) on the interface connector. The ACU Multiplexer can be assigned any base device address from :01 through :1F. When assigning a base device address, care must be taken to avoid assigning a device address already in use or a device address dedicated to a specific peripheral or use. Refer to the appropriate computer reference manual for a listing of standard device address assignments and restrictions.

The bit assignments for the device address, along with the pin settings corresponding to the recommended device address, are shown in Figure 4-1. The jumper connections for all 31 possible device addresses are listed in Table 4-1. The table is coded for device address bit values of 0 = grounded pin and 1 = ungrounded pin. The recommended ACU Multiplexer device address for compatibility with Computer Automation software is :0C and is shown shaded in Table 4-1.

Table 4-1. Device Address Jumper Connections

DEVICE ADDRESS	PIN B03	PIN B02	PIN B01	PIN A02	PIN A01		DEVICE ADDRESS	PIN B03	PIN B02	PIN B01	PIN A02	PIN A01
:01	0	0	0	0	1		:10	1	0	0	0	0
:02	0	0	0	1	0		:11	1	0	0	0	1
:03	0	0	0	1	1		:12	1	0	0	1	0
:04	0	0	1	0	0		:13	1	0	0	1	1
:05	0	0	1	0	1		:14	1	0	1	0	0
:06	0	0	1	1	0		:15	1	0	1	0	1
:07	0	0	1	1	1		:16	1	0	1	1	0
:08	0	1	0	0	0		:17	1	0	1	1	1
:09	0	1	0	0	1		:18	1	1	0	0	0
:0A	0	1	0	1	0		:19	1	1	0	0	1
:0B	0	1	0	1	1		:1A	1	1	0	1	0
:0C	0	1	1	0	0		:1B	1	1	0	1	1
:0D	0	1	1	0	1		:1C	1	1	1	0	0
:0E	0	1	1	1	0		:1D	1	1	1	0	1
:0F	0	1	1	1	1		:1E	1	1	1	1	0
							:1F	1	1	1	1	1
LEGEND: GROUNDED = 1 UNGROUNDED = 0												

Shaded section :0C is the recommended ACU Multiplexer device address for compatibility with Computer Automation software.

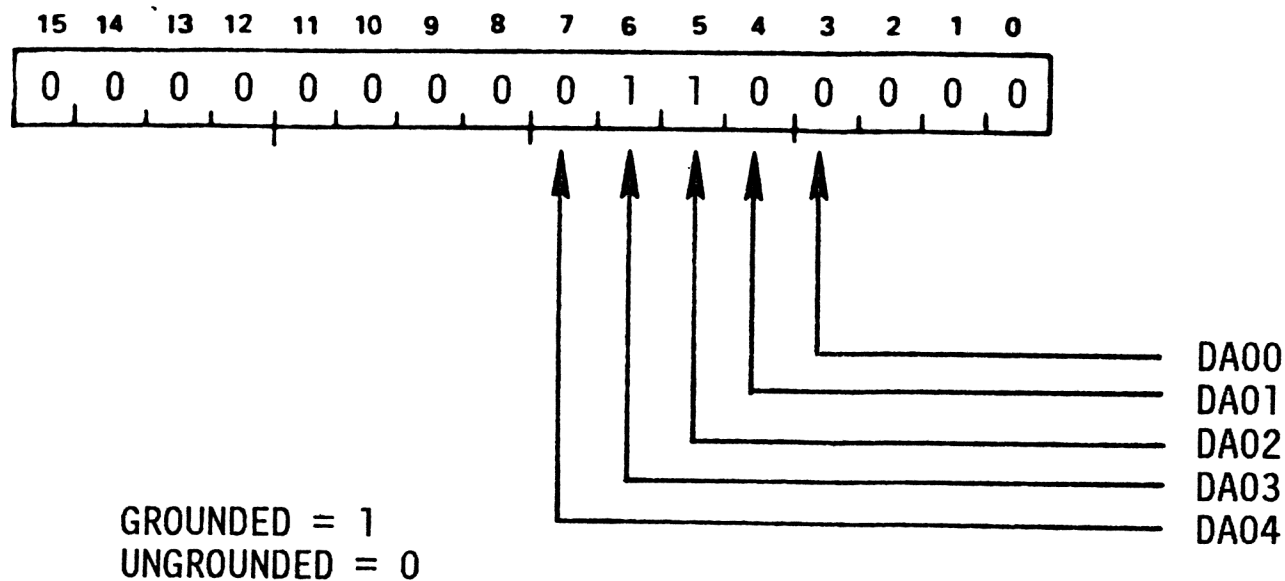


Figure 4-1. Device Address Bit Assignments

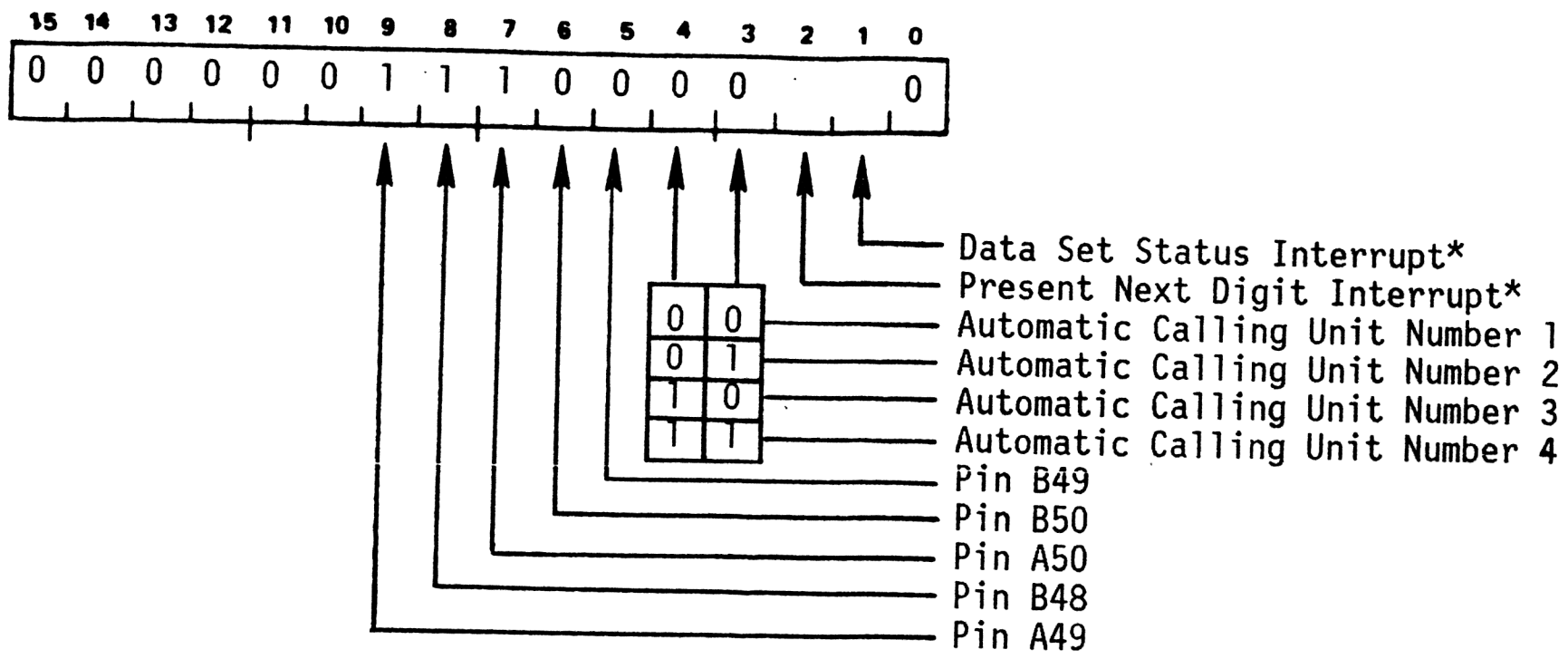
Because the I/O Distributor uses a 4-bit base device address rather than the 5-bit device address used by most other Computer Automation, Inc., I/O controllers, it is necessary to check the absolute value of the device address to be sure a conflict does not occur with other I/O controller device addresses. The software treats the field value of the device address format as an absolute 5-bit value.

4.2.2 Interrupt Vector Address

The ACU Multiplexer is assigned a base interrupt vector address within the first 512 words of memory. Care must be taken to avoid assigning a vector address already in use or dedicated to a specific peripheral or use. Refer to the computer handbook for a listing of standard interrupt vector address assignments and restrictions. The recommended interrupt vector address for compatibility with software is :60. The area of memory dedicated to ACU Multiplexer interrupts must consist of 32 consecutive memory locations starting at the strappable base interrupt vector address location. The ACU Multiplexer standard base interrupt vector address places the interrupt vector offset addresses in locations which are standard vectors for other devices. If these devices are to be used with the same processor as the ACU Multiplexer uses, they must be assigned new interrupt locations or the ACU Multiplexer must be assigned an alternate interrupt base value.

The interrupt vector address is assigned to the ACU Multiplexer by strapping the Address Select pins to a ground on the interface connector. Of the 9-bits required to address 512 words of memory, bits five through nine are selectable by strapping the required base interrupt vector address, bit three and four define the Automatic Calling Unit number, and bit one and two define the type of interrupt. The bit assignments for the strapping elements, along with the pin settings corresponding to the recommended interrupt vector address, are shown in Figure 4-2.

If several ACU Multiplexers interface to the processor, base interrupt vector address assignments should be made such that all I/O interrupts address a continuous block of memory in the order of the assigned line numbers. An ACU Multiplexer with less than four Automatic Calling Units should be assigned the last block of vector address for optimum use of memory. Interface connector pin assignments are shown in Table 4-2.



GROUND = 1
UNGROUND = 0

*If both bit one and two are off, then the Abandon Call and Retry Interrupt is enabled.

Figure 4-2. Interrupt Vector Address Bit Assignments

Revised 12/78



Table 4-2. Interface Connector Pin Assignments

PIN	SIGNAL NAME	PIN	SIGNAL NAME
A01	DA00	A32	DIGIT BIT 3 - OUTPUT 3
A02	DA01	A33	DIGIT BIT 1 - OUTPUT 3
A03	PRESENT NEXT DIGIT - INPUT 1	A34	DIGIT BIT 2 - OUTPUT 3
A04	GROUND	A35	STORED CALL REQUEST - OUTPUT 3
A05	DATA LINE OCCUPIED - INPUT 1	A36	DIGIT PRESENT - OUTPUT 4
A06	ABANDON CALL & RETRY - INPUT 1	A37	DIGIT PRESENT - OUTPUT 3
A07	DATA SET STATUS - INPUT 1	A38	GROUND
A08	DIGIT BIT 3 - OUTPUT 1	A39	REQUEST - OUTPUT 4
A09	DIGIT BIT 4 - OUTPUT 1	A40	DATA SET STATUS - INPUT 4
A10	DIGIT BIT 2 - OUTPUT 1	A41	ABANDON CALL & RETRY - INPUT 4
A11	DIGIT BIT 1 - OUTPUT 1	A42	DIGIT BIT 4 - OUTPUT 4
A12	DIGIT PRESENT - OUTPUT 1	A43	DIGIT BIT 3 - OUTPUT 4
A13	GROUND	A44	DIGIT BIT 1 - OUTPUT 4
A14	CALL REQUEST - OUTPUT 1	A45	DIGIT BIT 2 - OUTPUT 4
A15	CALL REQUEST - OUTPUT 2	A46	DATA LINE OCCUPIED - INPUT 4
A16	DIGIT PRESENT - OUTPUT 2	A47	GROUND
A17	DIGIT BIT 3 - OUTPUT 2	A48	PRESENT NEXT DIGIT - INPUT 4
A18	DIGIT BIT 4 - OUTPUT 2	A49	ADDRESS SELECT 00
A19	DIGIT BIT 2 - OUTPUT 2	A50	ADDRESS SELECT 02
A20	DIGIT BIT 1 - OUTPUT 2	B01	DA02
A21	DATA LINE OCCUPIED - INPUT 2	B02	DA03
A22	GROUND	B03	DA04
A23	PRESENT NEXT DIGIT - INPUT 2	B04	GROUND
A24	DATA SET STATUS - INPUT 2	B13	GROUND
A25	ABANDON CALL & RETRY - INPUT 2	B22	GROUND
A26	PRESENT NEXT DIGIT - INPUT 3	B29	GROUND
A27	DATA SET STATUS - INPUT 3	B38	GROUND
A28	ABANDON CALL & RETRY - INPUT 3	B47	GROUND
A29	GROUND	B48	ADDRESS SELECT 01
A30	DATA LINE OCCUPIED - INPUT 3	B49	ADDRESS SELECT 04
A31	DIGIT BIT 4 - OUTPUT 3	B50	ADDRESS SELECT 03

