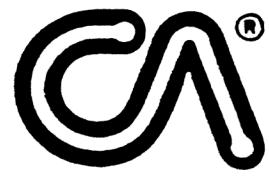
NAKED MINI 4® FAMILY

GENERAL MEMORY REFERENCE MANUAL

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NAKED MINI® Division
18651 Von Karman, Irvine, CA 92713
tel. (714) 833-8830 TWX: (910) 595-1767

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REVISION HISTORY

Revision	Issue Date	Comments
A0	Feb. 1978	Original issue.
A1	Oct. 1978	Incorporates switch SW2 and resistor-pack RP1 modifications for interleaving and sub module 16K and 32K half-card available with 4/10 Processor.
A2	Jan. 1980	Includes a new board, and general revisions.
B0	Sep. 1980	Manual updated to include models 53819 and 53828 memories.
C0	Jan. 1984	General revisions, including addition of 53642 16KB RAM Module and 53909 1 MB Map Memory Module.
D0	Feb. 1984	Adds information on MAXI-BUS® Expandable Memory Board (model 53988).

PREFACE

The NAKED MINI® 4 Family General Memory Reference Manual contains information on core and semiconductor memories for the NAKED MINI® 4 Family computers. Discussions of functional descriptions, specifications, and special installation requirements are included for each type of memory.

In addition, due to the volatile nature of the semiconductor memories and the consequent possibility of data loss related to power interruptions, a Battery Backup section is included. Discussions include types of memories and batteries, charging, battery pack, expansion, and operation hints.

This manual refers to the model numbers for each memory module and Battery Backup module.

The following manuals are also helpful to NAKED MINI® 4 Family users:

	Order No.
NAKED MINI® 4/10, 4/12, and 4/22 Computer Reference Manual	53931-91
LSI 4/30 Computer Reference Manual	20991-91
LSI 4/90 Computer Reference Manual	20945-91
NAKED MINI® 4/Series 5 Principles of Operation Manual	53817-90
Chassis Configuration Reference Manual & Installation Guide	21426-91
NAKED MINI® 4 ROM/PROM Format Generator Manual	93060-90

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SECTION 1

OVERVIEW

1.0 INTRODUCTION

This section gives an overview of the memories, memory options, and battery backup systems covered in this manual.

1.1 MEMORIES

Computer Automation, Inc., produces a wide range of memories which vary both in type and size of memory. The specific type of memory storage used separates the available memory modules into four categories:

1. Core RAM modules
2. Semiconductor RAM modules
3. Semiconductor combination RAM and ROM modules
4. Semiconductor RAM modules with 22-bit addressing

The available memories are shown in Figure 1-1.

1.1.1 Core RAM Modules

The core RAM modules provide the most stable form of memory storage with both read and write capabilities. The integrity of data stored in core memory is retained when power to the memory module is interrupted. Both half card and full card core memory modules are available in a variety of storage capacities. The typical memory cycle time for the full card core memory modules is 850 to 1200 nanoseconds.

1.1.2 Semiconductor RAM Modules

The semiconductor RAM modules usually have a faster memory cycle time than core memories. The memory storage capacity of a semiconductor memory module usually is larger--often double or more--than a core memory module of similar physical size. However, data stored in semiconductor RAM modules is volatile; that is, the data loses its integrity when power to the memory is interrupted. Both half card and full card semiconductor RAM modules are available in a variety of storage capacities.

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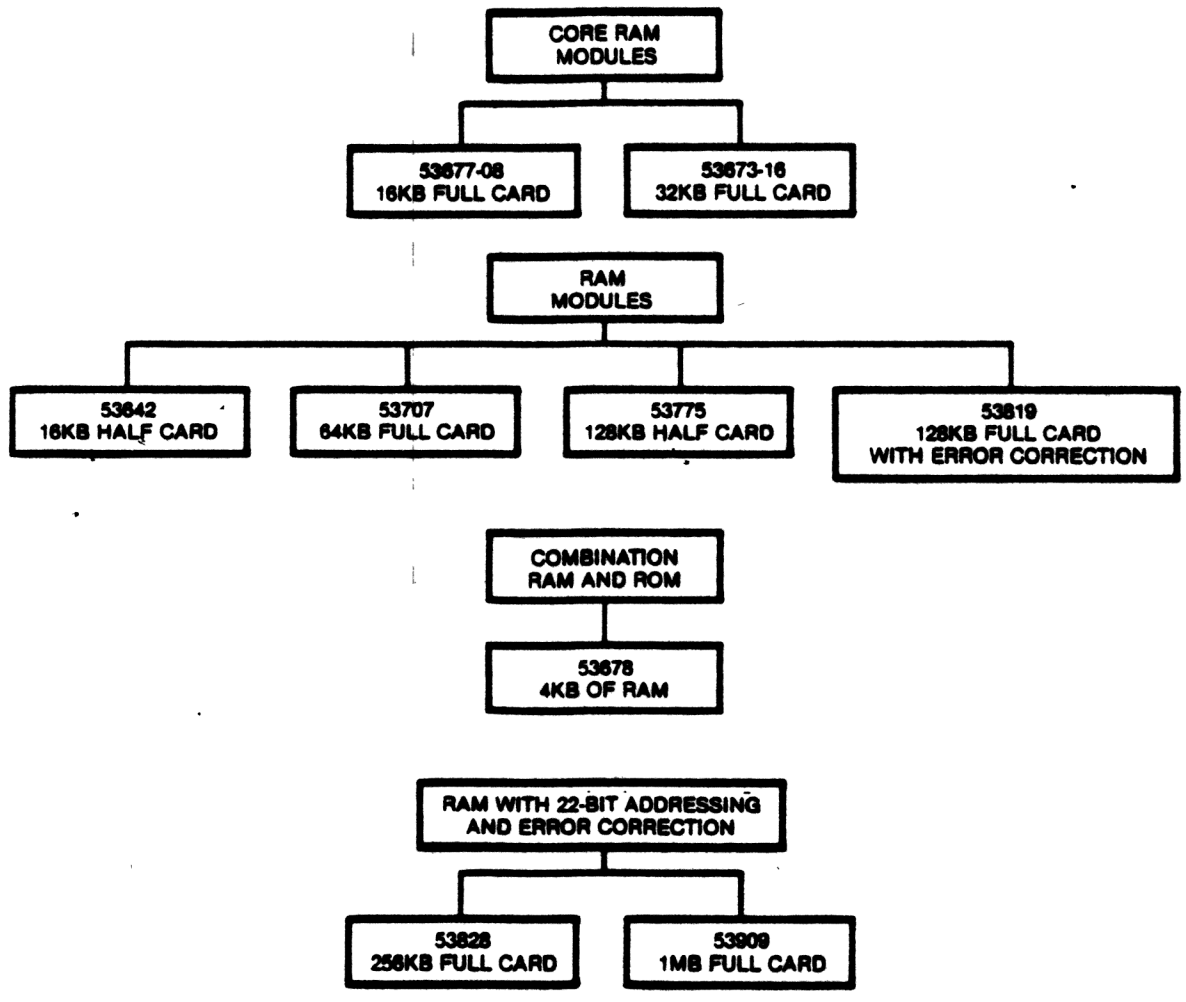


Figure 1-1. Memories

1.1.3 Semiconductor Combination RAM and ROM Modules

The combination memory modules are primarily ROM modules that can be programmed with permanent or very infrequently changed data. These memory modules usually provide for up to 2K words of RAM in addition to the ROM capability. This allows use of a single combination memory module in special purpose, limited memory applications.

The combination memory modules are available in half card modules only. The maximum storage capacity of these modules, both RAM and ROM, is 10K words.

Each different module is restricted to a specific type (or types) of ROM. However, modules are available for the three most popular types of read-only memory:

1. Mask-programmed Read-Only Memory (ROM)
2. Programmable Read-Only Memory (PROM)
3. Ultraviolet Erasable, Programmable Read-Only Memory (EPROM)

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1.1.4 Semiconductor RAM Modules with 22-Bit Addressing

Semiconductor RAM modules with 22-bit addressing and error correction provide up to 8M bytes of addressable memory. The 22-bit modules are built on standard full cards, and must be driven by a 53794 or 53861 Memory Management Unit (MMU). RAM modules with 22-bit addressing also require a split backplane environment, such as a 53822 motherboard (S17 chassis) or a 53940 motherboard (S9 chassis).

1.2 MEMORY FEATURES

Computer Automation, Inc., includes the memory banking and interleaving options with some of the core and semiconductor memory modules. The 53828 and 53909 semiconductor memory modules do not need, and therefore do not have, memory banking or interleaving options.

1.2.1 Memory Banking Option

When the memory banking option is used, the total memory installed in a system can exceed the 128K byte direct addressing limit of the processor. In addition, memory banking enables (makes available) or disables (restricts the availability of) portions of the total memory installed in a system. The integrity of data stored in a disabled portion of memory and the data-transfer timing are not affected by memory banking.

Because of its selective partitioning feature, memory banking is particularly valuable in multiuser applications, wherein individual system users are restricted to a specific portion of memory, or in applications that require large data bases.

The memory banking option is implemented by a controller that supervises the configuration of memory available to the processor. The 32-bit general purpose intelligent cable is one such controller that meets the requirements to serve as a memory banking controller.

Figure 1-2 shows how the 32-bit general purpose intelligent cable fits into the system. The processor, memory, and I/O distributor connect directly with the MAXI-BUS Interface. The 32-bit general purpose intelligent cable receives command signals from the processor via the I/O distributor and generates the enabling signals required to configure the memory subsystem. Once set, the specified memory configuration is retained until the 32-bit general purpose intelligent cable receives a new set of command signals.

Some memory modules are internally partitioned using the sub-module memory banking option.

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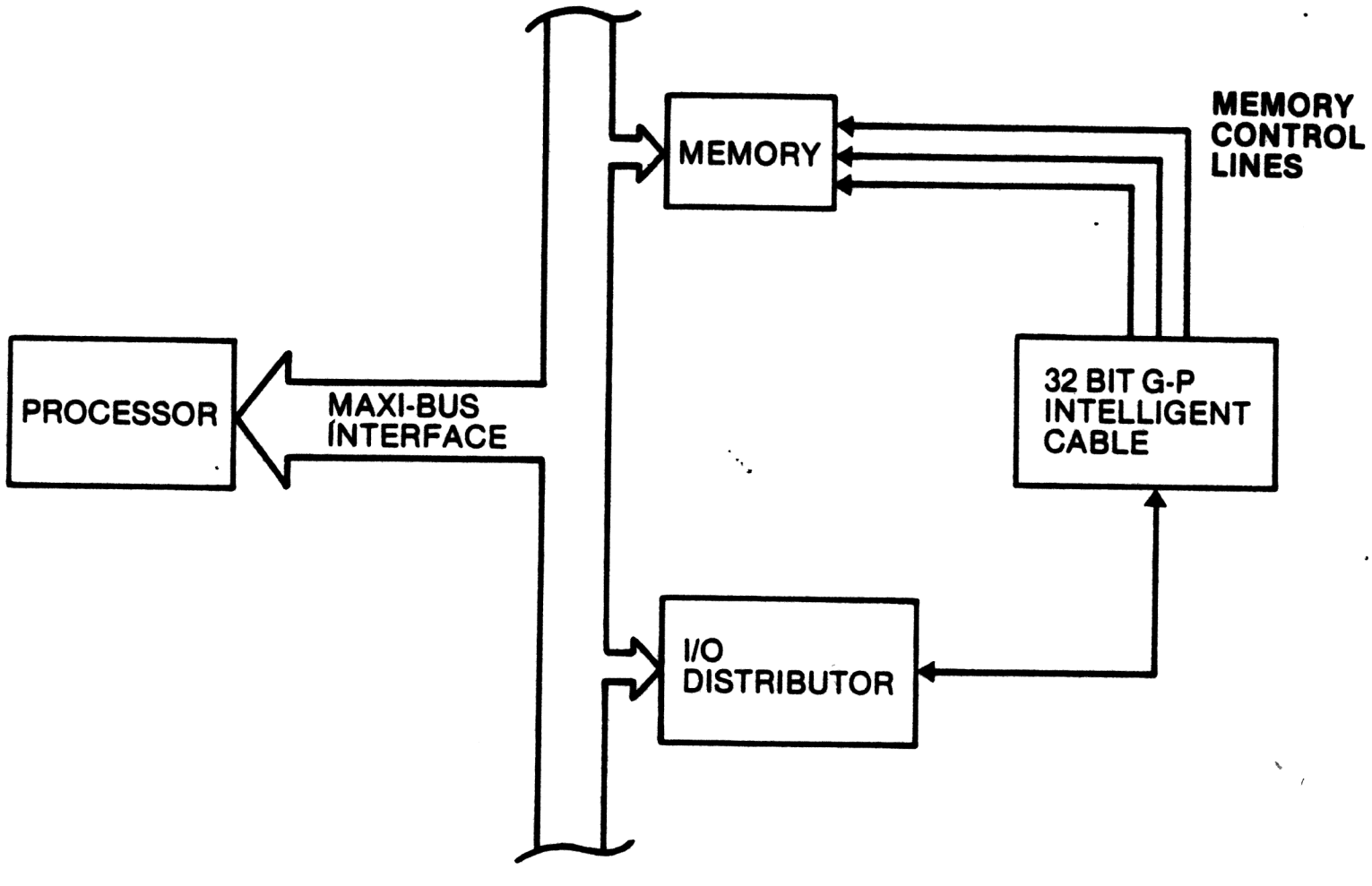


Figure 1-2. Memory Banking System

1.2.2 Memory Module Interleaving

Memory module interleaving is used to decrease the total data transfer time required when blocks of data are being transferred. Single memory transfer times are unaffected by memory module interleaving.

The memory cycle of any memory module can be divided into an access interval and an overhead interval. The access interval is that period of time when data is actually read from or written into memory. The overhead interval is that period of time when the internal logic of the memory module recovers from the access interval. For example, with a core memory read operation, the data is rewritten during the overhead interval.

The memory interleaving feature takes advantage of this memory cycle division to improve data transfer timing. Memory interleaving allows two memory modules to be assigned to the same range of memory addresses. That is, both modules assume the same low limit address. However, one module is strapped to recognize only the even memory addresses and the other is strapped to recognize only the odd addresses. In general, to interleave X words of RAM, use two X/2 word modules. The INTER- and ODD- signals control the module enabling for even and odd memory locations, respectively.

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1.2.2.1 Memory Interleaving Timing

The effect of using memory interleaving is shown by comparing Figures 1-3 and 1-4. Figure 1-3 shows memory cycle timing when interleaving is not used. As shown in the figure, the processor asserts MST- a minimum of 75 nanoseconds after the address on the address bus becomes valid. Asserting MST- initiates the memory access period. The length of the access period, during which data is read from or written into memory, varies with the type of memory. When the access is complete the memory asserts MACK-, indicating to the processor that the bus transfer is complete. The processor then removes MST- and may place the next address on the address bus. This operation may take place in parallel with the RAM 1 overhead period.

The MAXI-BUS Interface imposes the constraint that MST- cannot be reasserted until a minimum of 100 nanoseconds (ns) after MST- is removed. Because the overhead time is longer than 100 ns for all available memories, this constraint does not effect the memory cycles for non-interleaved memories. If the modules are interleaved, and the next access is to a location in the other of the pair of modules, the access can begin once the 100 ns requirement is met. The timing is shown in Figure 1-4. Typically, the time from MACK- to the next MST- is 200 ns. If the memory overhead is longer than this period, interleaving the memories reduces the apparent cycle time by utilizing part of the overhead time. For memories with a shorter overhead period, no improvement is achieved by interleaving.

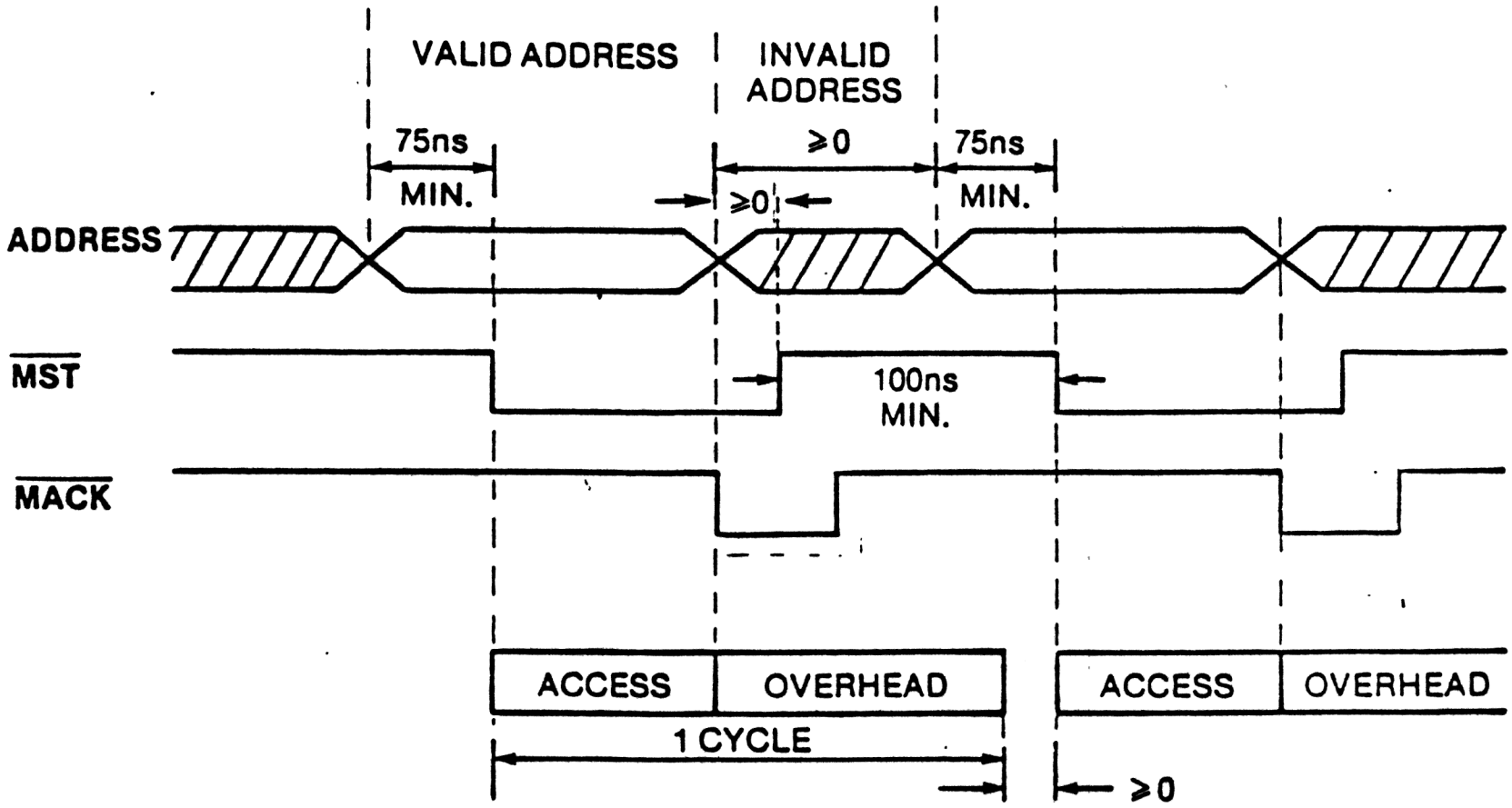


Figure 1-3. Memory Cycle Timing Without Interleaving

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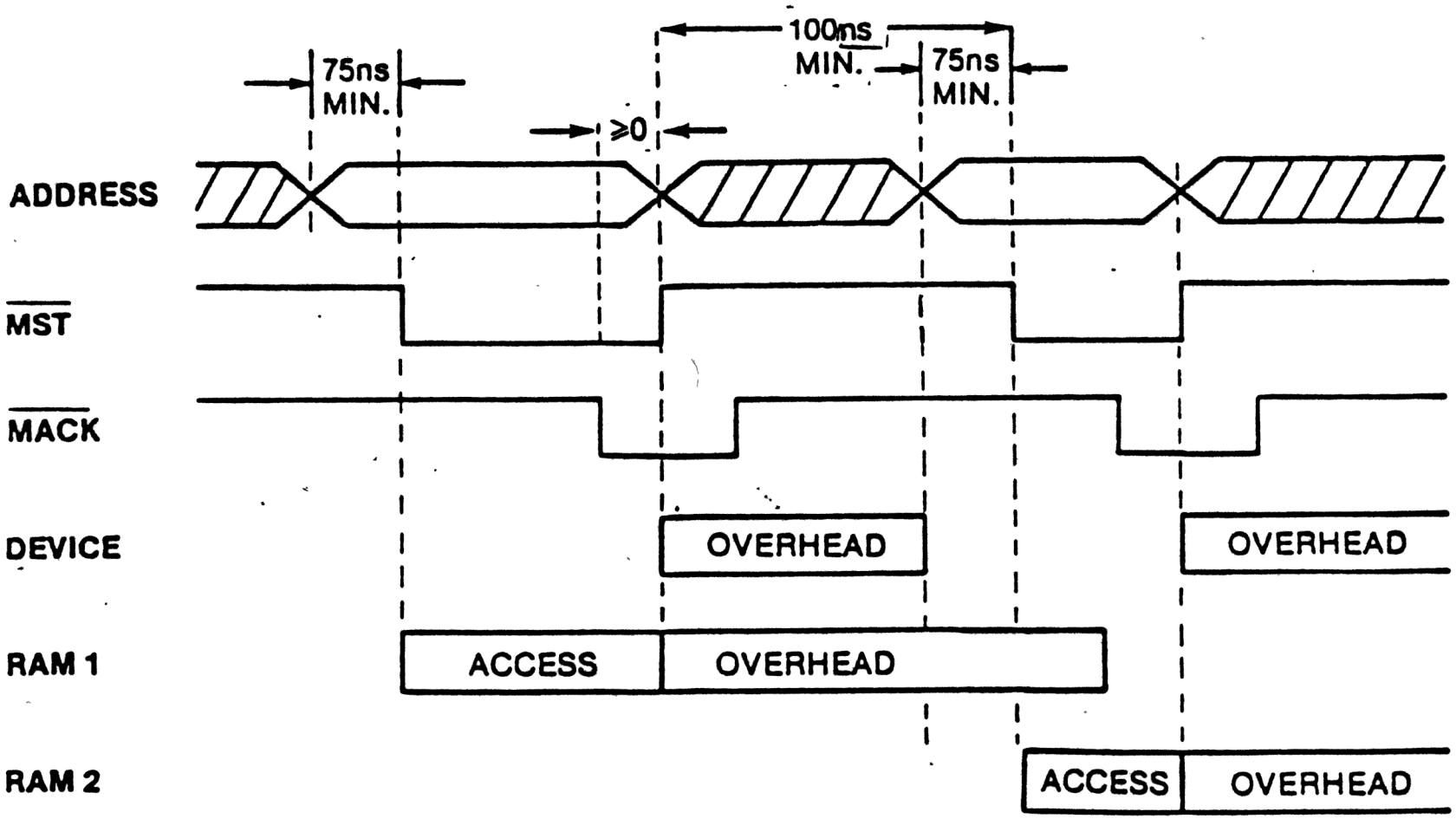


Figure 1-4. Memory Cycle Timing With Interleaving

1.2.2.2 Word Mode

Figure 1-5 illustrates how a sequence of data transfers affects the interleaved pair of memory modules. Since the access interval for one module can occur during the overhead interval of the other module in the interleaved pair, the effective transfer rate for any given memory module is improved.

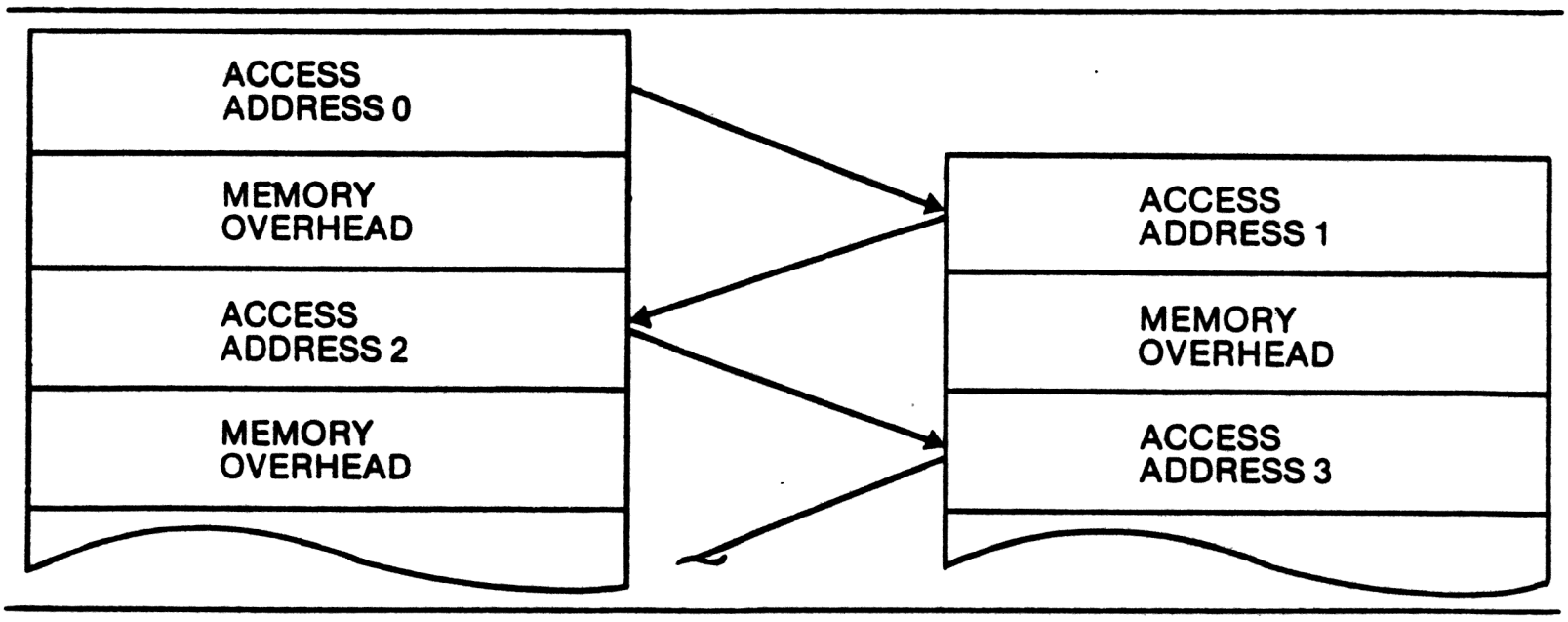


Figure 1-5. Interleaved Memory Access Sequence (Word)

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1.2.2.3 Byte Mode

The description of memory interleaving in word mode assumed the data transferred was in 16-bit words. When 8-bit bytes are transferred, it is necessary to perform two memory cycles in one memory module. In byte mode, bytes can be accessed independently and in any order. Figure 1-6 illustrates the optimum interleaved memory access sequence in byte mode.

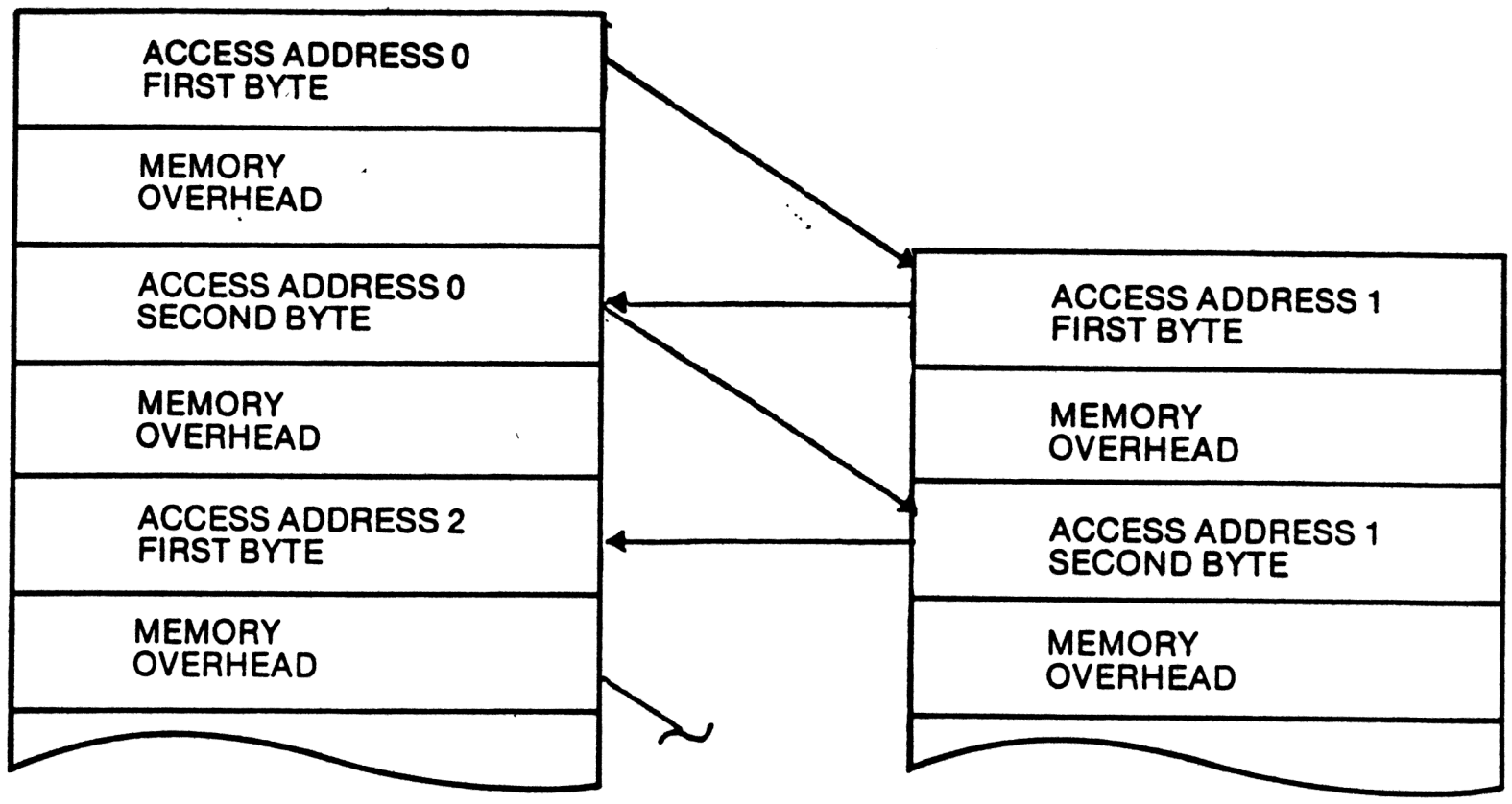


Figure 1-6. Interleaved Memory Access Sequence (Byte)

1.2.2.4 Power Consumption

The meaning of operating and standby power consumption differs for core and semiconductor memories.

For core memories, the maximum operating power consumption refers to the power consumed when the memory is powered, is being accessed by the CPU or a Direct Memory Access (DMA) controller, and contains all one bits. The typical operating power consumption is the amount of power consumed when the memory is powered, is being accessed by the CPU or a DMA controller, and contains an equal number of zero and one bits. Core standby power consumption refers to the power consumed when the memory is powered but is not being accessed.

For semiconductor memories, the operating power consumption is the power consumed when the memory is powered and being accessed by the CPU or a DMA controller. The standby power consumption is the power consumed when the memory is powered but is not being accessed.

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1.3 BATTERY BACKUP

NAKED MINI 4 Family semiconductor RAM memories are equipped with invalid data detection logic. This logic monitors the voltage being supplied to the on-board RAM array and senses if this voltage drops below the "safe" level.

An on-card battery backup option is offered with several of the NAKED MINI 4 Family semiconductor memories. This option consists of a rechargeable nickel-cadmium battery and associated voltage regulator and charging circuits. When fully charged, this battery enables the memory to maintain the integrity of the stored data during a short-term loss of power. Normally the on-card battery backup, when fully charged, is able to maintain data integrity for a minimum of two minutes.

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SECTION 2

CORE RAM MODULES

2.0 INTRODUCTION

The storage of digital data requires a device having two stable and distinct states for each bit of data. A core memory uses a toroidal ferrite which has two distinct flux states. The flux state of a core is changed by driving current, with sufficient amplitude, through the wires threaded through the core. The flux remains in either a 0 or 1 state until a current of sufficient amplitude is driven in the opposite direction to cause a change of state.

The core flux direction is detected by driving a current through the core in one direction. If the core changes state, the relatively large flux change is detected by the induced voltage on the sense winding. The reading of a core, therefore, is destructive and will leave the core in a zero state. A write operation then is necessary to restore the data.

Coincident current selection provides an efficient method of addressing the core. Drive current is provided by two wires threaded through the core with each wire carrying only half the current required to switch the core. A core located at the intersection of the two wires receives full-select current; all other cores receive half-select current.

The sense line is used to detect the switching flux in a read operation and as an inhibit wire during a write. Inhibit current equal in amplitude to the half-select drive current is driven through all cores in one bit when a 1 is to be written; the effect of one of the half-select drive currents is cancelled.

The MAXI-BUS Interface, an asynchronous negative true bus consisting of address, data, and control signals, provides the computer interface.

The address portion of the MAXI-BUS Interface consists of lines labeled AB00- through AB15-, Extra Bit of Address (EBA-), and Select Lower Byte (SLB-). Lines AB00- through AB14- and EBA- provide 64K word addressability. Address line AB15- is asserted to perform byte mode addressing. SLB- not asserted selects the upper byte; asserted, it selects the lower byte. In byte mode, all data is transmitted on data lines DB00- through DB07-. Data lines DB08- through DB15- are driven high to produce all zeroes.

2.1 CORE RAM MODULE SPECIFICATIONS

This section provides specifications for the 16KB full card (Model 53677-08) and 32KB full card (Model 53673-16) core memories.

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2.1.1 Model 53677-08

The 16KB full card core memory (Model 53677-08) has a capacity of 16,384 bytes or 8,192 words with 16 bits per word.

2.1.1.1 Memory Cycle Times (Nominal)

Memory cycle times for the Model 53677-08 core memory are summarized in Table 2-1.

Table 2-1. Memory Cycle Times, Model 53677-08

	READ	WRITE
Access Interval	375 ns	250 ns
Overhead Interval	475 ns	600 ns
Total	850 ns	850 ns
Minimum Interleaved	475 ns	350 ns

2.1.1.2 Environmental

Environmental specifications for the Model 53677-08 core memory are summarized in Table 2-2.

Table 2-2. Environmental Specifications, Model 53677-08

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Noncondensing)	10 to 90

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NOTE

Free air flow around the unit is required to provide adequate cooling.

2.1.1.3 Physical

Physical specifications for the Model 53677-08 full card core memory are summarized in Table 2-3.

Table 2-3. Physical Specifications, Model 53677-08

Length	42.88 cm (16.88 in.)
Width	38.10 cm (15.0 in.)
Height	1.52 cm (0.6 in.)
Weight	1.8 kg (4 lb)

2.1.1.4 Electrical

Electrical specifications for the Model 53677-08 core memory are summarized in Table 2-4.

Table 2-4. Electrical Specifications, Model 53677-08

Power Dissipation (Maximum, All Voltages)	96 W
Voltage Regulation (All Voltages)	±2%
Power Consumption	
+12 Vdc Typical Operating	2.5 A
+12 Vdc Maximum Operating	2.6 A
+12 Vdc Standby	0.4 A
-12 Vdc Typical Operating	2.2 A
-12 Vdc Maximum Operating	4.2 A
-12 Vdc Standby	0.1 A
+5 Vdc Typical Operating	2.6 A
+5 Vdc Maximum Operating	2.8 A
+5 Vdc Standby	2.5 A

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2.1.2 Model 53673-16

The 32KB full card core memory (Model 53673-16) has a capacity of 32,768 bytes or 16,384 words with 16 bits per word.

2.1.2.1 Memory Cycle Times (Nominal)

Memory cycle times for the Model 53673-16 full card core memory are summarized in Table 2-5.

Table 2-5. Memory Cycle Times, Model 53673-16

	READ	WRITE
Access Interval	550 ns	250 ns
Overhead Interval	650 ns	950 ns
Total	1,200 ns	1,200 ns
Minimum Interleaved	650 ns	350 ns

2.1.2.2 Environmental

Environmental specifications for the Model 53673-16 core memory are summarized in Table 2-6.

Table 2-6. Environmental Specifications, Model 53673-16

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Noncondensing)	10 to 90

NOTE

Free air flow around the unit is required to provide adequate cooling.

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2.1.2.3 Physical

Physical specifications for the Model 53673-16 full card core memory are summarized in Table 2-7.

Table 2-7. Physical Specifications, Model 53673-16

Length	42.88 cm (16.88 in.)
Width	38.10 cm (15.0 in.)
Height	1.52 cm (0.6 in.)
Weight	1.8 kg (4 lb)

2.1.2.4 Electrical

Electrical specifications for the Model 53673-16 core memory are summarized in Table 2-8.

Table 2-8. Electrical Specifications, Model 53673-16

Power Dissipation (Maximum, All Voltages)	104 W
Voltage Regulation (All Voltages)	±2%
Power Consumption	
+12 Vdc Typical Operating	2.3 A
+12 Vdc Maximum Operating	2.5 A
+12 Vdc Standby	0.4 A
-12 Vdc Typical Operating	2.4 A
-12 Vdc Maximum Operating	5.2 A
-12 Vdc Standby	0.1 A
+5 Vdc Typical Operating	2.65 A
+5 Vdc Maximum Operating	3.0 A
+5 Vdc Standby	2.45 A

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2.2 CORE INSTALLATION

There are special installation requirements for memory modules that use interleaving and both module and submodule memory banking. Both interleaving and memory banking are controlled using the memory control connector; therefore, use of both features at the same time is not recommended due to the resulting installation complications.

2.2.1 Model 53677-08

The 16KB full card core (Model 53677-08) has memory banking and interleaving features. Both features require special installation instructions.

2.2.1.1 Memory Banking Requirements

The 16KB full card core module has the memory banking feature which requires special installation for the memory control connector (J2). The memory banking strapping is detailed in this section.

2.2.1.2 Interleaving Requirements

The 16KB full card core module has the interleaving feature which has special requirements for the memory control connector (J2).

2.2.1.3 Interleaving Strapping

Each memory module in an interleaved pair is assigned either the odd or even address for the range of addresses covered by the interleaved pair. The two same-sized memory modules are interleaved with the odd memory address module closer to the processor on the MBIN/MBOT priority chain.

The strapping required for interleaving is made on the memory control connector header. Figure 2-1 shows the strapping pin locations on the memory control connector. To select interleaved mode, install a jumper between pins 5 and 12 on each module. One memory module of each interleaved pair of memory modules must be strapped for the odd addresses by installing a second jumper between pins 6 and 11. Use metric gauge 3 to 5 (AWG 24 to 28) solid wire for the jumpers and solder all connections.

Modules in interleaved mode must be installed in vertically adjacent slots on the MBIN/MBOT priority chain, with the odd-address module installed closest to the processor. The propagation delay induced by the buffer board on the expansion chassis is greater than any timing improvement derived by interleaving.

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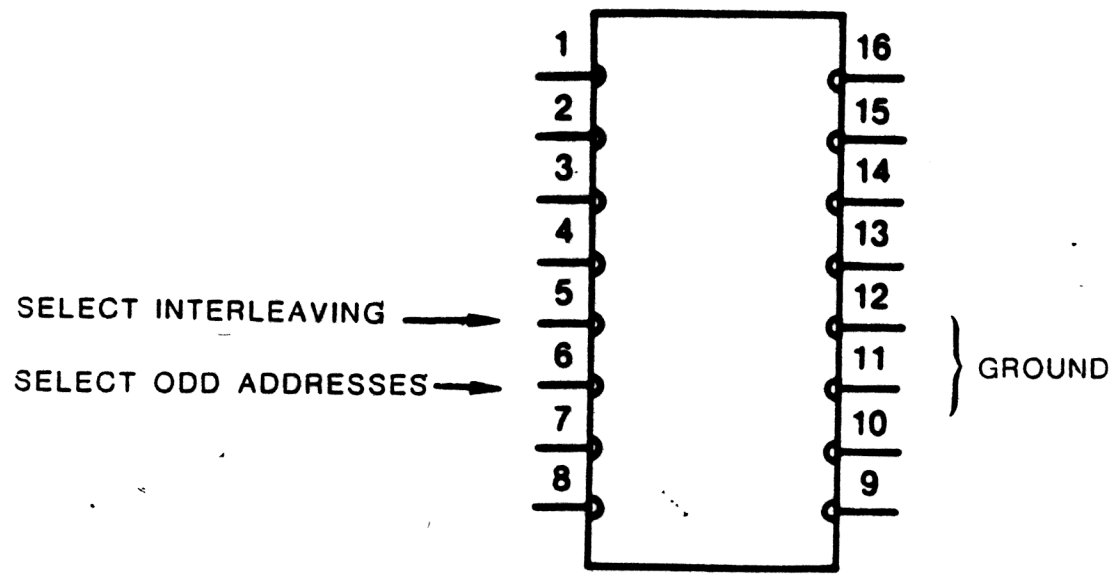


Figure 2-1. Memory Module Interleaving Strapping

2.2.2 Model 53673-16

The 32KB full card core memory (Model 53673-16) has the module and submodule memory banking feature.

2.2.2.1 Memory Banking Strapping

The strapping required for memory banking is made on the memory control connector (J2) header (Figure 2-2). If the memory control cable is changed from primary to alternate or from alternate to primary memory block control, the memory control header must be rewired.

To change from primary to alternate, remove the jumper between pins 8 and 9 and move the enable wire from pin 7 to pin 8.

To change from alternate to primary, move the enable wire from pin 8 to pin 7 and insert a jumper between pins 8 and 9.

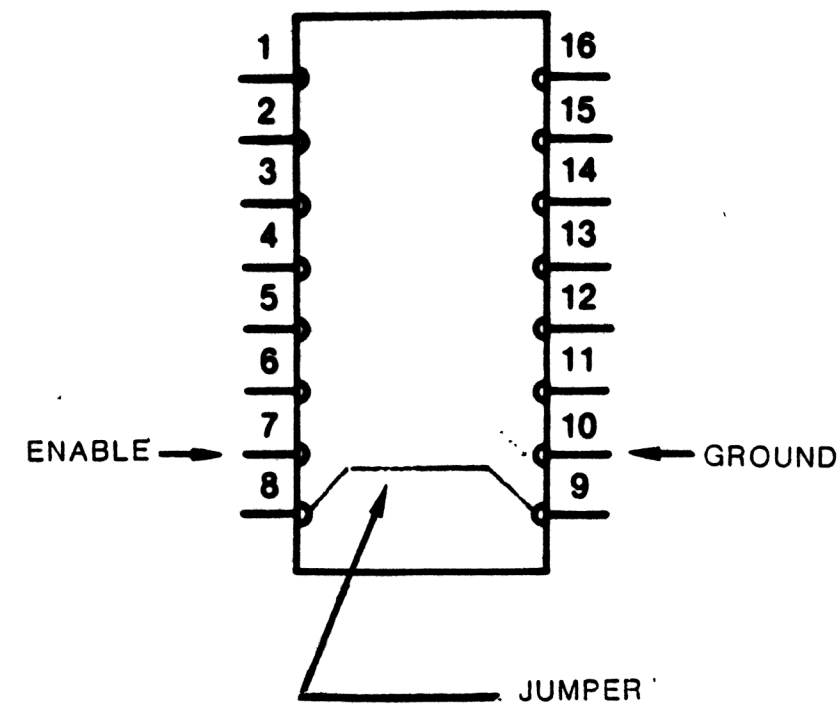
Use metric gauge 3 to 5 (AWG 24-28) solid wire and solder all connections.

Alternate memory modules for a given primary memory module must be located on the MAXI-BUS Interface between the processor and the primary memory.

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PRIMARY CONTROL CABLE CONNECTOR



ALTERNATE CONTROL CABLE CONNECTOR

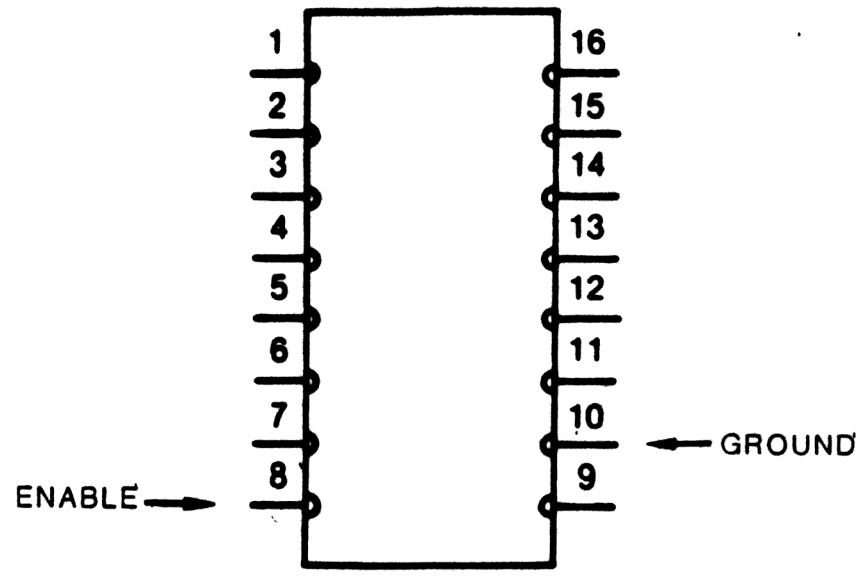


Figure 2-2. Control Cable Connector Wiring

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2.2.2.2 Submodule Memory Banking Strapping

Submodule memory banking is a feature on the 32KB full card module and has installation requirements for the memory control connector (J2) in addition to those requirements for module level memory banking. Submodule banking requires either assembly 53673-36 (32KB core memory with 16KB banking) or assembly 53673-46 (32KB core memory with 8KB banking).

For submodule memory banking, one or two additional wires must be connected to pins 1 and 2 of the memory control connector header to provide the submodule block selection (Figure 2-3). The requirements for adding wires are as follows:

1.	Submodule banking disabled	No wire
2.	Subdivided into two blocks	1 wire (2^1)
3.	Subdivided into four blocks	2 wires (2^1 and 2^0)

The submodule block select lines are listed as carrying a binary value that is related to a subdivided block size of 8K bytes.

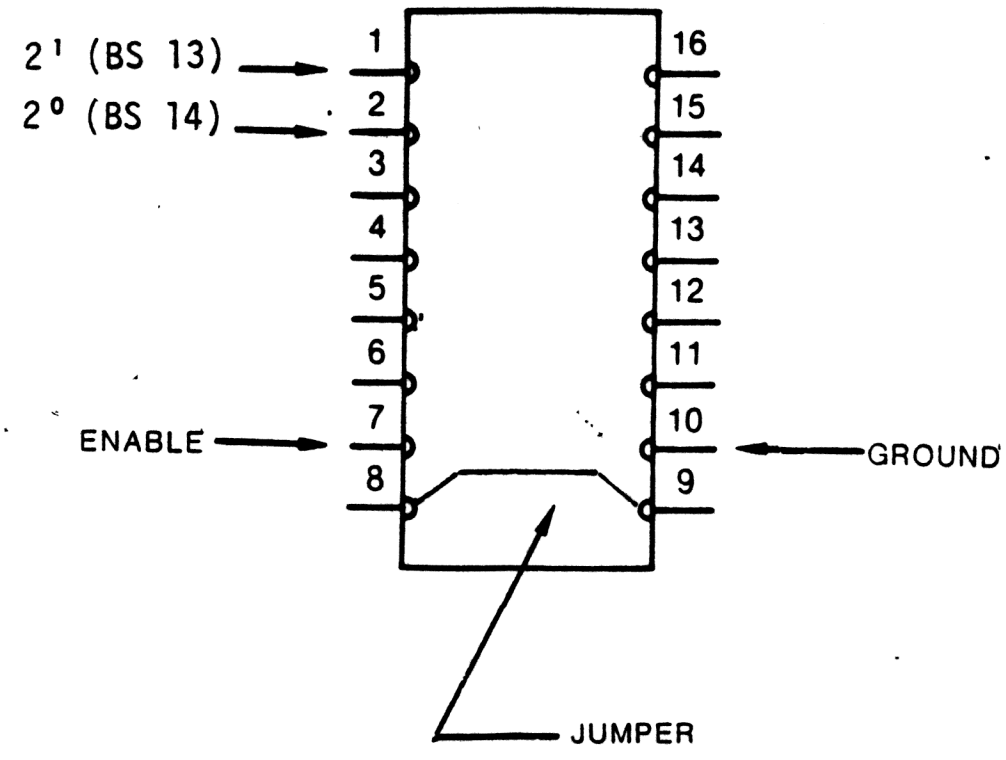
2.2.2.3 Interleaving Requirements

The 32KB full card module has the interleaving feature which has special installation requirements for the memory control connector (J2). The memory interleaving strapping is detailed in this section.

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PRIMARY CONTROL CABLE CONNECTOR AND STRAPPING



ALTERNATE CONTROL CABLE CONNECTOR AND STRAPPING

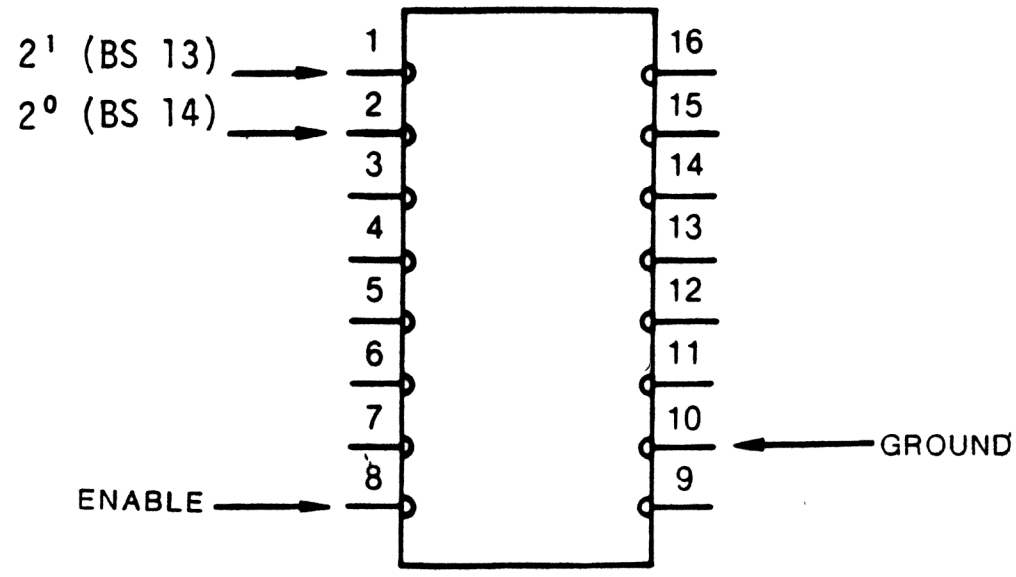


Figure 2-3. Memory Control Cable Connector Wiring

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SECTION 3

SEMICONDUCTOR COMBINATION RAM AND ROM MODULES

3.0 INTRODUCTION

Computer Automation, Inc., produces semiconductor combination memory modules with up to 4K bytes of read/write memory (RAM) and sockets for up to 16K bytes of ultraviolet Erasable, Programmable Read-Only Memory (EPROM) or mask-programmed Read-Only Memory (ROM). Table 3-1 summarizes the model numbers for the combination memory modules.

The basic storage element is a 512 byte by four-bit n channel static MOS RAM that has a one microsecond access and cycle time.

The read-only memory (ROM) is a 2K byte by eight-bit n channel device with a 450 nanosecond access and cycle time.

Table 3-1. Environmental Specifications, Model 53678-XX

WORDS (RAM)	BATTERY BACKUP	
	WITHOUT	WITH
0	53678-00	--
256	--	53678-39
1K	--	53678-59
2K	--	53678-69

3.1 SPECIFICATIONS

This section provides specifications for the combination semiconductor memory module, Model 53678-XX.

3.1.1 Memory Cycle Times (Read and Write, Nominal)

Memory cycle times for the combination memory module (Model 53678-XX) are summarized in Table 3-2.

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Table 3-2. Memory Module Cycle Times, Model 53678-XX

Access Interval	1.4 µs
Overhead Interval	0 µs
Total	1.4 µs

3.1.2 Environmental

Environmental specifications for the combination memory module are summarized in Table 3-3.

Table 3-3. Environmental Specifications, Model 53678-XX

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Noncondensing)	5 to 80

NOTE

Free air flow around the unit is required to provide adequate cooling.

3.1.3 Physical

Physical specifications for the combination memory module are summarized in Table 3-4.

Table 3-4. Physical Specifications, Model 53678-XX

Length	42.88 cm (16.88 in.)
Width	19.00 cm (7.48 in.)
Height	1.52 cm (0.6 in.)
Weight	1.35 kg (3 lb)

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3.1.4 Electrical

Electrical specifications for the combination memory module are summarized in Table 3-5.

Table 3-5. Electrical Specifications, Model 53678-XX

Power Dissipation (Maximum, All Voltages)	45 W
Voltage Regulation (All Voltages)	±5%
Power Consumption (No RAM) +5 Vdc Average Operating +5 Vdc Maximum Operating -12 Vdc Maximum Operating	 0.9 A 1.1 A 2 mA
Power Consumption (256 Words RAM) +5 Vdc Average Operating +5 Vdc Maximum Operating -12 Vdc Maximum Operating	 1.1 A 1.3 A 2 mA
Power Consumption (1K Words RAM) +5 Vdc Average Operating +5 Vdc Maximum Operating -12 Vdc Maximum Operating	 1.5 A 1.78 A 2 mA
Power Consumption (2K Words RAM) +5 Vdc Average Operating +5 Vdc Maximum Operating -12 Vdc Maximum Operating	 2.0 A 2.8 A 2 mA
Addtional Power Consumption Per 1K ROM +12 Vdc Average Operating +12 Vdc Maximum Operating -12 Vdc Average Operating -12 Vdc Maximum Operating +5 Vdc Average Operating +5 Vdc Maximum Operating	 50 mA 65 mA 30 mA 45 mA 6 mA 10 mA

NOTE

When the battery backup option is used, battery charging results in an additional power consumption at +12Vdc of approximately 12 milliamps.

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3.2 INSTALLATION

This section discusses the requirements for installing the combination memory module (Model 53678-XX).

3.2.1 Joining Requirements

There are no special requirements if the combination memory module is installed in a half card chassis. If the combination memory module is to be installed in a full card chassis, it first must be joined with a half card processor, an I/O controller, a filler card, or another half card memory module. The J1 connector on the memory module (see Figure 3-1) accepts one end of the 16-pin jumper when the half card combination module is joined to a half card processor. Refer to the applicable computer reference manual for information on the joining of half cards.

The joining of a half card memory with another half card module could require modification of the motherboard if an expansion chassis is used. Refer to the appropriate computer reference manual if motherboard modifications are required.

3.2.2 Switch Settings

There are three sets of switches (labeled SW1, SW2, and SW3) on the semiconductor combination memory board. SW1 and SW2 are located near the J4 connector, and SW3 is located on the P4 plug and selects the battery backup option (Section 6).

3.2.2.1 Selecting Lower Limit and Memory Size

The lower address limit and memory size are added to form the upper address limit. Each input address received on the address bus is compared with the upper and lower address limits. If it is within these limits, the memory board is activated.

Table 3-6 shows how the lower address limit is selected using switches SW1-1 through SW1-6.

Generally, set the lower address limit 4 KB below the beginning address of the ROM, regardless of the amount of RAM on the board. If a gap occurs between the end of RAM and the beginning of the ROM, the gap can be filled using overlap or ghost memory (described in this section).

Lower memory limit will be required at the last address of the preceding memory unless overlapping is selected. If overlapping is selected, the lower limit equals the difference between the upper limit of the preceding memory and the amount of overlap (2 KB or 4 KB). See Figure 3-1.

Table 3-7 shows how to specify the memory size using switches SW2-1 through SW2-4. Set the memory size of the configuration equal to or above the actual memory size being used. For example, with 512 bytes of RAM and a 6 KB ROM, set the switches as shown for the "XB RAM + 8KB ROM" configuration.

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Table 3-6. Lower Limit Switch Settings (Page 1 of 2)

LOWER LIMIT	SW1-6	SW1-5	SW1-4	SW1-3	SW1-2	SW1-1
0	ON	ON	ON	ON	ON	ON
1K	ON	ON	ON	ON	ON	OFF
2K	ON	ON	ON	ON	OFF	ON
3K	ON	ON	ON	ON	OFF	OFF
4K	ON	ON	ON	OFF	ON	ON
5K	ON	ON	ON	OFF	ON	OFF
6K	ON	ON	ON	OFF	OFF	ON
7K	ON	ON	ON	OFF	OFF	OFF
8K	ON	ON	OFF	ON	ON	ON
9K	ON	ON	OFF	ON	ON	OFF
10K	ON	ON	OFF	ON	OFF	ON
11K	ON	ON	OFF	ON	OFF	OFF
12K	ON	ON	OFF	OFF	ON	ON
13K	ON	ON	OFF	OFF	ON	OFF
14K	ON	ON	OFF	OFF	OFF	ON
15K	ON	ON	OFF	OFF	OFF	OFF
16K	ON	OFF	ON	ON	ON	ON
17K	ON	OFF	ON	ON	ON	OFF
18K	ON	OFF	ON	ON	OFF	ON
19K	ON	OFF	ON	ON	OFF	OFF
20K	ON	OFF	ON	OFF	ON	ON
21K	ON	OFF	ON	OFF	ON	OFF
22K	ON	OFF	ON	OFF	OFF	ON
23K	ON	OFF	ON	OFF	OFF	OFF
24K	ON	OFF	OFF	ON	ON	ON
25K	ON	OFF	OFF	ON	ON	OFF
26K	ON	OFF	OFF	ON	OFF	ON
27K	ON	OFF	OFF	ON	OFF	OFF
28K	ON	OFF	OFF	OFF	ON	ON
29K	ON	OFF	OFF	OFF	ON	OFF
30K	ON	OFF	OFF	OFF	OFF	ON
31K	ON	OFF	OFF	OFF	OFF	OFF
32K	OFF	ON	ON	ON	ON	ON
33K	OFF	ON	ON	ON	ON	OFF
34K	OFF	ON	ON	ON	OFF	ON
35K	OFF	ON	ON	ON	OFF	OFF
36K	OFF	ON	ON	OFF	ON	ON
37K	OFF	ON	ON	OFF	ON	OFF
38K	OFF	ON	ON	OFF	OFF	ON
39K	OFF	ON	ON	OFF	OFF	OFF
40K	OFF	ON	OFF	ON	ON	ON
41K	OFF	ON	OFF	ON	ON	OFF
42K	OFF	ON	OFF	ON	OFF	ON
43K	OFF	ON	OFF	ON	OFF	OFF

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Table 3-6. Lower Limit Switch Settings (Page 2 of 2)

LOWER LIMIT	SW1-6	SW1-5	SW1-4	SW1-3	SW1-2	SW1-1
44K	OFF	ON	OFF	OFF	ON	ON
45K	OFF	ON	OFF	OFF	ON	OFF
46K	OFF	ON	OFF	OFF	OFF	ON
47K	OFF	ON	OFF	OFF	OFF	OFF
48K	OFF	OFF	ON	ON	ON	ON
49K	OFF	OFF	ON	ON	ON	OFF
50K	OFF	OFF	ON	ON	OFF	ON
51K	OFF	OFF	ON	ON	OFF	OFF
52K	OFF	OFF	ON	OFF	ON	ON
53K	OFF	OFF	ON	OFF	ON	OFF
54K	OFF	OFF	ON	OFF	OFF	ON
55K	OFF	OFF	ON	OFF	OFF	OFF
56K	OFF	OFF	OFF	ON	ON	ON
57K	OFF	OFF	OFF	ON	ON	OFF
58K	OFF	OFF	OFF	ON	OFF	ON
59K	OFF	OFF	OFF	ON	OFF	OFF
60K	OFF	OFF	OFF	OFF	ON	ON
61K	OFF	OFF	OFF	OFF	ON	OFF
62K	OFF	OFF	OFF	OFF	OFF	ON
63K	OFF	OFF	OFF	OFF	OFF	OFF

Table 3-7. Memory Size Switch Settings

MEMORY SIZE	SW2-4	SW2-3	SW2-2	SW2-1
0 RAM	ON	ON	ON	ON
256W-1K RAM ONLY	ON	ON	ON	OFF
2K RAM ONLY	ON	ON	OFF	ON
RAM $\leq$ + 2K ROM	ON	OFF	ON	ON
RAM $\leq$ + 4K ROM	ON	OFF	OFF	ON
RAM $\leq$ + 6K ROM	OFF	ON	ON	ON
RAM $\leq$ + 8K ROM	OFF	ON	OFF	ON

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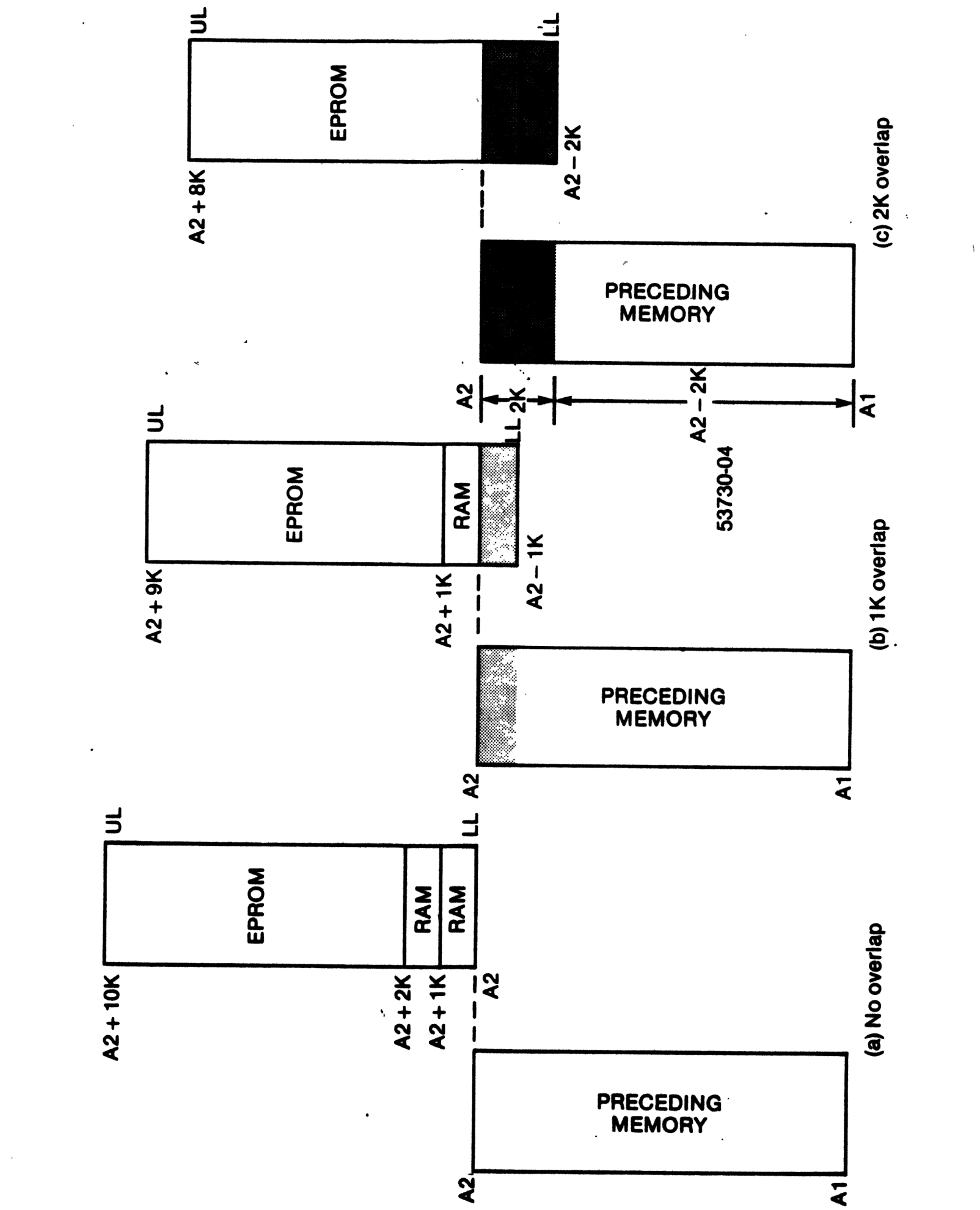


Figure 3-1. Memory Overlap

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Table 3-8. Option Switch Settings--SW2-5 unused

OPTION	SWITCH	SETTING
1K Overlap	SW1-7 SW1-8	ON OFF
2K Overlap	SW1-8 SW1-7 SW2-8	ON OFF OFF
Ghost Memory	SW2-8	ON
Automatic Startup	SW2-7 SW2-6	ON OFF ON OFF } LSI 2/3

3.2.2.2 Selecting Memory Options

The semiconductor combination memory options include overlap, ghost memory, and Automatic Startup (ASU). Table 3-8 summarizes the switch settings used to select a memory option.

3.3 MEMORY OPTIONS

This section discusses memory options for the combination memory module, including overlap memory, ghost memory, and ASU.

3.3.1 Overlap and Ghost Memory

If the semiconductor combination memory module has less than 4K bytes of RAM, a gap will exist between the end of the RAM and the beginning of the ROM. The gap will vary between zero bytes (with 4KB of RAM memory on the board) and 4 KB (with no RAM memory on the board). The gap is filled in one of two ways: overlap or ghost memory, but these techniques cannot be used simultaneously.

3.3.1.1 Overlap Memory

If the RAM/EPROM memory module is not the first (lowest address) memory in the system, the gap can be filled by overlapping with the preceding (lower address) memory. The preceding memory must be large enough to cover the gap. Switch settings for overlap are shown in Table 3-8.

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3.3.1.2 Ghost Memory

Where the ghost memory feature is enabled to fill the gap, it spreads whatever RAM is on the board (512, 2K, or 4K bytes) across the entire 4K byte area allotted for RAM. For example, if there are 512 bytes of RAM, the ghost memory feature causes a given RAM location to respond to eight different addresses, each addressing 512 bytes from the adjacent address. Ghost memory does not affect the addressing of the read-only memory. For example, the same location could be addressed as :X064, :X164, :X264, or :X364 (assuming 512K bytes are installed and ghosted).

It should be noted that only the integer power of two amounts of RAM can be installed if the user wishes to use ghosting. Thus, while 512 bytes or 1,024 bytes of RAM could be used, with the rest of the addressing space ghosted or overlapped, 1,536 bytes could not be used ($1536 = 3 \times 2^9$). It is possible, say, to install 1536 bytes in the upper 2 KB of the RAM space, and eliminate the the lower 2 KB by overlapping, but the 512 byte gap cannot be eliminated.

NOTE

The ghost memory feature does not increase the amount of memory, but makes existing on-board RAM easier to address. Since each RAM location responds to two or more addresses, depending upon the amount of on-board RAM, care must be taken to avoid accidentally writing over data stored previously at the same RAM location.

3.3.2 Automatic Startup

Automatic Startup (ASU) initiates execution of a power-up service routine at initial power on time and upon resumption of power following a power failure. The ROM portion of memory can be used to store a custom or user AutoLoad program in lieu of an optional AutoLoad ROM. The AutoLoad program is contained in the lowest ROM memory location in the system. This ROM must be in an address space lower than any core location in the system.

To initiate ASU manually, place the computer in the Run Enable mode by pressing AUTO (on the Programmer's Console) or START (on the Operator's Console). Pressing one of these switches sets the Invalid Data Detect (IDD) flip-flop, which disables the RAM memory. In addition, the IDD flip-flop forces a power-fail sequence by firing a 15 millisecond one shot power surge. When the one shot surge has timed out, the processor initiates a power-up sequence.

The processor then begins executing instructions at :0080. This location must be in semiconductor RAM. Since RAM is disabled, all RAM locations will be interpreted as zeros (no-op instructions). The processor will pass or bubble through each RAM location until the first ROM location is reached. This location must contain an OUT instruction specifying the A, Q, X, or Y register with a device address 0 and function code 2. Executing the instruction resets the AutoLoad condition on the console and turns off the AUTOLOAD indicator. The next instruction must contain a COPY (store) to memory instruction to any location in installed RAM. This resets the IDD flip-flop and enables RAM. Finally, the next instruction location must contain either a jump to a power-up service routine or the first instruction in that power-up service routine.

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ASU can be initiated automatically at power-up. Applying power to the computer will set the IDD flip-flop, which disables RAM and causes the processor to bubble through RAM to the first instruction in ROM.

3.4 EPROM MEMORY ARRAY

This section presents information for possible EPROM configuration and programming.

3.4.1 Description

The socketed EPROM array is designed to accomodate up to 16 Intel 2708 EPROM chips (or equivalent), where each Intel 2708 provides 1K by 8 bits of storage. The metal-masked ROM version of this chip, Intel 2308 (or equivalent), can also be used if desired. These chips are not included with the memory board and must be ordered directly from the manufacturer.

Table 3-9 shows the correlation between the 16 possible EPROMs and portions of a user's EPROM program (by address relative to the lower limit).

A low at an EPROM address input corresponds to a logical zero in the computer system. A low at an EPROM data output corresponds to a logical one in the computer system. Intel ships its 2708 and 2308 chips with all their data written as high levels (logical zeros) to the system.

Table 3-9. EPROM Socket Locations

ADDRESS ABOVE LOWER LIMIT (HEXADECIMAL)	EPROM FOR DATA BITS 8-15	EPROM FOR DATA BITS 0-7
:0800-:0BFF	86	87
:0C00-:0FFF	88	89
:1000-:13FF	90	91
:1400-:17FF	92	93
:1800-:1BFF	94	95
:1C00-:1FFF	96	97
:2000-:23FF	98	99
:2400-:27FF	100	101

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3.4.2 ROM/PROM Format Generator

The ROM/PROM Format Generator (ROMGEN) is a Computer Automation, Inc., utility program for generating input patterns required by the following vendors in the manufacture of ROMs, PROMs, and EPROMs:

1. Data I/O--Universal PROM Programmer
2. Electronic Arrays
3. Intel
4. Monolothic Memories
5. Signetics
6. Texas Instruments.

The ROMGEN program is supplied on paper tape (Part Number 00-96060) or on floppy disk (00-93060) in standard Computer Automation, Inc., object format which can be loaded via any NAKED MINI 4 binary loader. It requires a minimum of 4K words of memory and a terminal for operator communication and input. A tape reader (e.g., ASR-33 TTY) can also be used for input.

The formatted output is to a high-speed paper tape punch, the TTY punch or EBCDIC patterns on magnetic tape, which are card images that can be used to produce a card deck.

For more information, see the NAKED MINI 4 ROM/PROM Format Generator Manual.

3.5 POWER FAIL SEQUENCE

Semiconductor RAM memories are volatile in nature. That is, they can lose data if the supply voltage from the computer drops below a preset "safe" level. For this reason, all NAKED MINI 4 Family memories that contain semiconductor RAM are equipped with invalid data detection logic. If the voltage being supplied to the board drops below the "safe" level, the invalid data detection logic indicates whether the integrity of the data has been maintained.

3.5.1 With Battery Backup Option Installed

If the supply voltage does drop below the safe level, the memory disable signal will switch the board to battery backup power, if this option is installed (Section 6).

3.5.2 Battery Backup Exhausted or Not Installed

If battery backup is not present, or if it is exhausted, the invalid data detection logic will set an internal memory flip-flop called Invalid Data Detect (IDD). The IDD flip-flop disables RAM on the board and causes it to respond to any subsequent memory read operation by putting all zeros (no-op instructions) on the data bus. Read operations from ROM are not affected.

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All NM4 Series memories are connected together by the ALSP- line. If one memory loses RAM power, the IDD flip-flop is set, and the ALSP- line is driven low. Each semiconductor memory in the system receives the ALSP- line and sets its own IDD flip-flop.

3.5.3 At Power Return

When power returns, the RAM will remain disabled until the IDD flip-flop is reset. This resetting can be accomplished by a COPY (store) to memory instruction to any location in installed RAM. Once IDD is reset, normal operation is resumed.

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SECTION 4

RANDOM ACCESS SEMICONDUCTOR MEMORY MODULES

4.0 INTRODUCTION

This section describes the four semiconductor RAM modules designed for interface with LSI Series and NAKED MINI 4 Family computers. The modules are designated 53642, 53707, 53775, and 53819.

4.1 MODEL 53642

Model 53642 is a 16 KB half card RAM module designed for use with the LSI Series computers. The memory (16 KB x 16 bits) can also be configured as 8 KB x 16 bits.

4.1.1 Specifications

This section presents specifications for the RAM semiconductor module Model Number 53642.

4.1.1.1 Memory Cycle Times

Memory cycle times for Model 53642 are summarized in Table 4-1.

Table 4-1. Memory Cycle Times, Model 53642

Read Access Time	540 ns
Write Access Time	390 ns
Read or Write Cycle Time	840 ns
Refresh Cycle Time	840 ns

4.1.1.2 Environmental

Environmental specifications for Model 53642 are summarized in Table 4-2.

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Table 4-2. Environmental Specifications, Model 53642

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-Operating Temperature Range (Degrees Celsius)	-30 to +90
Relative Humidity (Percent, Noncondensing)	15 to 80

4.1.1.3 Physical

Physical specifications for Model 53642 are summarized in Table 4-3.

Table 4-3. Physical Specifications, Model 53642

Length	42.89 cm (16.89 in.)
Width	19.00 cm (7.48 in.)

4.1.1.4 Electrical

Electrical specifications for Model 53642 are summarized in Table 4-4.

Table 4-4. Electrical Specifications, Model 53642

Voltage Regulation (All Voltages)	±5%
+5 Vdc Maximum Operating +5 Vdc Standby	1.16 A 0.23 A
+12 Vdc Maximum Operating +12 Vdc Standby	0.48 A 0.036 A
-12 Vdc Maximum Operating -12 Vdc Standby	0.018 A 0.018 A

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4.1.2 Installation

Prior to removing or installing a module, it is essential to remove all power from the system. After powering down, any battery backup must be removed. Set the battery select (INT/EXT, S1) to INT. Next remove all battery connectors from the external battery connectors P3 and P4. Then switch the select switch to the EXT position.

CAUTION

Failure to disconnect battery backup power from a RAM module will result in damage to the RAM.

The RAM board has on-board MOS memory devices that are sensitive to static electricity. Caution should be used when handling or installing the module to insure the highest degree of reliability.

This module is a half card module which can be installed in either half card or full card chassis. If it is to be installed in a half card chassis, no special preparation is needed for that purpose. However, for installation in a full card chassis, the module must first be joined with another half card, such as another memory module or a half card processor card and propagation requirements of the Memory Banking In/Memory Banking Out (MBIN/MBOT) chain must be observed. Refer to the Chassis Configuration Reference Manual and Installation Guide for information on the joining of half cards.

4.1.3 Automatic Startup (ASU)

Automatic Startup (ASU) is a standard feature which makes the 53642 RAM module compatible with the 53595 ROM/PROM board.

ASU initiates execution of a power-up service routine at initial power on time and upon resumption of power following a power failure. The ROM portion of the 53595 memory can be used to store a custom or user AutoLoad program in lieu of an optional AutoLoad ROM. The AutoLoad program is contained in the lowest ROM memory location in the system. This ROM must be in an address space lower than any core location in the system.

To initiate ASU manually, place the computer in the Run Enable mode by depressing AUTO (on the Programmer's Console) or START (on the Operator's Console). Pressing one of these switches sets the Invalid Data Detect (IDD) flip-flop which disables the RAM memory. In addition, the IDD flip-flop forces a power-fail sequence by firing a 15-millisecond one shot power surge. When the one shot surge has timed out, the processor will initiate a power-up sequence.

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The processor then begins executing instructions at :0080. This location must b in semiconductor RAM. Since RAM is disabled, all RAM locations will be interpreted as zeros (no-op instructions). The processor will pass or bubble through each RAM location until the first ROM location is reached. This location must contain an OUT instruction specifying the A, Q, X, or Y register with a device address 0 and function code 2. Executing the instruction resets the AutoLoad condition on the console and turns off the AUTOLOAD indicator. The next instruction must contain a COPY (store) to memory instruction to any location in installed RAM. This resets the IDD flip-flop, enabling RAM. Finally, the next instruction location must contain either a jump to a power-up service routine or the first instruction in that power-up service routine.

ASU can be initiated automatically at power-up. Applying power to the computer will set the IDD flip-flop, which disables RAM and causes the processor to bubble through RAM to the first instruction in ROM.

4.1.4 Refresh

The memory board uses cycle stealing refresh which is asynchronous to normal memory operation.

A memory busy flip-flop indicates that a memory cycle, either refresh or normal, is underway. If a refresh clock signal occurs while the memory is busy with normal operation, it is stored. At the end of a normal memory cycle the refresh cycle is started. If the memory is not busy with a normal cycle when the refresh clock signal occurs, the refresh cycle is started without delay.

The refresh clock has a period of approximately 25 microseconds.

The memory supplies a refresh address and retains the new refresh address for the next refresh cycle.

4.2 MODEL 53707

The Model 53707 memory module is available in two basic models, one using a medium speed RAM and the other using a high speed RAM. Each basic model is available in configurations from 16K bytes to 32K bytes, with battery backup and parity. Interleaving and memory module banking are standard features on all models. Model 11611-32 allows sub-module memory banking. Table 4-5 summarizes the available models.

Table 4-5. Memory Identification, Model 53707

MODEL	DESCRIPTION	XX*
11611-XX	Medium Speed RAM with BBU and Parity	16, 32
11711-XX	Fast Speed RAM with BBU and Parity	16, 32
NOTE: *16 = 32K byte capacity, 32 = 64K byte capacity		

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4.2.1 Specifications

This section presents specifications for the semiconductor RAM module, Model Number 53707.

4.2.1.1 Memory Cycle Times

A minimum cycle time occurs if a refresh signal (Topic 4.2.3.2) is sent at the end of a normal memory cycle. A "worst case" or maximum cycle time occurs if a refresh signal is sent at the beginning of a normal memory cycle. Refresh cycle time is equal to normal memory cycle time; the maximum cycle time is double the minimum cycle time.

The minimum cycle times for read and write operations and the minimum cycle time using interleaved modules are summarized in Table 4-6.

Table 4-6. Memory Cycle Times, Model 53707-XX

MODEL 11611-XX	Access Interval Overhead Interval Total Minimum Interleaved	495 ns 210 ns 705 ns 595 ns
MODEL 11711-XX	Access Interval Overhead Interval Total Minimum Interleaved	380 ns 170 ns 550 ns 480 ns

4.2.1.2 Environmental

Environmental specifications for Model 53707 are summarized in Table 4-7.

Table 4-7. Environmental Specifications, Model 53707

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Noncondensing)	15 to 80

NOTE

Free air flow around the unit is required to provide adequate cooling.

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4.2.1.3 Physical

Physical specifications for Model 53707 are summarized in Table 4-8.

Table 4-8. Physical Specifications, Model 53707

Length	42.88 cm (16.88 in.)
Width	38.10 cm (15 in.)
Height	1.52 cm (0.6 in.)
Weight	1.3 kg. (3.5 lb.)

4.2.1.4 Electrical

Electrical specifications for Model 53707 are summarized in Table 4-9.

Table 4-9. Electrical Specifications, Model 53707

Voltage Regulation (All Voltages)	±5%
Power Consumption--550 nanoseconds (ns) +12 Vdc Typical Operating +12 Vdc Maximum Operating +12 Vdc Standby -12 Vdc Typical Operating -12 Vdc Maximum Operating -12 Vdc Standby +5 Vdc Typical Operating +5 Vdc Maximum Operating +5 Vdc Standby	 1.25 A 2.0 A 0.8 A 0.02 A 0.2 A 0.02 A 1.5 A 2.0 A 1.5 A
Power Consumption--705 ns +12 Vdc Typical Operating +12 Vdc Maximum Operating +12 Vdc Standby -12 Vdc Typical Operating -12 Vdc Maximum Operating -12 Vdc Standby +5 Vdc Typical Operating +5 Vdc Maximum Operating +5 Vdc Standby	 1.20 A 2.0 A 0.8 A 0.02 A 0.2 A 0.02 A 1.5 A 2.0 A 1.5 A

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4.2.2 Installation

The RAM is a full card module, as shown in Figure 4-1. Special installation requirements are described in the following paragraphs. Both interleaving and memory banking are controlled using the memory control connector; therefore, use of both features at the same time is not recommended due to the resulting installation complications.

CAUTION

The RAM memory board has on-board MOS memory devices that are sensitive to static electricity. Caution should be used when handling or installing the module to insure the highest degree of reliability.

4.2.2.1 Module Installation

Prior to removing or installing modules in a chassis, it is necessary to set the INT/EXT switch S3 to INT and ensure that no external batteries are connected to the external battery connectors P3 and P4. Then set the INT/EXT Switch S3 to EXT, and proceed with the installation or removal.

CAUTION

Failure to disconnect external backup batteries and internal battery backup prior to removing or installing module in chassis may result in damage to the module.

Each memory module in an interleaved pair is assigned either the odd or even address for the range of addresses covered by the interleaved pair. The two same size memory modules are interleaved with the odd memory address module closest to the processor on the MBIN/MBOT priority chain.

The strapping required for interleaving is made on the memory control connector header. Figure 4-2 shows the strapping pin locations on the memory control connector. To select interleaved mode, install a jumper between pins 5 and 12 on each module. One memory module of each interleaved pair of memory modules must be strapped for the odd addresses by installing a second jumper between pins 6 and 11. Use AWG 24 to 28 (metric gauge 3 to 5) solid wire for the jumpers and solder all connections.

Modules in interleaved mode must be installed in vertically adjacent slots on the MBIN/MBOT priority chain, with the odd-address module installed closest to the processor. The bottom slot in a chassis is considered adjacent to the top slot in a downstream expansion chassis. However, interleaving of modules should be limited to those modules housed in the primary chassis; the propagation delay induced by the buffer board on the expansion chassis is greater than any timing improvement derived by interleaving.

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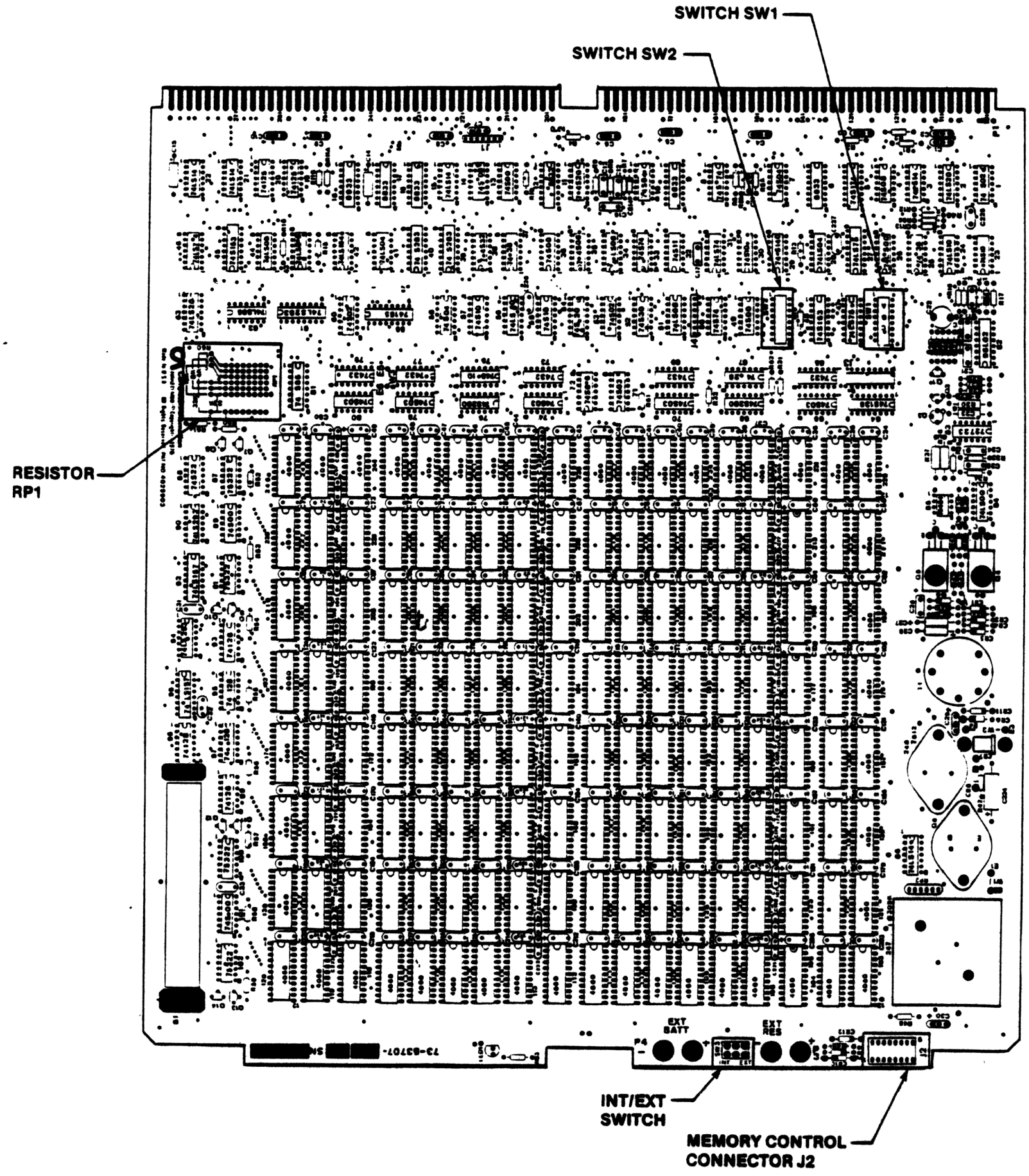


Figure 4-1. Random Access Full Card Memory Module

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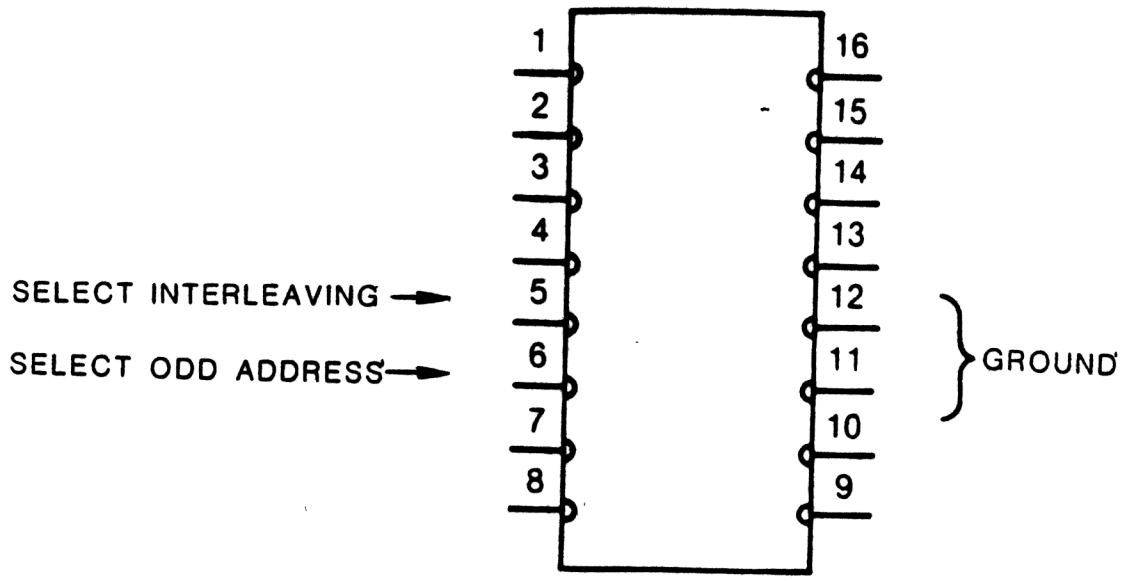


Figure 4-2. Memory Module Interleaving Strapping

4.2.2.2 Memory Banking Requirements

The RAM memory module has module and submodule memory banking features which both require special installation procedures for the memory control connector (J2).

4.2.2.3 Module Memory Banking Strapping

The strapping required for memory banking is made on the memory control connector header (see Figure 4-3). If the memory control cable is changed from primary to alternate or from alternate to primary memory block control, the memory block must be rewired. (Module and submodule memory banking are illustrated in Figure 4-6.)

NOTE

A Memory Banking Controller (MBC) can be initialized two ways. When ENABLE- (Pin 7) is used, the MBC is initialized so that its output is all zeros. When ENABLE (Pin 8) is used, the MBC is initialized so that its output is all ones.

The primary module is enabled by the initialization value; thus, when ENABLE- (Pin 7) is used, 0 enables the MBC, or, when ENABLE (Pin 8) is used, 1 enables the MBC. In this publication, by convention, the primary module is assumed enabled by a low (ENABLE-) signal.

To change from primary to alternate, remove the jumper between pins 8 and 9, and move the enable wire from pin 7 to pin 8.

To change from alternate to primary, move the enable wire from pin 8 to pin 7, and insert a jumper between pins 8 and 9.

Use AWG 24 to 28 (metric gauge 3 to 5) solid wire and solder all connections.

Alternate memory modules for a given primary memory module must be located on the MAXI-BUS Interface between the processor and the primary memory.

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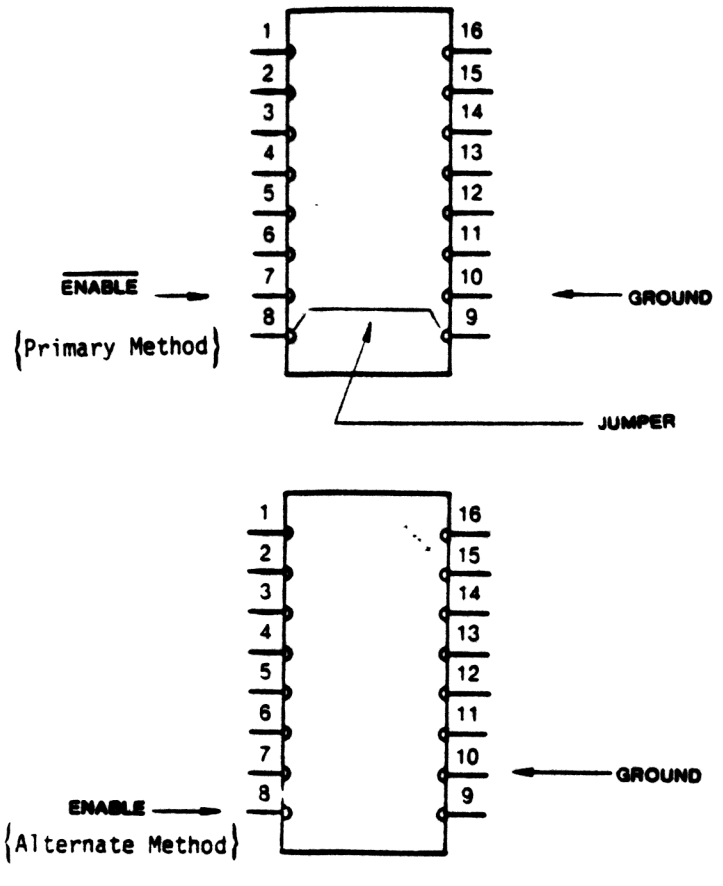


Figure 4-3. Control Cable Connector Wiring

4.2.2.4 Submodule Memory Banking Strapping

Submodule memory banking requires additional modification to those required for module level memory banking. Module and submodule memory banking are illustrated in Figure 4-6.

To provide the sub-module block selection, up to three additional wires must be connected to pins 1, 2, and 3 of the memory control connector (J2) (see Figure 4-4).

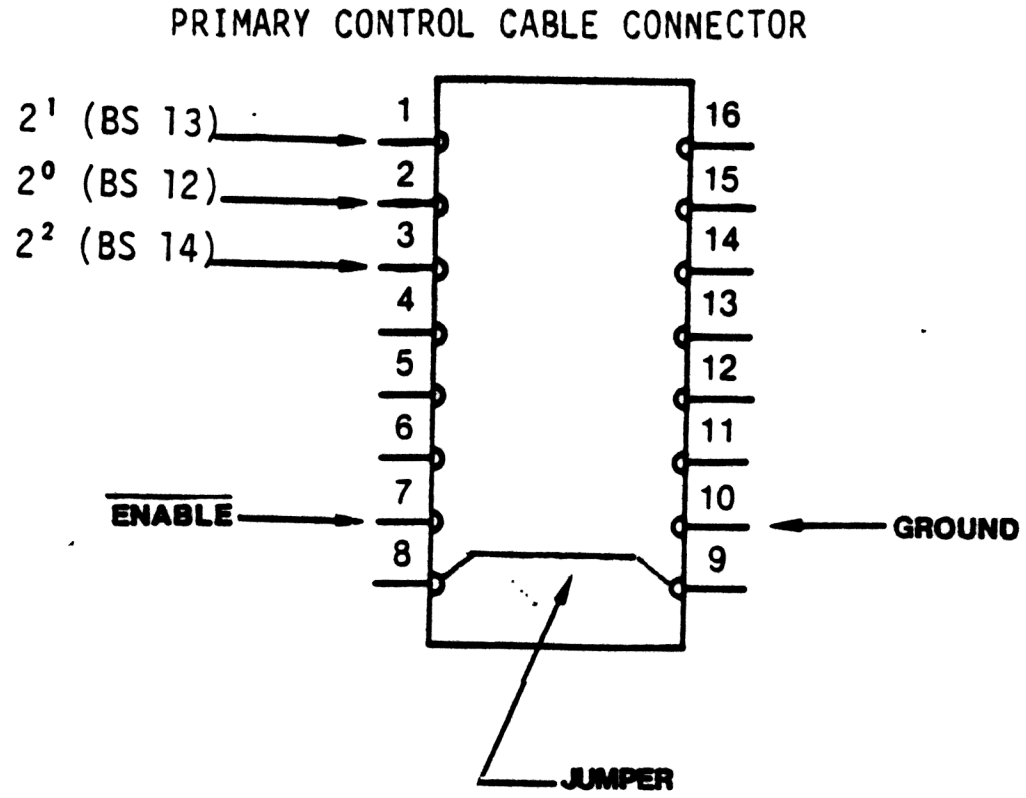
The requirements for adding wires are as follows:

1. Sub-module banking disabled--no wires
2. Subdivided into two blocks--one wire (2^1)
3. Subdivided into four blocks--two wires (2^1 and 2^0)
4. Subdivided into eight blocks--three wires (2^2,2^1, and 2^0).

The submodule block select lines are listed as carrying a binary value that is related to a subdivided block size of 8K bytes.

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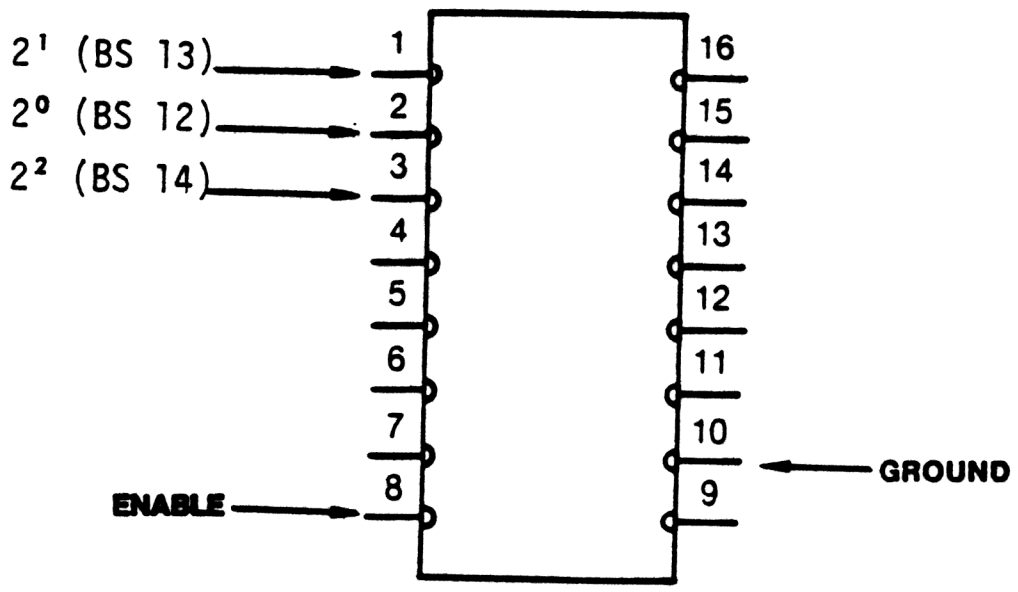


Figure 4-4. Memory Control Cable Connector Wiring

Submodule memory banking is implemented by connecting the external bank select lines, BS12- to BS14-, to the memory control connector (J2), and by installing resistor pack 1. Table 4-10 shows the switch settings required to provide the submodule banking configuration, and the switch setting to select operation in a LSI-2 series or NAKED MINI 4 Family environment.

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Table 4-10. Submodule Memory Banking Switch Settings

BANKING CONFIGURATIONS	SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	SW1-6
2 x 8 KB	ON	OFF	OFF	ON	OFF	ON
4 x 8 KB	ON	OFF	ON	OFF	OFF	ON
8 x 8 KB	ON	OFF	ON	OFF	ON	OFF
2 x 16 KB	OFF	ON	ON	OFF	OFF	ON
4 x 16 KB	OFF	ON	ON	OFF	ON	OFF
2 x 32 KB	OFF	ON	OFF	ON	ON	OFF
NO BANKING	OFF	ON	OFF	ON	OFF	ON

	SW2-1	SW2-2	SW2-4	SW2-5	SW2-6	SW2-7	SW2-8
ALL CONFIGURATIONS	ON	OFF	OFF	ON*	OFF	OFF	ON

NOTE: *SW2-5 is OFF for LSI-2 and LSI-3 systems

To implement submodule memory banking, resistor pack RP-1 and resistor R60 must be installed in the position corresponding to the desired size of each bank. See Figure 4-5 for detail and Figure 4-1 for the location of the resistor pack on the card. To retain the ability to reconfigure the module, use sockets for RP1 and R60. Using a soldering tool directly on the resistor or resistor pack may result in heat damage to it. Use seven eight-pin Single In-line Pin, (SIP) sockets. RP1 is a 10 ohm eight-resistor device. Use Dale LD16-01-100J or equivalent.

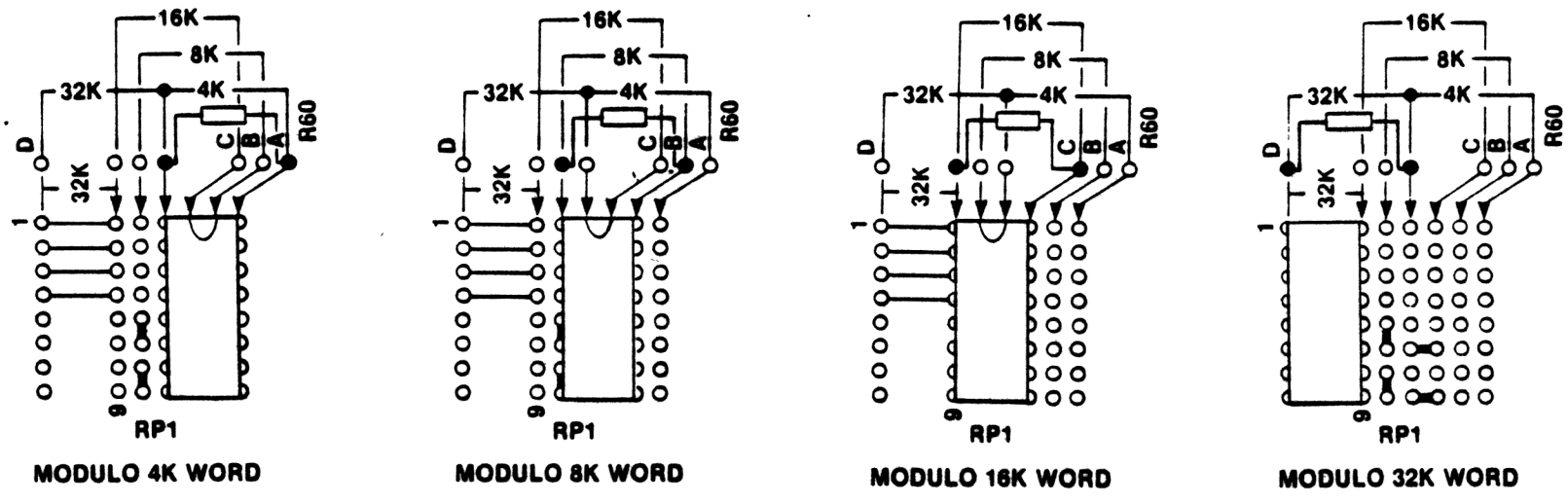


Figure 4-5. Sub-Module Memory Banking Resistor-pack Configuration

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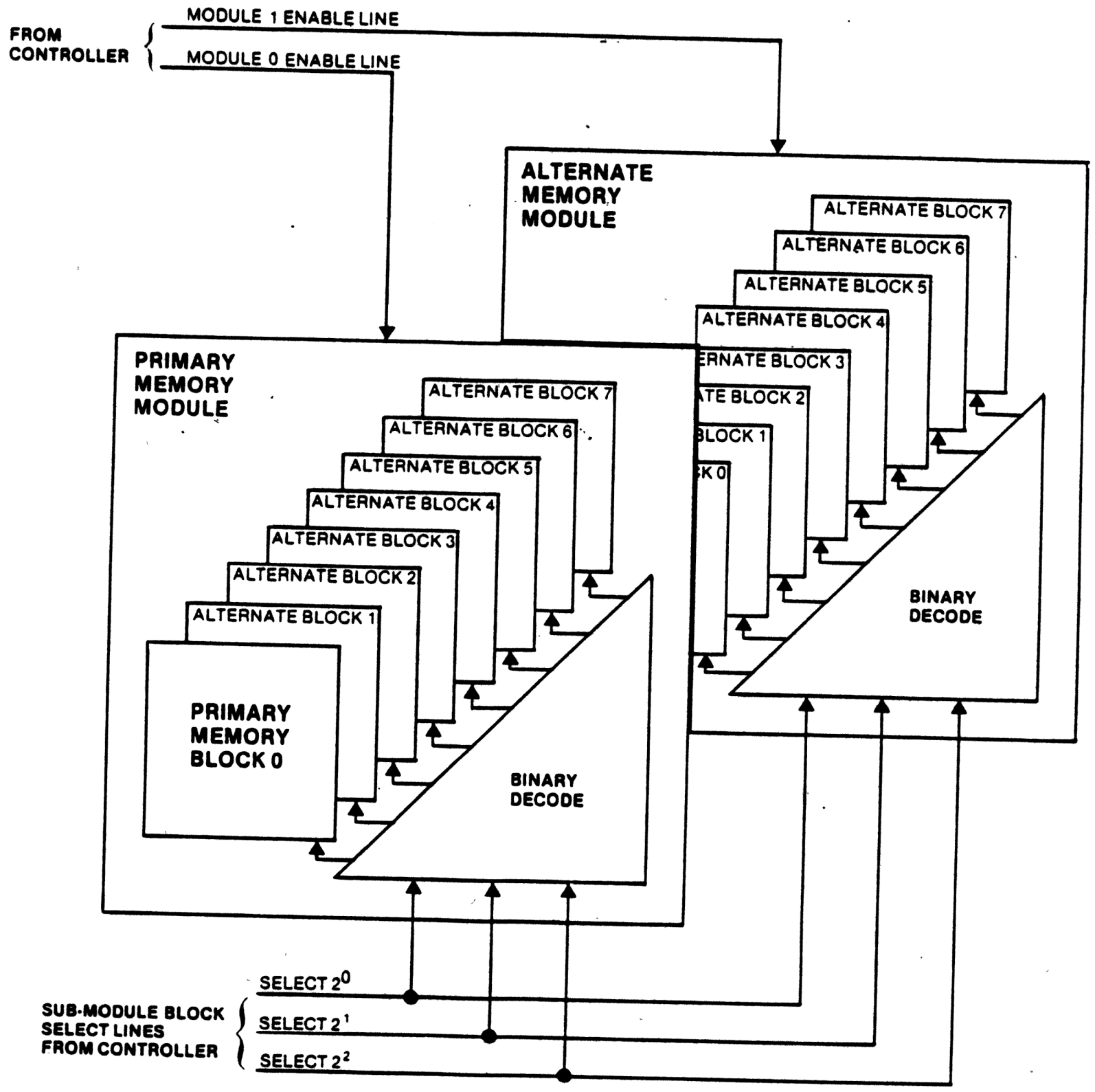


Figure 4-6. Module and Sub-Module Banked Memory Selection

4.2.3 Memory Features

This section describes two RAM module memory features: parity and refresh.

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4.2.3.1 Parity

Parity is a technique for checking the aceuracy of stored binary numbers. It can be used in two different ways:

1. As a normal internally-generated and internally-checked parity

2. As an 18-bit memory storing bits from an external source and supplying all 18 bits when read by the same source with no checking

The normal internally generated and checked parity method receives the 16 bits of data from the memory controlling source (processor or DMA controller) and internally reads the 16 bits of data, recomputes parity, and compares it to the stored parity bits. It supplies only the 16 bits to the controlling device. If an error occurs, the memory is inhibited from responding with MACK.

The external parity selection operates when the EXEC- signal is driven low at the same time as the MST- signal. The memory receives externally generated parity along with the 16 bits of data and stores all the bits like a normal operation. This feature is intended to be implemented by a user-designed DMA I/O distributor.

When reading data from the memory, the EXEC- signal must again be driven low to allow the memory controlling device to read its supplied parity data bits along with the 16 data bits. The memory module does no parity checking in the external mode.

4.2.3.2 Refresh

The memory board uses cycle stealing refresh that is asynchronous to normal memory operation.

A memory busy flip-flop indicates that a memory cycle, either refresh or normal, is underway. If a refresh clock signal occurs while the memory is busy with normal operation, it is stored. At the end of a normal memory cycle the refresh cycle is started. If the memory is not busy with a normal cycle when the refresh clock signal occurs, the refresh cycle is started without delay.

The refresh clock has a period of approximately 25 microseconds.

The memory supplies a refresh address and retains the new refresh address for the next refresh cycle.

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4.2.4 Power Fail Sequence

Semiconductor RAM memories are volatile in nature. That is, they can lose data if the supply voltage from the computer drops below a preset "safe" level. For this reason, all NAKED MINI 4 Family memories that contain semiconductor RAM are equipped with invalid data detection logic. If the voltage being supplied to the board drops below the "safe" level, the invalid data detection indicates whether the integrity of the data has been maintained.

4.2.4.1 With Battery Backup Option Installed

If the supply voltage does drop below the safe level, the memory disable signal will switch the board to battery backup power if this option is installed (Section 6).

4.2.4.2 Battery Backup Exhausted or not Installed

If battery backup is not present or has elapsed, the invalid data detection logic will set an internal memory flip-flop, called Invalid Data Detect (IDD). The IDD flip-flop disables RAM on the board and causes it to respond to any subsequent memory read operation by putting all zeros (no-op instructions) on the data bus.

All NAKED MINI 4 Family memories are connected together by the ALSP- line. If one memory loses RAM power, the IDD flip-flop is set, and the ALSP- line is driven low. Each semiconductor memory in the system receives the AL- line and sets its own IDD flip-flop.

4.2.4.3 At Power Return

When power returns, the RAM will remain disabled until the IDD flip-flop is reset. This resetting can be accomplished by writing into any memory location (e.g., AutoLoad). Once IDD is reset, normal operation is resumed.

4.3 MODEL 53775, HALF CARD SEMICONDUCTOR RAM

Computer Automation, Inc., produces a half card semiconductor RAM memory module designed for interface with all NAKED MINI 4 Family computers. The module is designated 53775 and is described in this section. Model 53775 is available in 32K byte, 64K byte, and 128K byte configurations (Table 4-11).

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Table 4-11. Memory Identification, Model 53775

MODEL	DESCRIPTION
53775-16	32K Byte RAM with Battery Backup
53775-32	64K Byte RAM with Battery Backup
53775-64	128K Byte RAM with Battery Backup

These cards feature CPU-transparent refresh and are designed to work with the power-up features of the NAKED MINI 4 processors. In the event of a power failure where memory integrity is lost, the RAM card presents NOP instructions (:0000) to the CPU, thereby forcing it to "bubble up" to the first non-RAM location in memory above the card. This location should then contain the restart sequence. However, on a 128K byte RAM system, the CPU would continue to cycle through NOPs, until the outside world stopped it. The RAM is enabled by performing a write operation to the module.

4.3.1 Specifications

This topic presents specifications for RAM memory Model Number 53775.

4.3.1.1 Memory Cycle Times

A minimum cycle time occurs if a cycle-stealing refresh cycle is started at the end of a normal memory cycle. A "worst-case" or maximum-cycle time occurs if a refresh cycle is started at the beginning of a normal cycle time. Since refresh cycle time is equal to normal memory cycle time, the maximum cycle time is equal to double the total minimum cycle time. The minimum cycle times are summarized in Table 4-12.

Table 4-12. Memory Cycle Times, Model 53775

Access Interval	470 ns
Overhead Interval	110 ns
Cycle Time	580 ns

4.3.1.2 Environmental

Environmental specifications for Model 53775 are summarized in Table 4-13.

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Table 4-13. Environmental Specifications, Model 53775

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Noncondensing)	5 to 90

NOTE

At least 200 linear feet per minute of free air flow around the unit is required to provide adequate cooling.

4.3.1.3 Physical

Physical specifications for Model 53775 are summarized in Table 4-14.

Table 4-14. Physical Specifications, Model 53775

Length	42.88 cm (16.88 in.)
Width	19.05 cm (7.5 in.)

4.3.1.4 Electrical

Electrical specifications for Model 53775 are summarized in Table 4-15.

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Table 4-15. Electrical Specifications, Model 53775

Voltage Regulation (All Voltages)	±5%
Power Consumption with BBU +12 Vdc Operating Standby -12 Vdc Operating Standby +5 Vdc Operating Standby	 1.2 A 1.0 A 0.1 A 0.1 A 1.6 A 1.6 A
Power Consumption without BBU +12 Vdc Operating Standby -12 Vdc Operating Standby +5 Vdc Operating Standby	 0.5 A 0.1 A 0.1 A 0.1 A 0.8 A 0.8 A

4.3.2 Installation

Prior to removing or installing a module, it is essential to remove all power from the system. After powering down, any battery backup must be removed. Set the battery select switch (INT/EXT, S1) to INT. Next remove all battery connectors from the external battery connectors P3 and P4. Then switch the select switch to the EXT position.

CAUTION

Failure to disconnect battery backup power from a RAM module will result in damage to the RAM.

The RAM memory board has on-board MOS memory devices that are sensitive to static electricity. Caution should be used when handling or installing the module to insure the highest degree of reliability.

These modules are half card modules, and can be installed in either half card or full card chassis. If a module is to be installed in a half card chassis, no special preparation is needed for that purpose. However, for installation in a ful card chassis, the module must first be joined with another half card, such as another memory module or a half card processor card and propagation requirements of the MBIN/MBOT chain must be observed. Refer to the Chassis Configuration Reference Manual and Installation Guide for information on the joining of half cards.

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4.4 MODEL 53819

Computer Automation, Inc., produces a RAM semiconductor memory with error correction built on a standard full card. The board is available in the following configurations:

1. Model 53819-16--32K bytes of memory, available with the memory interleaving feature.

2. Model 53819-32--64K bytes of memory, available with submodule banking and interleaving features.

3. Model 53819-64--128K bytes of memory, available with the submodule interleaving feature.

Board level banking can be implemented on all models. All boards are equipped with battery backup.

4.4.1 Specifications

This topic presents specifications for RAM memory with error correction, Model Number 53819.

4.4.1.1 Memory Cycle Times

The maximum cycle times for read and write operations depend on whether error correction is required. Write operation cycle times also depend on whether the operation is performed in word or byte mode. In addition, all times assume that the operation does not overlap a refresh cycle. The cycle times are summarized in Table 4-16.

Table 4-16. Memory Cycle Times, Model 53819

Read	
Access (without correction)	380 ns
(with correction)	495 ns
Overhead (without correction)	140 ns
(with correction)	185 ns
Total (without correction)	520 ns
(with correction)	680 ns
Minimum Interleaved	480 ns
Write (word)	
Access	220 ns
Overhead	240 ns
Total	460 ns
Mimimum Interleaved	320 ns
Write (byte)	
Access	380 ns
Overhead	350 ns
Total	730 ns
Mimimum Interleaved	480 ns

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4.4.1.2 Environmental

Environmental specifications for Model 53819 are summarized in Table 4-17.

Table 4-17. Environmental Specifications, Model 53819

Operating Temperature Range (Degrees Celsius)	0 to 50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Noncondensing)	15 to 80

NOTE

Free air flow around the unit is required to provide adequate cooling.

4.4.1.3 Physical

Physical specifications for Model 53819 are summarized in Table 4-18.

Table 4-18. Physical Specifications, Model 53819

Length	42.88 cm (16.88 in.)
Width	38.10 cm (15.00 in.)
Height	1.52 cm (0.6 in.)
Weight	1.1 kg (2.5 lb)

4.4.1.4 Electrical

Electrical specifications for Model 53819 are summarized in Table 4-19.

4.4.2 Functional Description

The full card error correcting semiconductor memory consists of the following functional units:

1. Memory ICs and associated addressing circuitry
2. Error correction logic
3. Memory refresh circuitry
4. Memory banking and interleaving circuitry
5. Battery backup circuitry
6. MAXI-BUS Interface logic.

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Table 4-19. Electrical Specifications, Model 53819

Voltage Regulation (All Voltages)	±5 percent
Power Consumption--53819-64	
+5 V Maximum Operating	4.75 A
+12 V Standby	1.4 A
+12 V Maximum Operating	1.7 A
-12 V Maximum Operating	0.04 A
Power Consumption--53819-32	
+5 V Maximum Operating	4.50 A
+12 V Standby	1.3 A
+12 V Maximum Operating	1.6 A
-12 V Maximum Operating	0.04 A
Power Consumption--53819-16	
+5 V Maximum Operating	4.50 A
+12 V Standby	1.2 A
+12 V Maximum Operating	1.5 A
-12 V Maximum Operating	0.04 A

4.4.2.1 Memory ICs

The memory ICs are 16K x 1 RAMs, 21 RAMs per word, installed to a maximum capacity per board of 128K bytes. The 21 bit word length includes 16 data bits and 5 error checking bits. Only the 16 data bits are available on the MAXI-BUS Interface.

4.4.2.2 Error Correcting Circuitry

The error correcting circuitry generates 5 error check bits from the 16 data bits. A word is stored as 21 bits where the 5 appended bits are error bits EØ through E4. The error correcting algorithm maximizes two bit error detection and minimizes error bit generation and checking delays. The error correcting circuitry can be disabled for test purposes using a switch on the board.

The error check bits are generated when the data word is written into memory and error checking is performed when the word is read. All single bit errors are detected and corrected. If a single bit error is detected, corrected data is placed on the data bus. Correction of the data written in memory does not take place at this time, however, but during a refresh cycle. The circuitry cannot determine the bit locations of double or multiple bit errors. If a multiple bit error is detected, a memory configured for operation with NAKED MINI 4 processors does not acknowledge the access. A memory configured for operation with LSI-2 processors generates a parity error.

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Error checking is also carried out when a write operation is performed in byte mode. Before writing the byte, the error correcting circuitry checks the entire word already written in the addressed location for errors. If a single bit error is detected, a correction is made. The new byte is then substituted for the old, and the entire word written back into memory. If a multiple bit error is detected, processors and DMA devices react in the same manner as when a multiple bit error is detected during a word read operation. Because of the checking required, byte mode write operations require longer cycle times than word mode write operations. The cycle time for write operations in byte mode is identical whether or not an error is found.

4.4.2.3 Memory Refresh and Error Correction

A refresh cycle is performed an average of once every 15 microseconds. In addition, one word of memory is selected and checked for bit errors. Detection of a single bit error extends the refresh cycle to a read/modify/write cycle during which the word is corrected and written back into memory. Detected double bit errors are ignored. An error checking/correcting operation is performed on each word of memory at the following approximate intervals:

1. Model 53819-16--every 1/4 second
2. Model 53819-32--every 1/2 second
3. Model 53819-64--every second.

A detected error pulses a light on the rear of the board. A single bit hard error in one word will therefore pulse the light once every error checking/correcting cycle. Any soft error in the five checking bits will also pulse the light.

4.4.2.4 Memory Banking and Interleaving

The memory banking circuitry permits both external and internal memory banking. Memory interleaving can be implemented if installed memory on the 53819 module does not exceed 64K bytes, and total system memory does not exceed 128K bytes. Implementation of these features is described in Installation (this section). Interleaving and internal banking should not be implemented at the same time, since doing so produces undefined operation. Interleaving and external memory banking is permissible.

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4.4.2.5 Battery Backup

The full card error correcting semiconductor memory has an on-board battery backup unit that functions automatically if power is interrupted (Section 6). The battery backup unit has a 7.2 volt battery which can provide enough power to retain data for a minimum of two minutes. The user can also attach an external six volt source. Use of the internal or external source is switch selectable on the board.

A green LED lights when power is applied to the board +5 volt internal line. The source of the power can be the chassis supply or the battery back-up unit. The LED remains lit when power is within specifications.

4.4.2.6 MAXI-BUS Interface

The MAXI-BUS Interface contains the memory addressing circuitry and the data bus transceivers.

4.4.3 Installation

The full card error correcting semiconductor memory is a full card module, as shown in Figure 4-7. Special installation requirements for the module are described in this topic.

4.4.3.1 Module Installation

The source of battery backup power is selected using switch 1 (SW1). The switch is set to INT to select the on-board battery and EXT to select an external source. Set SW1 to EXT before removing modules from or installing modules in the chassis, and ensure that a battery is not connected to the external battery connector J4. With external batteries disconnected, SW1 is set to EXT. The board can then be inserted into or removed from the chassis.

CAUTION

Failure to disconnect external backup batteries and internal battery backup prior to removing or installing the module in the chassis can result in damage to the module. Chassis power should always be turned off when inserting boards into or removing boards from the system.

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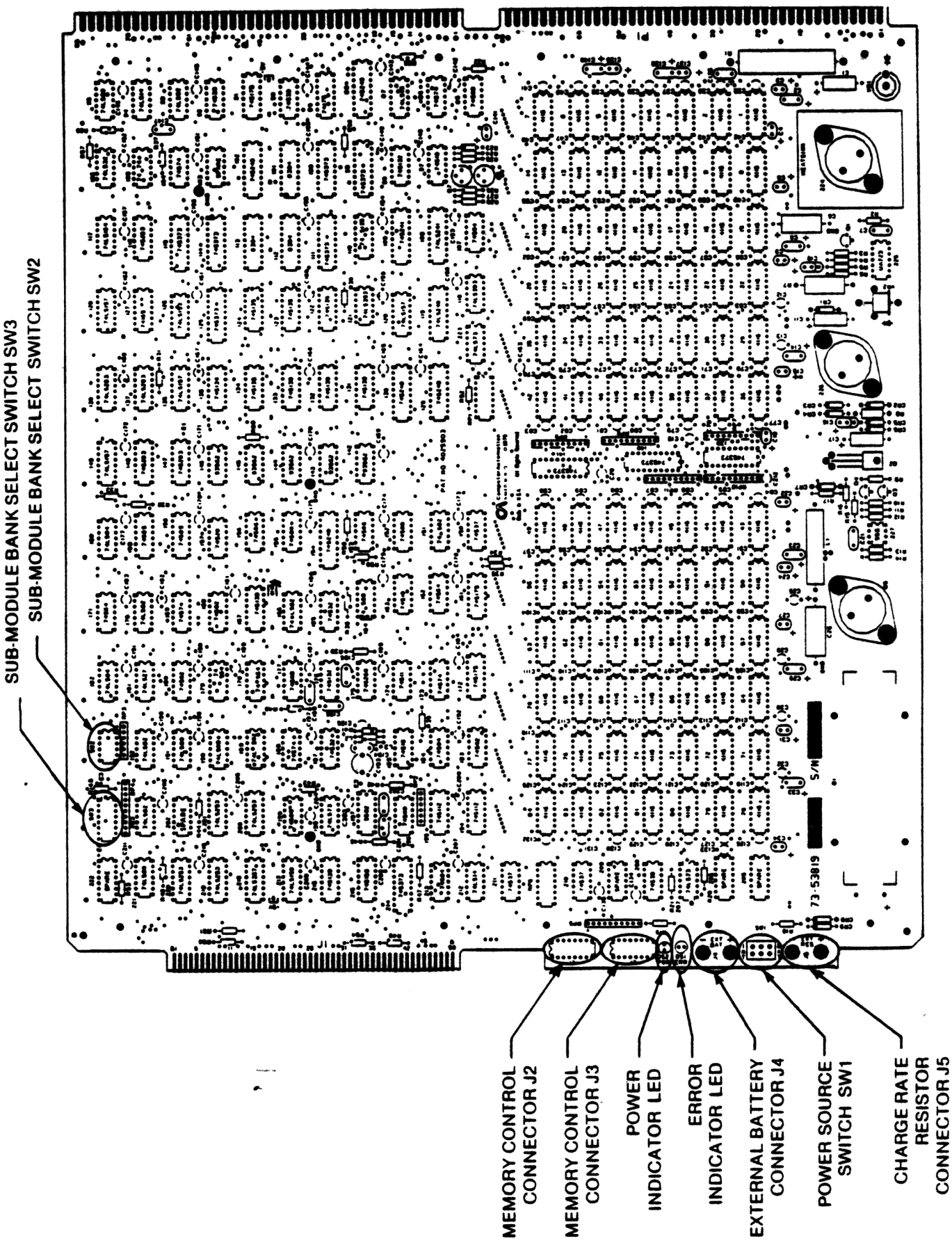


Figure 4-7. Full Card Error-Correcting Semiconductor Memory Board

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4.4.3.2 Interleaving Procedures

Each memory module in an interleaved pair is assigned either the odd or even addresses for the range of addresses covered by the interleaved pair. Two memory modules of the same size are interleaved with the odd memory address module closest to the processor on the MBIN/MBOT priority chain.

The strapping required for interleaving is made on the memory control connector header J2. Figure 4-8 shows the strapping pin locations. To select interleaved mode, install a jumper between pins 5 and 12 on each module. One memory module of each interleaved pair of memory modules must be strapped for the odd addresses by installing a second jumper between pins 6 and 11. Use AWG 24 to 28 (metric gauge 3 to 5) solid wire for the jumpers and solder all connections.

4.4.3.3 Memory Banking Procedures

The 53819-64 memory with 128K bytes of RAM memory is internally constructed as two 64K byte modules. These internal modules are designated A and B. The 53819-32 memory and the 53819-16 memory are depopulated versions of the 53819-64 memory. The 53819-32 memory contains A module memory only. The 53819-16 memory contains half the A module memory and can be strapped as a primary or alternate module. The A module can also be designated a primary module and the B module an alternate module. Switch settings on the board make various submodule banking configurations within the A and B modules possible. The 53819-32 module can be strapped as a primary or alternate module, with switch selected submodule banking configurations possible within the module. The 53819-16 memory allows board level banking as a primary or alternate module. Sub-module banking is not possible on the 53819-16 board.

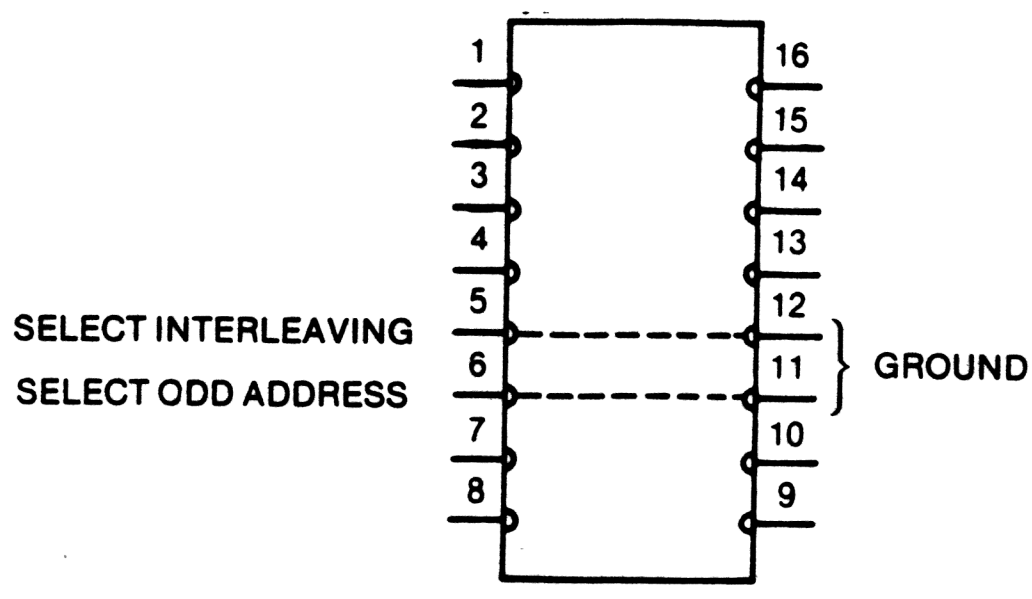


Figure 4-8. Memory Module Interleaving Strapping

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4.4.3.4 Module Memory Banking Strapping

The strapping required for memory banking is made on the memory control connector headers. The 53819-64 memory uses memory control connectors J2 and J3 to establish primary and alternate modules. If both connectors are strapped identically, the board acts as the primary or the alternate module, depending on the strapping used. Such strapping is not recommended, however, since it slows access to the memory. If modules A and B are to act as primary and alternate modules, module A must be strapped as the primary and module B as the alternate. The strapping of connector J2 determines the status of module A, and the strapping of J3 determines the status of module B. The 53819-32 board is configured using connector J2 only. The strapping required to establish a module as primary or alternate is shown in Figure 4-9.

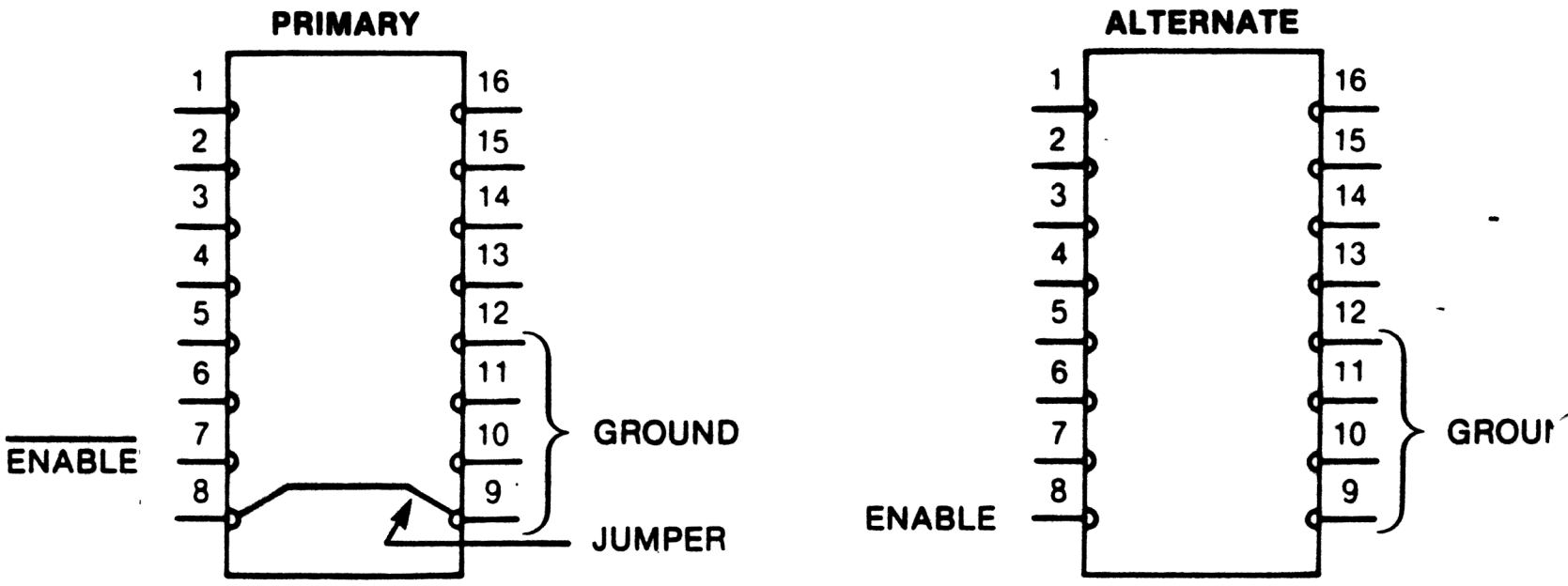


Figure 4-9. Control Cable Connector Wiring

NOTE

A Memory Banking Controller (MBC) can be initialized in two ways. When ENABLE- (Pin 7) is used, the MBC is initialized so that its output is all zeros. When ENABLE (Pin 8) is used, the MBC is initialized so that its output is all ones.

The primary module is enabled by the initialization value; thus, when ENABLE- (Pin 7) is used, 0 enables the MBC, or, when ENABLE (Pin 8) is used, 1 enables the MBC. In this publication, by convention, the primary module is assumed enabled by a low (ENABLE-) signal.

To change from primary to alternate, remove the jumper between pins 8 and 9, and move the enable wire from pin 7 to pin 8. To change from alternate to primary, move the enable wire from pin 8 to pin 7, and insert a jumper between pins 8 and 9. Use AWG 24 to 28 (metric gauge 3 to 5) solid wire and solder all connections.

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4.4.3.5 Submodule Memory Banking

Submodule banking on the 53819-64 memory is controlled through switches SW2 and SW3. The 53819-32 memory uses SW3 only. The functions controlled by the switch elements on SW3 and SW2 are shown in Figures 4-10 and 4-11.

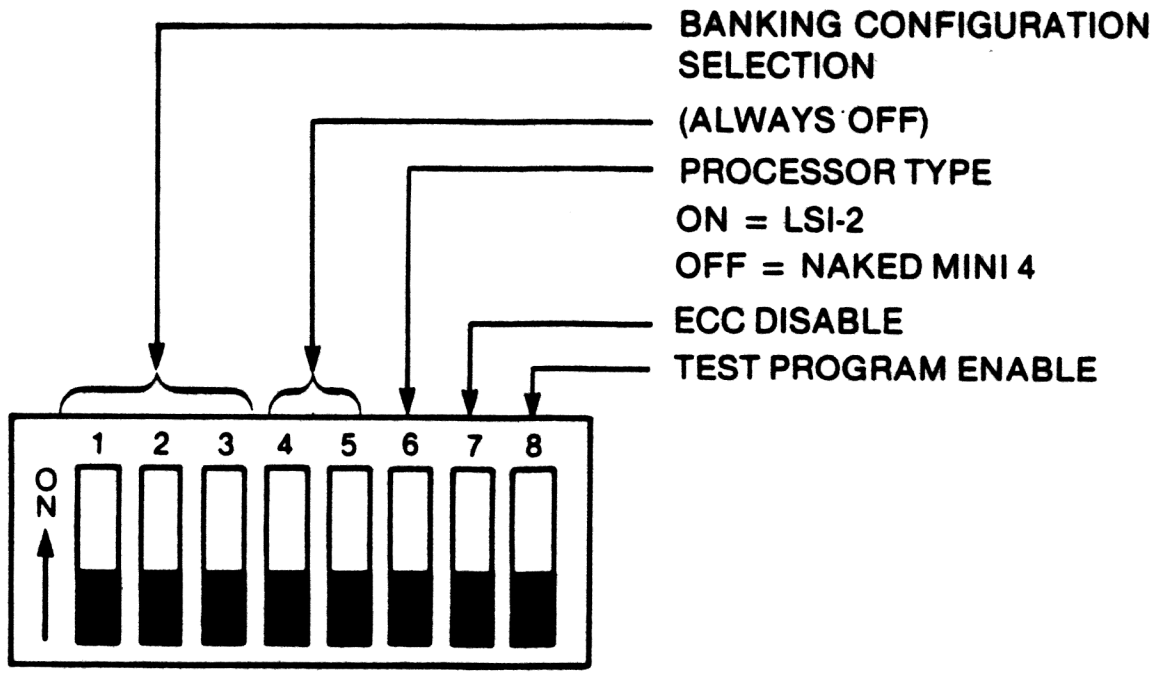


Figure 4-10. SW3, A Module Banking Control Switch Block

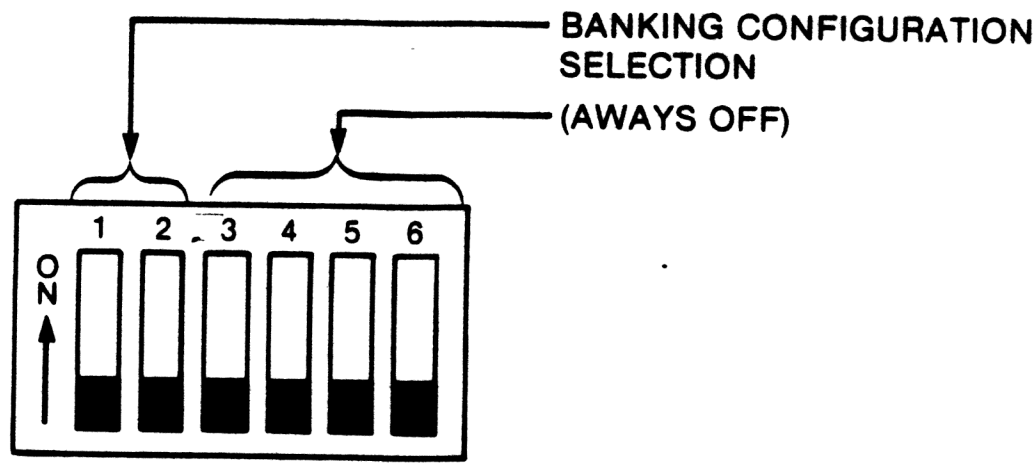


Figure 4-11. SW2, B Module Banking Control Switch Block

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Elements 1, 2, and 3 on SW3, and elements 1 and 2 on SW2 are used to control the sub-module banking configurations. The smallest block of addresses that can be selected through sub-module banking is 16K bytes. Sub-module banking configurations are built by designating some 16K byte blocks as primary and others as alternate memory. Only those blocks designated primary add to the total range of addresses allocated. The possible banking configurations for the A and B modules are shown in Figure 4-12. The switch settings required to implement each configuration are shown in Table 4-20. Any combination of switch settings not shown in the table produces undefined results. Configurations A, B, and C can be implemented independently in the A and B modules on the 53819-64 board. Configuration D combines the modules into one configuration. Each configuration adds the amount of address space shown only if the module enable line is asserted. If the enable line is not asserted, all blocks are banked as alternates. When using the D configuration, only the A module enable line is valid. The J2 connector may be strapped as primary or alternate memory. The strapping of the J3 connector is ignored.

When configuration B is implemented on the A module, it requires that switch element SW3-3 be ON. The corresponding element on SW2 is not required to implement this feature on the B module and should be OFF. Whenever the B configuration is used, the corresponding banking controller connector must have pins 1 and 3 jumpered together (connector J2 for the A module, connector J3 for the B module.)

Other switch elements are used as follows:

1. Element SW3-6 must be set to correspond with the processor used. The switch is set ON when using an LSI-2 Series processor. The switch is set OFF when using a NAKED MINI 4 Family processor.

2. Element SW3-7 is set ON to disable the error correction feature during testing. The element should be OFF during normal operation.

3. Element SW3-8 is set ON to enable the error correction test features of the test program. The element must be OFF for normal operation.

4. All other switch elements should be OFF. Setting other elements ON produces undefined results.

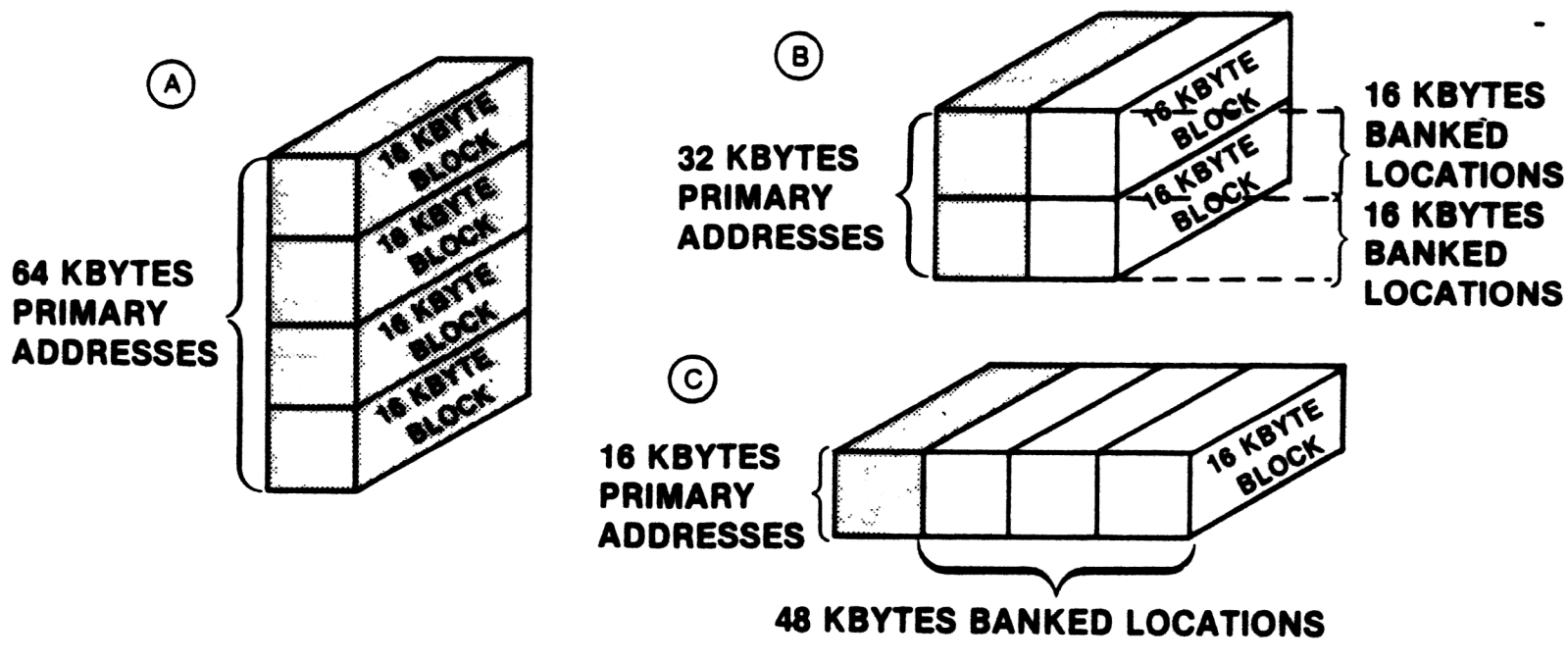
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Table 4-20. Submodule Banking Switch Settings

CONFIGURATION	ADDRESS SPACE SIZE	SW2-1	SW2-2	SW3-1	SW3-2	SW3-3
A 64K bytes	OFF	OFF	OFF	OFF	OFF	
B (2x16K)	32K bytes	ON	OFF	ON	OFF	ON
C (4x8K)	16K bytes	OFF	ON	OFF	ON	OFF
D (8x8K)	(See Text)	ON	ON	OFF	ON	OFF

A AND B MODULE CONFIGURATIONS (MODULE ENABLE LINE = O)



A AND B MODULE COMBINED CONFIGURATIONS (A MODULE ENABLE LINE = O)

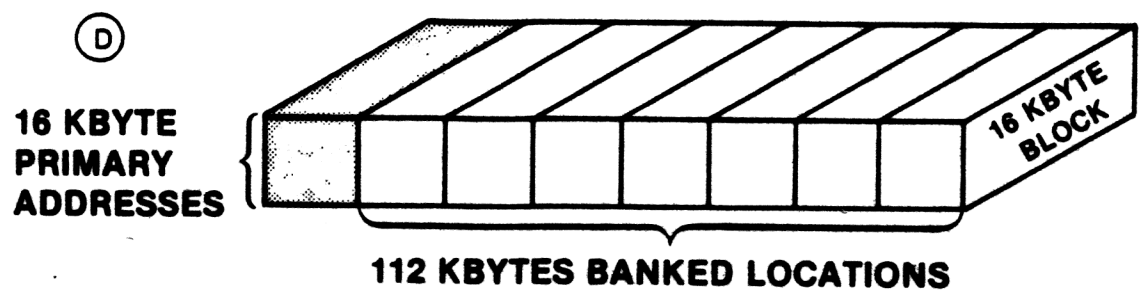


Figure 4-12. A and B Module Banking Configurations

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4.4.3.6 Submodule Banking Selection

Individual submodules are addressed through the bank select lines wired to the memory bank controller connectors. The J2 controller is used to select between A module submodules, and between all submodules in the 16K byte x 8 configuration (configuration D). Three bank select lines are used with configuration D. BS15A should not be used in any other configuration. Using BS15A in the A, B, or C configurations will interfere with memory operation. The J3 controller is used to select between B module submodules. The location of the bank select lines on the memory banking controller connectors is shown in Figure 4-13. The requirements for adding wires are as follows:

1. Submodule banking disabled--no wires
2. Subdivided into two blocks--one wire (2^1)
3. Subdivided into four blocks--two wires (2^1 and 2^2)
4. Subdivided into eight blocks--three wires (2^1, 2^2, and 2^3)

The figures shown in parentheses are the relative binary values of the data bits used to address the bank select lines.

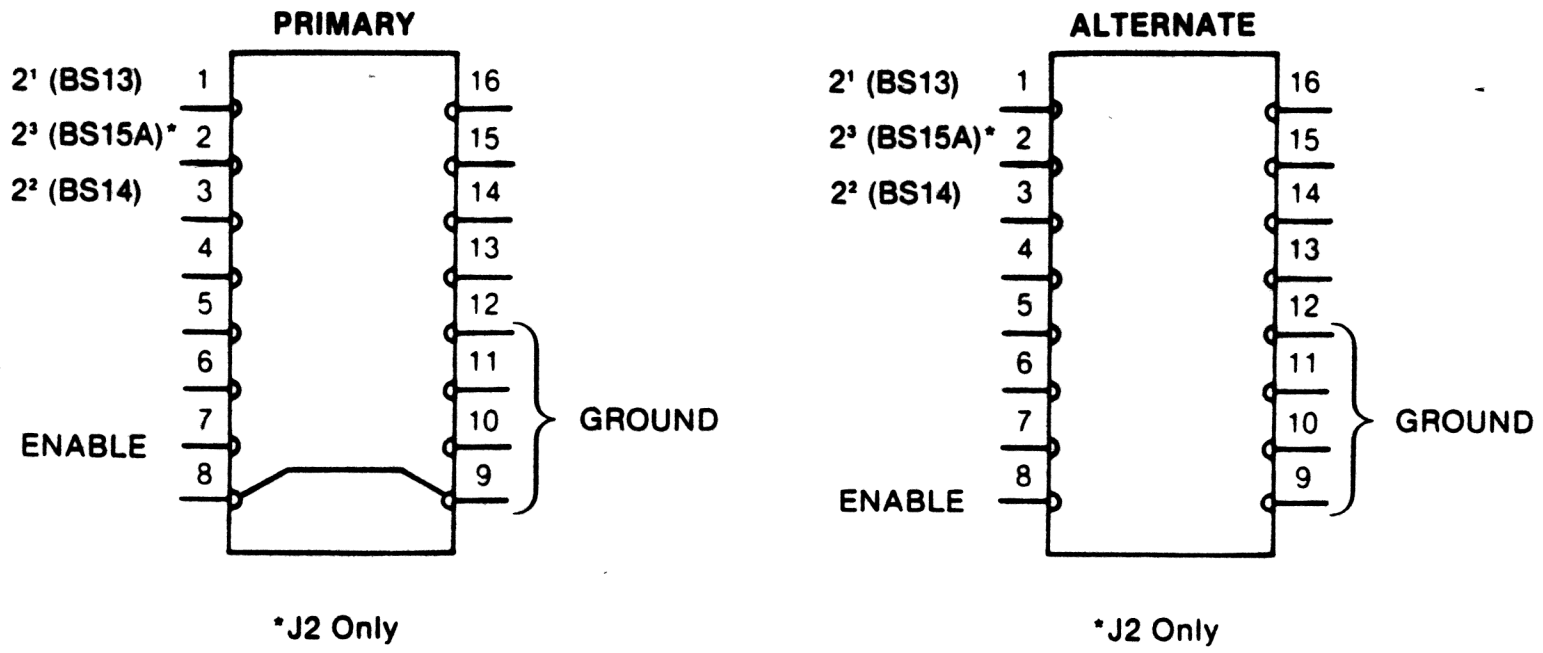


Figure 4-13. Bank Select Lines, Memory Banking Connectors

4.4.3.7 Module Enables

The state of the module enable signals depends on the inputs to pins 7 and 8 on the memory banking connectors J2 (module A) and J3 (module B). The pins are wired so that the modules are enabled if the pins are unconnected. If the pins are driven by the memory controller, the signals on pin 8 (enable high) and pin 7 (enable low) must not conflict or undefined operation and possible damage to the memory controller can occur. The input buffer configurations for the module enable signals are shown in Figure 4-14. The buffers are open collector.

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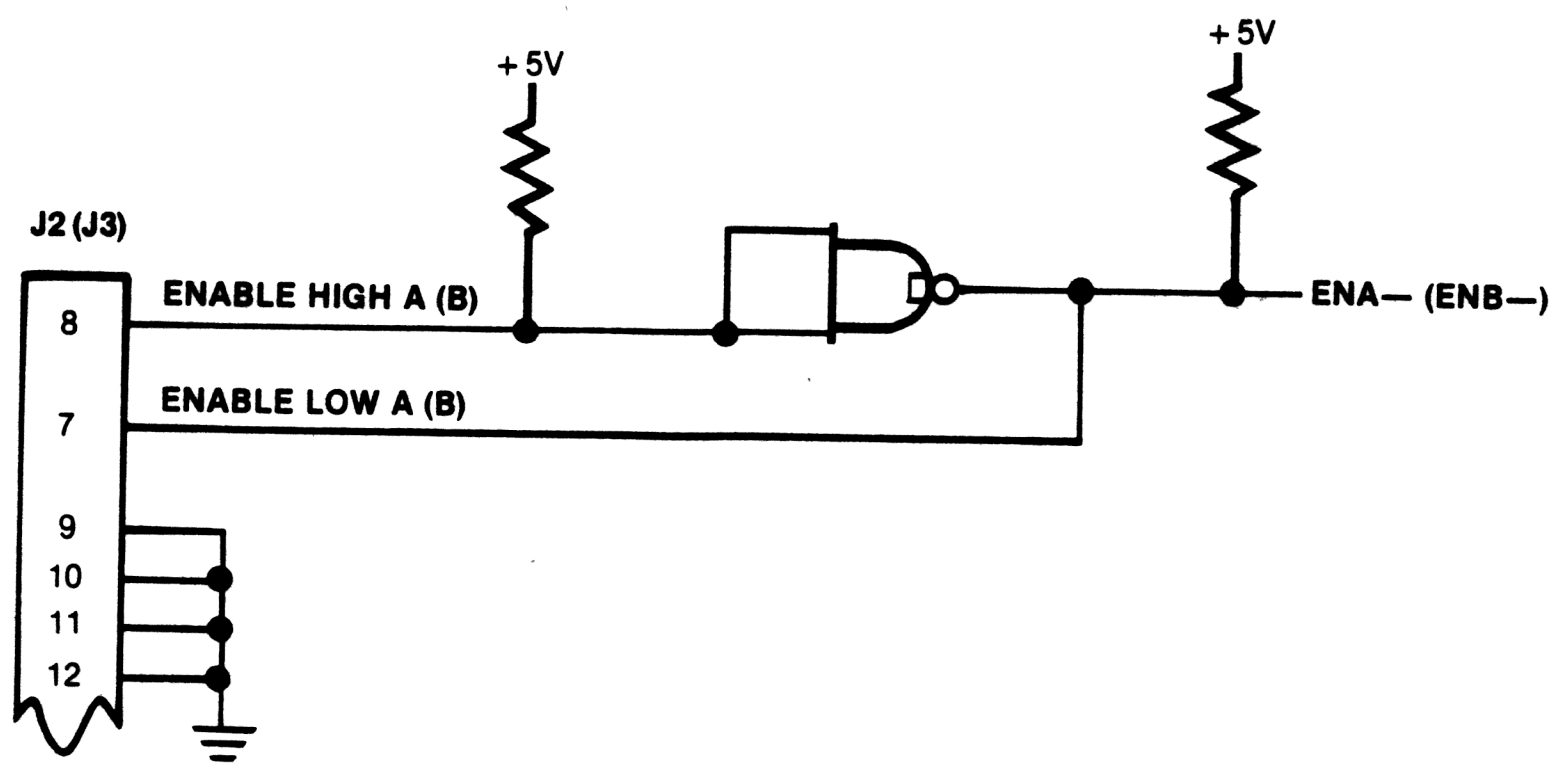


Figure 4-14. Module Enable Signal Logic

4.4.4 Power Fail Sequence

Semiconductor RAM memories are volatile in nature, which means that they lose data if the supply voltage from the computer drops below a preset level. For this reason, all NAKED MINI 4 Family memories that contain semiconductor RAM are equipped with invalid data detection logic. If the voltage supplied to the board drops below the "safe" level, the invalid data detection indicates whether the integrity of the data has been maintained.

4.4.4.1 With Battery Backup Option Installed

If the supply voltage does drop below the safe level, the memory disable signal switches the board to battery backup power.

4.4.4.2 Battery Backup Exhausted or not Installed

If battery backup is exhausted, the invalid data detection logic sets an internal memory flip-flop called Invalid Data Detect (IDD). The IDD flip-flop causes the memory to respond to any subsequent memory read operation by putting all zeros (no-op instructions) on the data bus.

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All NAKED MINI 4 Family memories are connected together by the ALSP- line. If one memory loses RAM power, the IDD flip-flop is set, and the ALSP- line is driven low. Each semiconductor memory in the system receives the ALSP- line and sets its own IDD flip-flop.

4.4.4.3 At Power Run

When power returns, memory will continue to return all zeros until the IDD flip-flop is reset. This resetting can be accomplished by executing any store instruction to an installed memory location in RAM. Once IDD is reset, normal operation is resumed.

4.4.5 Test Mode Programming

The 53819 memory board can be placed in a test mode in which the error correcting bits are written independently of the data bits. The test mode is enabled by placing switch element SW3-8 in the ON position. The write error correcting bits only feature is then turned on and off using appropriate select and present instructions. Select and Present (SELP) instructions have the following format:

```
SELP  R,Device Address + Function Code
```

where: R = the A, Q, X, or Y register.

The device address has an absolute value of 1 and the function code a value of 0. In machine language the Device Address and Function Code (DAFC) occupy the lower byte of the instruction word. The function code occupies the three least significant bits and the device address the upper five. Consequently, an absolute device address value of 1 means setting bit 3 of the instruction word. To establish the correct value, the following assembly language statements can be used:

```
ADBAS  EQU  1
ADFNL  EQU  ADBAS%3
```

The first statement equates the mnemonic ADBAS to the value 1. The second statement equates the mnemonic ADFNL to ADBAS shifted left three places. The Select and Present instruction then takes the form

```
SELP  R,ADFNL
```

Alternatively, the statement

```
SELP  R,8
```

can be used.

It is important to note that the device address 1 is not a dedicated address. Any device in the system that responds to a Select and Present instruction and is assigned device address 1 responds to the instruction shown. For this reason, caution must be exercised to avoid a conflict between two identically addressed devices.

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The write error correction bits only function is turned on by setting the most significant bit of the selected register to 1 and outputting it using the Select and Present instruction shown. The function is turned off by resetting the register bit to 0 and outputting it with the same instruction.

4.4.6 Error Correction Circuitry Testing

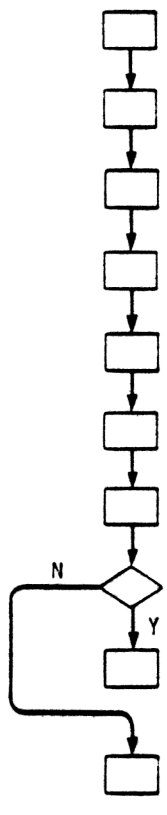
Error correction test circuitry can be tested for proper functioning in two ways. By turning on the write error correction bits only function, the error correction bits can be changed to correspond to a value one bit different than actually stored at a given location. A read operation should cause the data to be "corrected" to the value indicated by the error bits. Syndrome codes can also be used to generate specific error correction bit values. When the error bits are written with a syndrome code, a read operation should cause the error bits to be corrected to correspond with the value of the data word at that memory location. A flow chart of the first procedure is shown in Figure 4-15, and a flow chart of the second procedure is shown in Figure 4-16. The syndrome codes are given in Table 4-21. The procedure shown in Figure 4-16 "walks" a bit across the error correcting bits. Combinations of error bit settings can be generated by exclusive ORing of the codes.

Table 4-21. Error Correction Bit Syndrome Codes

ERROR CORRECTION BIT	SYNDROME CODE
0	:10
1	:0E
2	:0D
3	:0B
4	:07

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Enable write error correction bits only function (switch SW3-8 on).

Turn function off with select and present instruction (selected register DB15=0).

Write selected memory location with data pattern :8000.

Turn function on with select and present instruction (selected register DB15=1).

Write selected memory location with data pattern 0000

Turn function off with select and present instruction (selected register DB15=0).

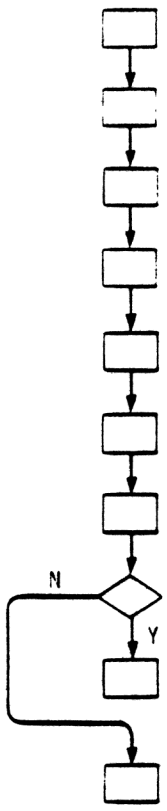
Read selected memory location?

Does the data pattern read :0000?

Write selected memory location with next data pattern .

Error correcting circuit failure indicated.

Figure 4-15. Error Circuitry Checking Through Data Pattern Correction.



Enable write error correction bits only function (switch SW3-8 on).

Turn function off with select and present instruction (selected register DB15=0).

Write selected memory location with data pattern :0000.

Turn function on with select and present instruction (selected register DB15=1).

Write selected memory location with syndrome code :10

Turn function off with select and present instruction (selected register DB15=0).

Read selected memory location?

Does the data pattern read :0000?

Write selected memory location with next data pattern

Error correcting circuit failure indicated.

Figure 4-16. Error Correction Circuitry Syndrome Test

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4.5 MODEL 53988

The MAXI-BUS® Expandable Memory Board (model 53988) is available in two different types:

1. Without banking capabilities, with 128K bytes of memory.
2. With banking capabilities in three sizes (128K, 256K, and 512K bytes of memory).

Both types have parity and provisions for external battery backup. Interleaving is not allowed on any of these modules. Table 4-22 summarizes the available configurations.

Table 4-22. Model 53988 Available Configurations

MODEL	DESCRIPTION
53988-00	128K bytes without banking
53988-01	128K bytes with banking
53988-02	256K bytes with banking
53988-03	512K bytes with banking

4.5.1 Specifications

This section presents specifications for the MAXI-BUS Expandable Memory Board.

4.5.1.1 Memory Cycle Times

If a refresh cycle is requested, a minimum cycle time occurs after a normal memory cycle (read or write) has begun. However, if a memory access request has to wait for a refresh cycle to end, the memory cycle time is twice the minimum memory cycle time. Table 4-23 summarizes the minimum cycle time.

Table 4-23. Memory Cycle Time

Memory Access Time (1)	350 ns
Memory Cycle Time (2)	500 ns

(1) Memory access time is defined as the time from Memory Start (MST) going true, to Memory Acknowledge (MACK) going true.

(2) Memory cycle time is defined as the time from Memory Start (MST) going true, to MST going true again (in request for another cycle).

4.5.1.2 Electrical Characteristics

The electrical specifications for the model 53988 board are summarized in Table 4-24.

Table 4-24. 53988 Electrical Characteristics

CAPACITY	ACCESSED +5V & +5VI*	NOT ACCESSED +5V & +5VI*	BACKUP +5VI*
128K bytes	5.0 amps	4.5 amps	1.5 amps
256K bytes	5.5 amps	4.7 amps	1.7 amps
512K bytes	6.0 amps	5.0 amps	2.0 amps

* "I" denotes internal voltage.

4.5.1.3 Environmental Characteristics

Temperature: 0 to 50 degrees centigrade
Humidity: 10% to 90% (non-condensing)
Voltage: 5 Volts ±5%

4.5.1.4 Physical Characteristics

The model 53988 is a half-card board with the following dimensions:

Length: 43.53 cm. (17.136 in.)
Width: 19.00 cm. (7.480 in.)

4.5.2 Functional Description

This section describes the operation of the MAXI-BUS Expandable Memory Board.

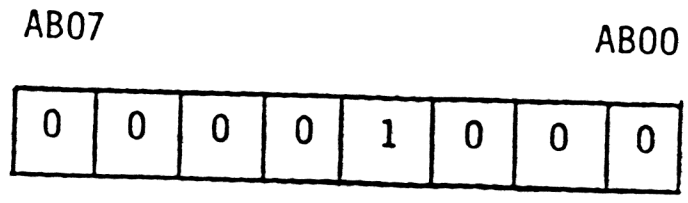
4.5.2.1 Banking Control

The 53988 provides for memory expansion in the standard MAXI-BUS (with the non-split backplane) through banking. Banking allows blocks (or banks) of memory to be brought into a small address space from a large memory space. The programmer has control over which banks of memory make up the logical address space of the machine at any one time. While the 53988 may have 512K bytes of memory, only 128K bytes are directly addressable at one time. The data in memory are not changed when banks are changed.

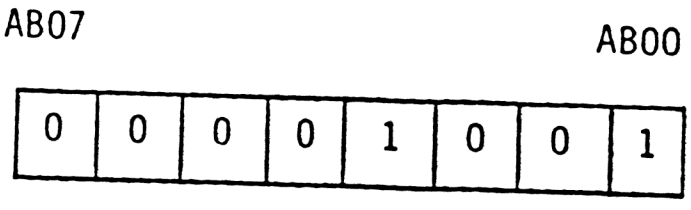
The banking control logic on the 53988 divides the logical address space into sixteen 8K byte blocks. A control register is associated with each block. The content of the control register is the address of the 8K byte block of physical memory occupying the block associated with the register

A system can contain up to four 53988 memory boards. The board provides the user with four configurable banks of memory and one non-configurable default bank. At power up, the default bank is active and consists of the first 128K bytes of physical memory in the system. In order to use the four configurable banks, the user must first initialize the banks by executing sixteen OUT instructions to each of the four banks. Only the banks being used need to be initialized. The form of the OUT instruction is as follows:

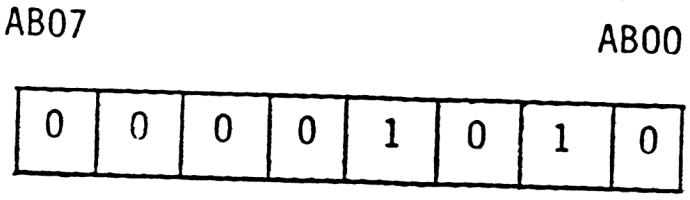
OUT to DAFC 8 (Bank 0)



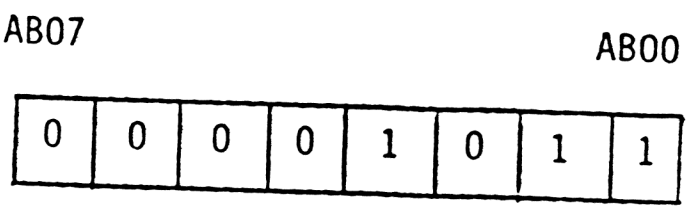
OUT to DAFC 9 (Bank 1, assigned to DMA operations via SACK jumper setting)

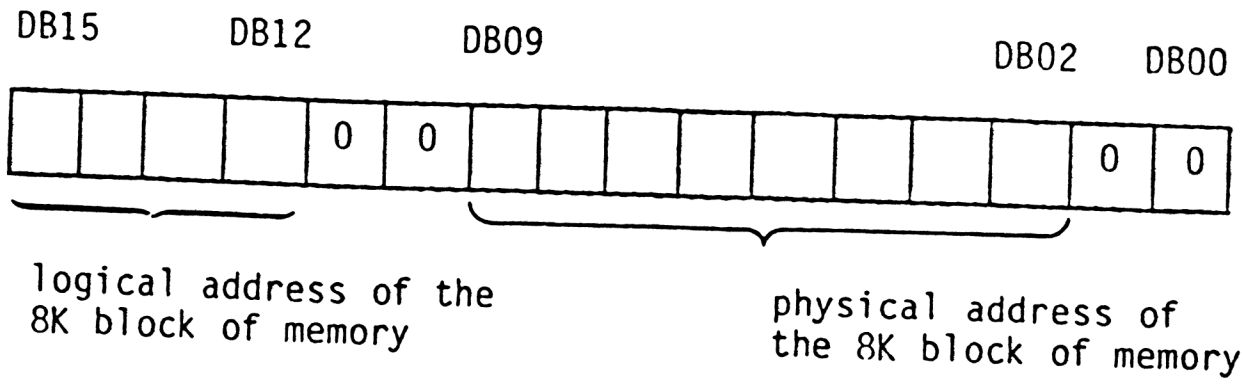


OUT to DAFC A (Bank 2)



OUT to DAFC B (Bank 3)





Each OUT instruction controls an 8K byte area of logical memory. The process of configuring a bank consists of storing the physical address of the 8K byte block of memory that is selected to reside in the logical address space in the register. According to the above OUT format, data bits 12 through 15 represent the logical address of the 8K byte block in the logical address space, and data bits 2 through 9 represent the physical address of this 8K byte block of memory. There are a maximum of 256 such 8K byte blocks possible in the system (2MB divided by 8K bytes). Address bits AB00 through AB11 allow access to one memory location out of the 4K locations in the system (4K words equals 8K bytes).

After initializing the banking registers to select the physical memory area, banking is enabled by a SELP (Select and Present) command to DAFC 9. (See Section 4.5.2.4, Switch Settings.) The data field for the SELP command is as follows:

SELP to DAFC 9 (for all bit charts below)

DB15 DB02 DB00

0	0	0	0	0	0	0	0	0	0	0	0	0			

BS2 BS1 BE

DB02 DB00

X	X	0

Banking disabled (default bank enabled)
(X denotes a don't care condition)

0	0	1

Bank 0 enabled

0	1	1

Bank 1 enabled

1	0	1

Bank 2 enabled

1	1	1

Bank 3 enabled

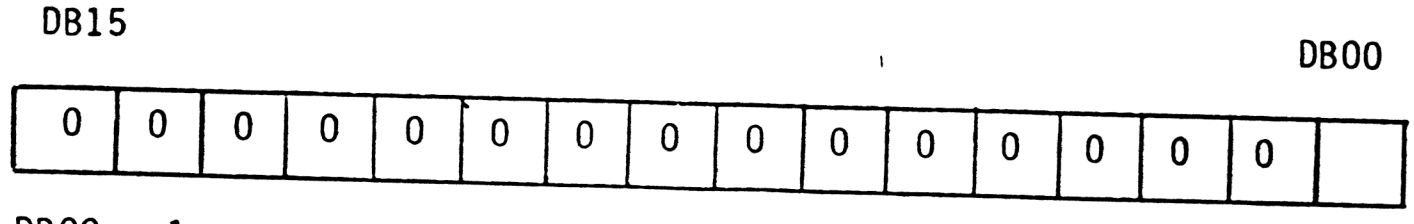
On power-up, all bits (DB00 - DB02) are set to 0, therefore going to the default bank, with banking disabled. If the board is jumpered with SW1 - 8 to the on position, it will automatically select Bank 1 for DMA operations.

For example, if the processor is operating from Bank 0 when a request for the bus goes true, when the processor gives up the bus (Stop Acknowledge, SACK going true on the MAXI-BUS), then the DMA operation begins and Bank 1 is selected. At the end of the DMA operation, when SACK goes false, bank 0 will be selected again and the processor can continue.

4.5.2.2 Parity

The 53988 is equipped with byte parity. A single parity bit is associated with each byte in memory. In case of a parity error, the red LED on the board is turned on. Parity can be enabled or disabled by software using a SELP command to DAFC 8.

SELP to DAFC 8



DB00 = 1 = parity enabled DB00 = 0 = parity disabled

At power up, parity is disabled (DB00 = 0) until it is enabled by the above command. Once enabled, the parity remains enabled until the above command disables it (RST will not disable parity).

The methods for reporting a parity error differ for Naked Mini 4 (NM4) and LSI-2 systems:

NM4 users: An error in either byte will cause the memory to withhold MACK in a word read cycle. An error in the selected byte will cause the memory to withhold MACK on a byte read cycle. A write cycle to a valid address will never withhold MACK. Withholding MACK will cause the processor's deadman timer to expire and enter the uninstalled memory trap at location :88 - :8B.

LSI-2 users: An error in either byte during a word read cycle will cause the memory to assert IL1. When the processor asserts IAR (Interrupt Address Request), the memory will drive data bit 4 (DB04) which defines the interrupt as a memory exception. An error in the selected byte during a byte read cycle will assert IL1 as above. A write cycle to a valid memory address will never cause IL1 to be asserted. The memory will never withhold MACK when set to LSI-2 mode.

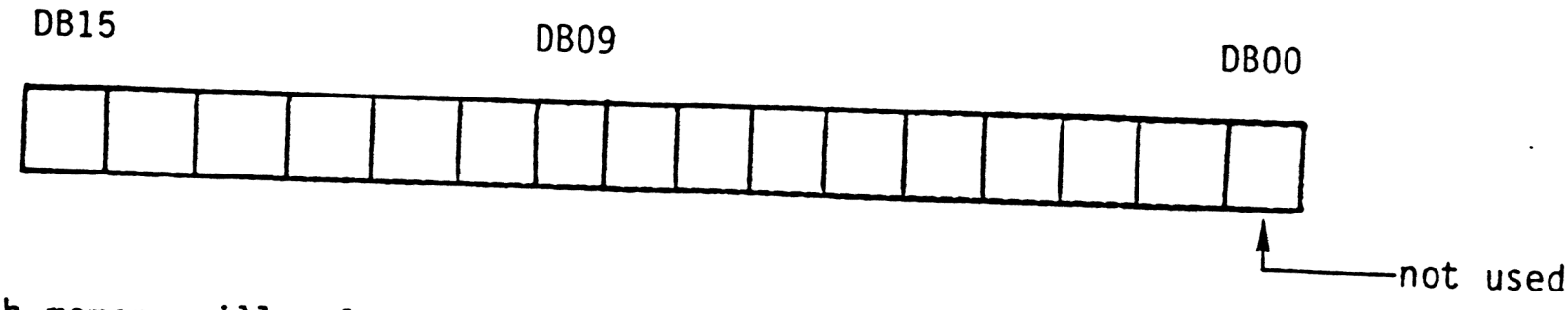
4.5.2.3 Autoload/Sourpower

The 53988 has an autoload/sourpower circuit that monitors the +5VI (+5 volt internal) and will indicate whether it has dropped below 4.5 volts. If power has dropped below the limit or if this is a cold start, the ALSP line is driven true indicating that memory data are invalid. The ALSP signal is driven to false after the first write to memory (when MACK goes true).

4.5.2.4 Memory Banking Configuration/IN Instruction

An IN instruction is used to inform the system of the types of memory in the system. The format of the IN instruction is as follows:

IN to DAFC 8



Each memory will only drive one bit in the field at any time (a wired "or" exists on the data bus so that more than one board can drive a given bit).

The 53988 drives DB09 high in response to an IN to DAFC 8, reporting that the board has 4 banks with 16 blocks per bank, and a granularity of 8K bytes (4K words) per block.

4.5.2.5 Switch Settings

Throughout this document the following switch setting for SW1 is assumed:

SW1-2 is on, with all other settings of SW1 being off (device address = 1).

It is recommended that the SW1 switch setting be kept as shown above. However the user may choose a different setting (therefore a different device address) than above as long as no other device in the system has this device address (note that all the 53988's in a system must have the same device address). Therefore if another device address is chosen, the instruction format must be changed accordingly from those listed here.

4.5.2.6 Refresh

The refresh circuitry uses a 20 MHZ (50 ns period) crystal oscillator as a basis of a refresh request. Refresh is performed once every 12.5 microseconds.

4.5.3 Installation

The 53988 board can be used only in systems with a non-split backplane. Since the board uses I/O commands, it is also treated as an I/O device. The board is used on the 200 side of the motherboard if there are available slots for it and it can be used on the 100 side only if all the slots in the 200 side are full. The board cannot be used on the 100 side if there are any unused slots on the 200 side of the motherboard.

NOTE

For dataCASE/5 systems with the non-split motherboard, the memory may be installed in either the 100 or 200 side. There should be no unused slots adjacent to the left most, or processor slot (this breaks the priority chain MBIN).

4.5.3.1 Battery Backup

The battery backup switch (SW2) and connector J2 allow external battery backup operation.

Battery backup mode:

SW2 should be in the "BBU" position and J2 should be connected with a cable to the backup source (the input to this board should be fully regulated since there is no onboard regulation for the input). In this case, only the memory chips (RAM IC's) plus a few associated logic gates are supported by the backup.

No battery backup mode:

SW2 should be in the "NBBU" position, and J2 is not used. The board gets its power (+5V) from the backplane.

4.5.3.2 SW1 Switch Setting

SW1 is used to set the device address, to select Bank 1 for all DMA operations, and to determine what computer (LSI2 or Naked Mini 4) the 53988 will be used in.

The SW1 positions are defined as follows:

SW1-1: Reserved and should be in OFF position.

SW1-2: Set the device address.

SW1-3: Set the device address.

SW1-4: Set the device address.

SW1-5: Set the device address.

SW1-6: Set the device address.

SW1-7: ON position for LSI-2 systems and OFF position for NM4 systems.

SW1-8: The ON position selects bank 1 (second bank) for all DMA operations. (In this case, bank 1 can also be used for non-DMA operations.)

The OFF position does not select any particular bank for DMA operations and, in the event of a DMA operation, the current working bank will be used.

4.5.3.3 Device Address Switch Setting

SW1-2 through SW1-6 set the device address. The default or recommended device address is :01 (SW1-2 being ON, all others being OFF). Other device addresses may be used as long as these addresses are not used by any other device in the system. Figure 4-17 shows the Device Address Function Code settings for SW1-1 through SW1-6.

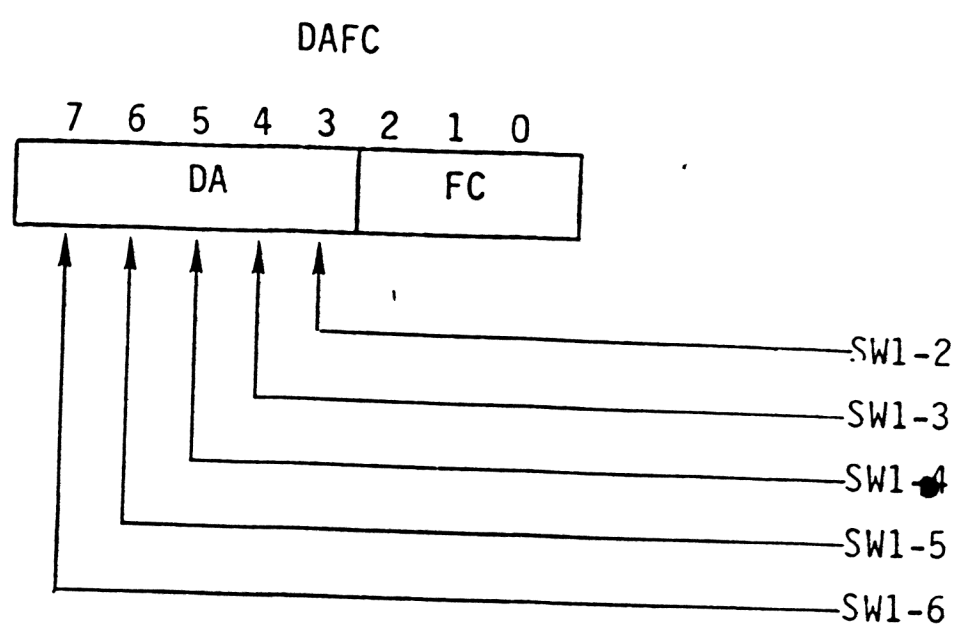


Figure 4-17. Device Address Function Code (SW1-2 through SW1-6)

CAUTION

SW1-1 is reserved and cannot be used (it must be in the OFF position). Since this bit corresponds to the third least significant bit in DAFC (AB02), AB02 must be OFF (0) in the DAFC field when using this board. Failure to do so would result in unpredictable operation of the system.

SECTION 5

SEMICONDUCTOR MODULES WITH ERROR CORRECTION AND 22-BIT ADDRESSING

5.0 INTRODUCTION

This section introduces Computer Automation, Inc., semiconductor RAM modules with error correction and 22-bit addressing: Models 53828 (256KB full card) and 53909 (1MB full card). Twenty-two bit addressing provides up to 8M bytes of addressable memory. Both full card modules must be driven by a Memory Management Unit (MMU, Models 53794 or 53861), and both require split backplane chassis (S17 chassis Model 53822 or S9 chassis Model 53940).

5.1 MODEL 53828 FULL-CARD SEMICONDUCTOR MEMORY WITH 22-BIT ADDRESSING

The 53828 semiconductor memory with error correction and 22-bit addressing is designed for use in a chassis with a Memory Management Unit (MMU). The memory is built on a standard full card and is available with 128K bytes (Model 53828-01) or 256K bytes (Model 53828-02) installed. Each memory board module is equipped with a four-word microcache, which significantly improves memory response times.

5.1.1 Specifications

This section presents specifications for Model 53828.

5.1.1.1 Memory Cycle Times

The maximum cycle times for read and write operations depend on whether error correction is required and whether the word is found in the microcache. Write operation cycle times also depend on whether the operation is performed in word or byte mode. In addition, all times assume that the operation does not overlap a refresh cycle. The cycle times are summarized in Table 5-1.

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Table 5-1. Memory Cycle Times, Model 53828

	FROM MEMORY	FROM MICROCACHE
Read		
Access (without correction)	370 ns	70 ns
(with correction)	510 ns	115 ns
Overhead (without correction)	280 ns*	280 ns*
(with correction)	280 ns*	280 ns*
Total (without correction)	630 ns	330 ns
(with correction)	770 ns	375 ns
* = limited by system factors external to memory		
Write (word)		
Access (without correction)	55 ns	--
Overhead (without correction)	380 ns	
Total (without correction)	435 ns	
Write (byte)		
Access (without correction)	435 ns	--
Overhead (without correction)	270 ns	
Total (without correction)	705 ns	

5.1.1.2 Environmental

Environmental specifications for Model 53828 are summarized in Table 5-2.

Table 5-2. Environmental Specifications, Model 53828

Operating Temperature (Degrees Celsius)	0 to 50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Humidity (Percent Noncondensing)	15 to 80

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NOTE

Free air flow around the unit is required to provide adequate cooling.

5.1.1.3 Physical

Physical specifications for Model 53828 are summarized in Table 5-3.

Table 5-3. Physical Specifications, Model 53828

Length	42.88 cm (16.88 in.)
Width	38.10 cm (15.00 in.)
Height	1.52 cm (0.6 in.)
Weight	1.1 kg (2.5 lb)

5.1.1.4 Electrical

Electrical specifications for Model 53828 are summarized in Table 5-4.

Table 5-4. Electrical Specifications, Model 53828

Voltage Regulation (All Voltages)	±5 percent
Power Consumption--53828-01 +5 V Maximum Operating +12 V Standby +12 V Maximum Operating -12 V Maximum Operating	 7.5 A 0.15 A (IDLE) 0.55 A (ACTIVE) 0.25 A
Power Consumption--53828-02 +5 V Maximum Operating +12 V Standby +12 V Maximum Operating -12 V Maximum Operating	 7.5 A 0.3 A (IDLE) 1.1 A (ACTIVE) 0.5 A

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5.1.2 Functional Description

The Model 53828 memory module consists of the following functional units:

1. Memory ICs and associated addressing circuitry
2. Error correction logic
3. Memory refresh circuitry
4. Microcache
5. MAXI-BUS Interface logic.

5.1.2.1 Memory ICs

The memory ICs are 16K x 1 RAMs, 21 RAMs per word, installed to a maximum capacity of 256K bytes. The 21-bit word length includes 16 data bits and 5 error checking bits. Addressing circuitry is provided to allow 256K byte addressability. The 16 data bits are available on the MAXI-BUS Interface. NAKED MINI 4/Series 5 processors can read or write the error correcting bits for test purposes only. The procedure is described in the NAKED MINI 4/ Series 5 Principles of Operation Manual.

5.1.2.2 Error Correcting Circuitry

The error correcting circuitry generates five error check bits from the 16 data bits. A word is stored as 21 bits where the five appended bits are error bits EØ through E4. The error correcting algorithm maximizes two-bit error detection and minimizes error bit generation and checking delays. The error correcting circuitry can be disabled for test purposes using a switch on the board.

The error check bits are generated when the data word is written into memory, and error checking is performed when the word is read. All single bit errors are detected and corrected. If a single-bit error is detected, corrected data is placed on the data bus. Correction of the data written in memory does not take place at this time, but during a refresh cycle. The circuitry cannot determine the bit locations of double or multiple bit errors. If a multiple bit error is detected, memory does not acknowledge the access.

Error checking is also carried out when a write operation is performed in byte mode. Before writing the byte, the error correcting circuitry checks the entire word already written in the addressed location for errors. If a single bit error is detected, a correction is made. The new byte is then substituted for the old, and the entire word written back into memory. If a multiple bit error is detected, processors and Direct Memory Access (DMA) devices react in the same manner as when a multiple bit error is detected during a word write operation. Because of the checking required, byte mode write operations require longer cycle times than word mode write operations. The cycle time for write operations in byte mode is identical whether or not an error is found.

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5.1.2.3 Memory Refresh and Error Correction

A refresh cycle is performed an average of once every 15 microseconds, and one word of memory is selected and checked for a bit errors. Detection of a single bit-error extends the refresh cycle to a read/modify/write cycle during which the word is corrected and written back into memory. Detected double bit errors are not corrected. An error checking/correcting operation is performed on each word of memory approximately once every 2 seconds on the 53828-02 (256K bytes) board, and once every second on the 53828-01 (128K bytes) board. A detected error pulses a light at the rear of board. A single-bit hard error in one word will therefore pulse the light once every error checking/correcting cycle.

5.1.2.4 Microcache

A four-word, parallel-loaded microcache is provided for each memory board. The microcache contains four words of data read from memory during a read operation in which the requested data word was determined to be within the memory module but not contained within the four word microcache. When updated, the microcache is loaded with the contents of four sequential memory locations, the two least significant bits of the address being ignored. For example, if memory access is requested at location :FC9C, and :FC9C is not one of the four words already loaded in the microcache, the microcache is loaded with the contents of memory location :FC9C, :FC9D, :FC9E, and :FC9F. The microcache provides increased access speeds for approximately 35 percent of all memory read cycles not cached by the memory management unit in the split chassis. Writing to a microcache location, byte writes to any on-board location, and any on-board refresh cycle, cause the microcache to be marked as invalid and require a read to update the microcache.

5.1.2.5 MAXI-BUS Interface

The MAXI-BUS Interface contains the memory addressing ciruitry, data bus drivers, and receiver. Because the 53828 memory board has 22 address lines, it should be installed only in a chassis that has an MMU (the S9 (Model 53940), S17 (Model 53822), and the dataCASE/5 S6 (Model 21719) chassis).

5.2 MODEL 53909

Computer Automation, Inc., produces the 53909 semiconductor RAM module with error correction and 22-bit addressing. Model 53909 requires an MMU and a spli back-plane motherboard, and is available in the following configurations:

1. 53909-01, 256K bytes installed
2. 53909-02, 512K bytes installed
3. 53909-03, 1M bytes installed.

All configurations are built on a standard full card.

5.2.1 Specifications

This section provides specifications for Model 53909, a RAM module with error correction and 22-bit addressing.

5.2.1.1 Memory Cycle Times

The maximum cycle times for read and write operations depend on whether or not error correction is required. Write operation cycle times also depend on whether the operation is performed in word or byte mode. In addition, all times assume that the operation does not overlap a refresh cycle. The cycle times are summarized in Table 5-5.

Table 5-5. Memory Cycle Times, Model 53909

Read	From Memory
Access (without correction)	370 ns
Access (with correction)	470 ns
Overhead (without correction)	260 ns*
Overhead (with correction)	260 ns*
Total (without correction)	630 ns
Total (with correction)	730 ns
* = limited by system factors external to memory	
Write (word)	
Access	80 ns
Overhead	345 ns
Total	425 ns
Write (byte)	
Access	385 ns
Overhead	380 ns
Total	765 ns

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5.2.1.2 Environmental

Environmental specifications for Model 53909 are summarized in Table 5-6.

Table 5-6. Environmental Specifications, Model 53909

Operating Temperature (Degrees Celsius)	0 to 50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Humidity (Percent Noncondensing)	15 to 80

NOTE

Free air flow around the unit is required to provide adequate cooling.

5.2.1.3 Physical

Physical specifications for Model 53909 are summarized in Table 5-7.

Table 5-7. Physical Specifications, Model 53909

Length	42.88 cm (16.88 in.)
Width	38.10 cm (15.00 in.)
Height	1.52 cm (0.6 in.)
Weight	1.1 kg (2.5 lb)

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5.2.1.4 Electrical

Electrical specifications for Model 53909 are summarized in Table 5-8.

Table 5-8. Electrical Specifications, Model 53909

Voltage Regulation (All Voltages)	±5 percent
Power Consumption--53909-01 +5V Maximum Operating	5.5 A
Power Consumption--53909-02 +5V Maximum Operating	5.85 A
Power Consumption--53909-03 +5V Maximum Operating	6.30 A

5.2.2 Functional Description

The Model 53909 memory module consists of the following functional units:

1. Memory ICs and associated addressing circuitry
2. Error correction logic
3. Memory refresh circuitry
4. MAXI-BUS Interface logic.

5.2.2.1 Memory ICs

The memory ICs are 64K x 1 RAMs, 21 RAMs per word, installed to a maximum capacity of 1M bytes. The 21-bit word length includes 16 data bits and 5 error checking bits. Addressing circuitry is provided to allow 1 MB addressability. The 16 data bits are available on the MAXI-BUS Interface. NAKED MINI 4/Series 5 processors can read or write the error correcting bits for test purposes only. The procedure is described in the NAKED MINI 4/ Series 5 Principles of Operation Manual.

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5.2.2.2 Error Correcting Circuitry

The error correcting circuitry generates five error check bits from the 16 data bits. A word is stored as 21 bits where the five appended bits are error bits EØ through E4. The error correcting algorithm maximizes two-bit error detection and minimizes error bit generation and checking delays. The error correcting circuitry can be disabled for test purposes using a switch on the board.

The error check bits are generated when the data word is written into memory, and error checking is performed when the word is read. All single bit errors are detected and corrected. If a single bit error is detected, corrected data is placed on the data bus. Correction of the data written in memory does not take place at this time, but during a refresh cycle. The circuitry cannot determine the bit locations of double or multiple bit errors. If a multiple bit error is detected memory does not acknowledge the access.

Error checking is also carried out when a write operation is performed in byte mode. Before writing the byte, the error correcting circuitry checks the entire word already written in the addressed location for errors. If a single bit error is detected, a correction is made. The new byte is then substituted for the old, and the entire word written back into memory. If a multiple bit error is detected, processors and Direct Memory Access (DMA) devices react in the same manner as when a multiple bit error is detected during a word write operation. Because of the checking required, byte mode write operations require longer cycle times than word mode write operations. The cycle time for write operations in byte mode is identical whether or not an error is found.

5.2.2.3 Memory Refresh and Error Correction

A refresh cycle is performed an average of once every 15 microseconds. In addition, one word of memory is selected and checked for a bit errors. Detection of a single bit error extends the refresh cycle to a read/modify/write cycle, during which the word is corrected and written back into memory. Detected double bit errors are not corrected. An error checking/correcting operation is performed on each word at the following approximate intervals:

1. Model 53909-01--every 2 seconds
2. Model 53909-02--every 4 seconds
3. Model 53909-03--every 8 seconds.

A detected error pulses a light at the rear of board. A single bit hard error in one word will therefore pulse the light once every error checking/correcting cycle.

5.2.2.4 MAXI-BUS Interface

The MAXI-BUS Interface contains the memory addressing ciruitry, data bus drivers, and receiver. Because the 53909 memory board has 22 address lines, it should be installed only in a chassis that has an MMU (the S9 (Model 53940) and S17 (Model 53822) chassis).

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SECTION 6

BATTERY BACKUP

6.0 INTRODUCTION

Semiconductor memories are volatile by nature and may lose stored data if primary power is interrupted. To guard against such losses, Computer Automation, Inc., provides a battery backup option. Battery backup supplies a continuation of power to its associated memory module(s) during interruptions, providing data retention for a minimum of 2 minutes.

Battery Backup is provided on board. The battery is mounted on the memory module.

NOTE

Model 53828 is not available with a battery backup option.
Battery backup for model 53909 is discussed in Section 7.

The Computer Automation, Inc., battery backup increases data integrity of semiconductor memories with the use of a wide range of batteries and charge rates.

6.1 SEMICONDUCTOR MEMORIES WITH ON-CARD BATTERY BACKUP

Semiconductor memories are available in both static and dynamic MOS; each type requires different battery backup considerations. Static memories normally require a single voltage source for memory retention, whereas dynamic memories are more complex and require up to three different voltages (generally, ±5 Vdc and +12 Vdc) to operate their timing, logic, and refresh circuitry. Computer Automation, Inc., provides a DC-to-DC converter and regulator as a part of the basic backup which is effectively used to simplify the number and types of batteries required. Using this technique, a single common 6 volt battery can be used to supply the multiple voltage and current requirements. Table 6-1 summarizes the configurations available with battery backup.

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Table 6-1. Memories With On-Card Battery Backup

MEMORY TYPE	MODEL NUMBER
RAM, 700 nsec full card	11611-xx (with parity)
RAM, 580 nsec half card	53775-xx
RAM, 550 nsec full card	11711-xx (with parity)
RAM/ROM/EPROM, half card	53678-xx (except 53678-00)
RAM with error correction	53819-xx

Typical backup power required for an 16KB by 16-bit dynamic memory module is approximately five watts, while an equivalent static memory module requires four times as much power.

6.2 BATTERIES

The most common types of commercially available batteries are alkaline, manganese, mercuric oxide, zinc air, silver zinc, lead-acid, and nickel-cadmium. Lead-acid and nickel-cadmium are most commonly used in uninterruptible power systems.

Standard commercial lead-acid batteries are rechargable and are currently available in sealed and unsealed configurations, with expected battery life-times of 3 to 5 years. Batteries can be obtained from many battery manufacturers, including Gates, Gould, Globe, Eagle, and Prichard. The most popular of these batteries is the sealed gelled electrolyte type, which does not require routine maintenance of adding liquid or checking liquid levels. These batteries are very small and compact and usually can be mounted in tilted or inverted positions.

WARNING

> Although most lead-acid batteries are temperature tolerant and generally exceed the environmental requirements of the computer system, adequate ventilation must be considered for unsealed batteries during fast charging utilization, since hydrogen and oxygen gases sometimes are released and could cause an explosion if a spark is introduced.

Nickel-cadmium batteries also are useful where longer life is required. These batteries generally are smaller in size, have a battery life of 9 to 12 years, are maintenance free, emit no gas during operation, and can be operated in any position without affecting performance. Computer Automation, Inc., battery backup products use nickel-cadmium batteries rated at a temperature of 50°C rather than the more common 40°C rating.

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Six volts is a popular, economical, readily obtained battery voltage, and is used in most semiconductor battery backup applications. Full environmental and application data for batteries can be obtained from most battery manufacturers.

Since batteries should be recharged after use, a small commercial charger is also recommended.

6.2.1 Charging Methods

Several charge methods are capable of effectively charging lead-acid or nickel-cadmium batteries. These methods all accomplish the same end: putting enough energy into the battery to provide the required amount of discharge energy. The various methods differ in the time it takes to accomplish the task, the complexity of circuitry used, and the techniques used to provide the charging function in a safe and reliable manner.

This section discusses methods for charging nickel-cadmium and lead-acid batteries.

6.2.1.1 Charging Nickel-Cadmium Batteries

The maximum charge current that can be used in the constant-current charge method is determined by the cell overcharge capability. This charge current level is typically some fraction of the nominal capacity of the cell. Standard nickel-cadminum sealed cells can tolerate 0.1 C (C is defined as the battery amp x hour rating) overcharge for extended periods of time without damage or serious performance deterioration. Special batteries with higher overcharge current capability are also available, but the 0.1 C overcharge capability is standard, most economical, and most often used.

Charging at the 0.1 C rate (a slow charge rate often referred to as "overnight charging") requires approximately 10 to 14 hours to restore a full charge in nickel-cadmium batteries. Although slow, the 0.1 C charge rate has the following advantages:

1. It permits the use of smaller, generally more economical, chargers than those for higher charge rates.

2. It permits the use of the least expensive batteries.

3. It minimizes cell temperature rise and internal pressure during charging.

The charging rate is usually 0.1 C whenever 10 hours of recharging time are available for full recharge of the battery. Chargers designed for slow rate charging are the simplest and least expensive of all nickel-cadmium battery chargers. See Table 6-2 for battery charging methods and rates.

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Table 6-2. Nickel-Cadmium Rates for Charging and Discharging

	CHARGE RATE	
CHARGING METHODS	CURRENT RATE (C = amp x hour)	RATES
Trickle	0.01 C	100 hours
	0.02 C	50 hours
	0.03 C	33 hours
Slow	0.04 C	25 hours
	0.05 C	20 hours
	0.06C	17 hours
	0.07 C	14 hours
	0.10 C	10 hours
Quick	0.20 C	5 hours
	0.50 C	2 hours
Fast	1 C	1 hours
	2 C	30 minutes
	3 C	20 minutes

The Computer Automation, Inc., on-card battery backup options use a slow 0.1 C constant current diode and resistor charger circuit (Figure 6-1). To determine the proper charge rate, divide by 10 the current drain rate that will discharge the battery in one hour. This type of slow charger normally can be left connected for long periods of time without damaging the battery.

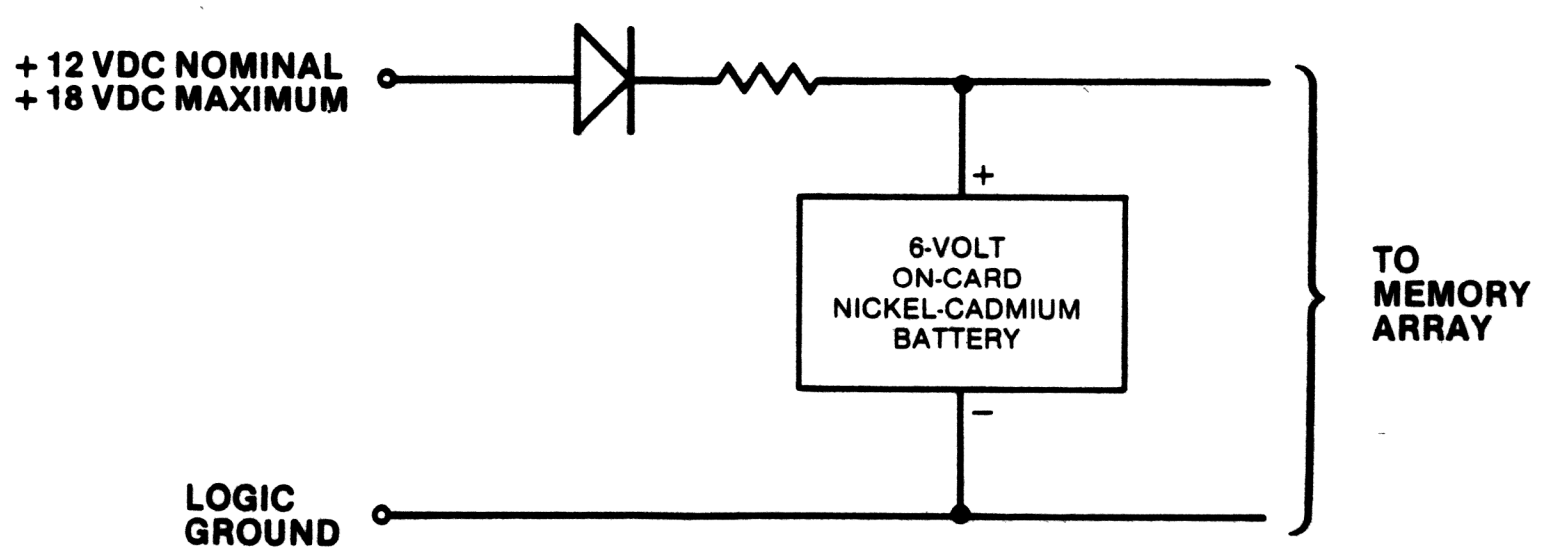


Figure 6-1. Simple Constant Current Source

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Many user applications require three or more partial or full discharges per day. Such applications, obviously, cannot accept a recharge time of 10 hours. Recharge time can be decreased by using batteries with three or more times the capacity (amp x hour) required for the particular memory. However, the added battery size and cost may be unsuitable for all applications, and a quick or fast charge can be a better solution. A quick charge usually is defined as charging a battery in 2 to 5 hours at a charge rate of 0.2 C to 0.5 C. This charge rate is ideal for applications requiring many partial or complete discharges per day. A fast charge can be defined as charging a battery at a rate of 0.5 C or greater. When using fast charging techniques, it is necessary to end the high charge rate before the battery goes into excessive overcharge.

Quick or fast charging circuits are possible with a split-rate approach. Split-rate charging is a technique where the battery is charged initially at a fast rate. Then, at the appropriate time--generally when the battery goes into overcharge--the charging is switched to a low or trickle rate.

The term "trickle rate" identifies a standby rate, approximately 0.01 C to 0.03 C, which is just high enough to keep a charged battery fully charged, and low enough that the battery can withstand being charged at this rate indefinitely. However, the trickle rate is too low to efficiently charge a discharged battery.

6.2.1.2 Charging Lead-Acid Batteries

Lead-acid batteries can be charged with constant voltage, constant current, and taper current. Of these, the constant voltage technique generally is the most efficient and fastest method of charging lead-acid batteries. Therefore, the following paragraphs discuss this approach.

The magnitude of the constant voltage applied to the battery during charging and the current capabilities of the charging source, dictate how long it will take to charge the battery. A lead-acid battery can be recharged in approximately 2 hours, although about 80 to 90 percent of the battery capacity expended during a discharge can be returned to the battery in about 30 to 45 minutes. The charger power source furnishes a 6 C charge rate at a constant voltage of approximately 7.5 volts. Chargers rated at 1 C to 10 C could take as long as 4 to 10 hours to recharge a battery. Consult the charger and battery manufacturer's specifications to determine the proper charger and recharge time requirements.

In using the constant voltage recharging technique, the battery normally accepts charge current at its own rate; the current is necessary to maintain full battery capacity. Proper battery chargers can be left on, connected to the battery, while the system is running. A simple constant voltage charging source is shown in Figure 6-2. Battery manufacturers can supply customers with application notes for all types of chargers, complete with schematics and parts lists. Commercially available automotive battery chargers should not be used, since they usually do not include a voltage regulator and can cause severe memory damage or reduced battery life. Other satisfactory and inexpensive commercial float chargers are available from manufacturers such as Mauratron, Gates, Globe, and Cellmate.

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6.2.1.3 Undervoltage Protection

Most rechargable batteries require some type of undervoltage protection to prevent irreversible battery damage during excessive or deep discharges. Computer Automation, Inc., provides this needed protection on all Battery Backup options for external and internal batteries. This undervoltage protection is normally set at about 4.6 volts.

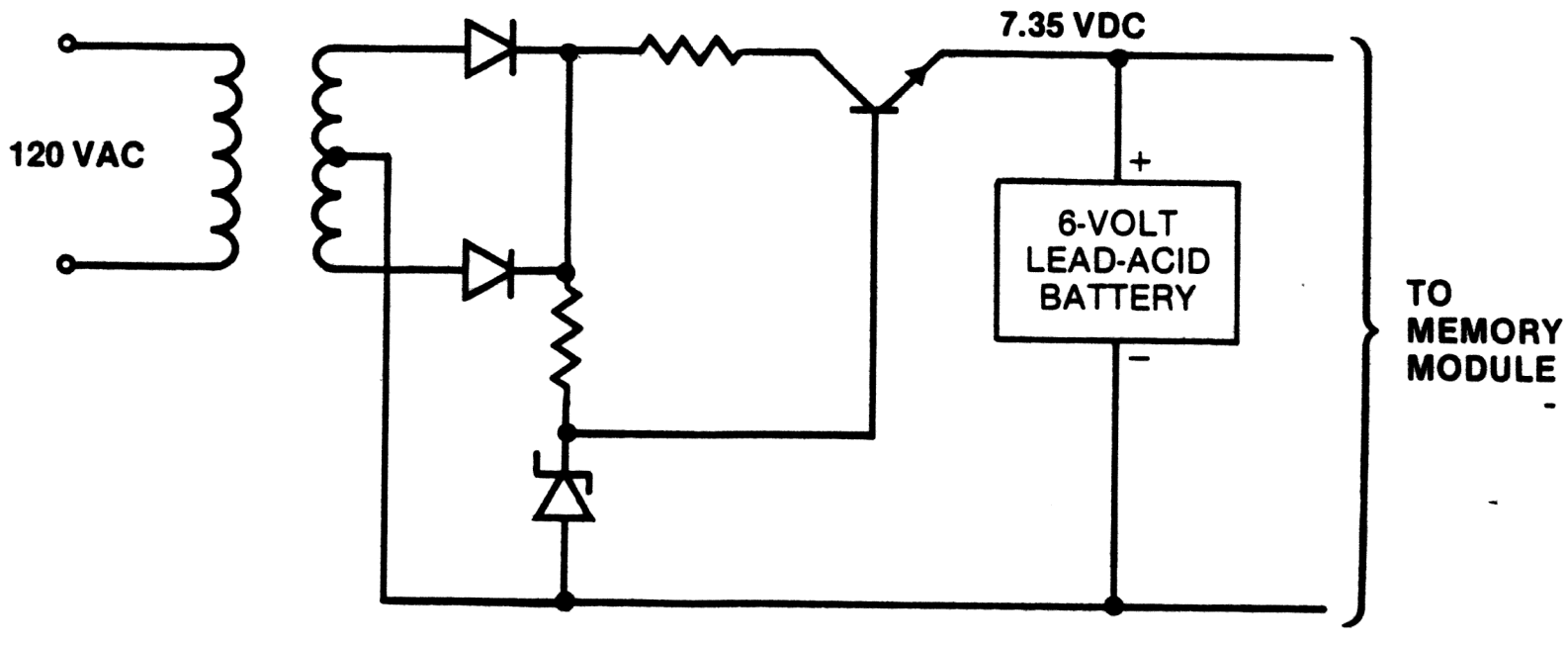


Figure 6-2. Simple Constant Voltage Source

6.2.2 Battery Requirements

A lead-acid automotive battery rated at 300 ampere-hours would provide a typical 16KB by 16-bit MOS dynamic memory module with emergency power for 9 weeks. Emergency power would undoubtedly be sufficient to carry through short power interruptions as well as power brown-outs and black-outs.

A more reasonable battery supplying 6 ampere-hours is typically smaller than 2 x 3 x 3 inches and provides 7 hours of emergency service. Generally, this is sufficient for most applications.

It is important to implement the appropriate Computer Automation, Inc., memory backup options, even when an external battery and charger must be added to extend the basic memory retention time. Power saving features, voltage sensing, power failure detection, and automatic switching are difficult, if not impossible, to mechanize externally from memory modules and computer equipment.

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6.3 ON-CARD BATTERY BACKUP

During a primary power outage, on-card battery backup provides a minimum of 2 to 9 minutes of data retention for the memory card on which it is mounted. Further, boards with on-card battery backup can be supported for even longer power outage intervals with a user-supplied external battery. On-card battery backup uses a 100 milliamp-hour nickel-cadmium battery. An on-card switch to external expansion are included.

To connect the on-board battery, set switch SW3 in the INT position. This switch is located on the P4 plug at the rear end of the memory board.

On-card battery backup includes these features:

1. Automatic power sensing and switching and invalid data detection

2. Undervoltage protection and internal constant-current charger for internal/ external battery

CAUTION

When removing a combination memory board with on-card battery backup from a chassis, set the internal/external battery backup selection switch in the EXT position to avoid severe machine damage. This switch (SW3) is located at the rear of the memory board. Any external battery must be also disconnected. During such disconnection, SW3 must be on INT.

Table 6-3 shows the memory retention characteristics for each memory module with on-card battery backup.

Table 6-3. Memory Retention with On-card Battery Backup

MEMORY MODULE	MINIMUM TIME (Minutes)	TYPICAL TIME (Minutes)
11611-16	3.0	5.0
11611-32	2.0	3.0
11711-16	3.0	3.25
11711-32	2.0	2.5
53678-39	9.0	19.0
53678-59	2.0	4.0
53678-69	1.5	3.0
53775-16	2.0	
53775-32	2.0	
53775-64	2.0	
53819-16	2.0	6.0
53819-32	2.0	6.0
53819-64	2.0	6.0

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External battery backup is described in detail in this section. Figure 6-3 shows a functional block diagram of how external battery backup can be added to a memory module with on-card battery backup. The external battery charger is not required if an internal charger is used.

The external battery cable should be less than 10 feet long, and should be constructed of two AWG 22 to 26 (metric gauge 5 to 8) stranded wires (four wires if internal charger is used). The connector should be Herman Smith #1234 or Keystone Electronics #72.

6.4 EXTERNAL EXPANSION

On-card battery backup can be expanded to provide additional memory retention by attaching a separate external battery and cable. An internal charger is incorporated into the basic backup for an external nickel-cadmium battery. This feature eliminates the external charger requirements for most expansion applications. An external charger can be connected where battery recharge ability is required and the internal charger is not adequate.

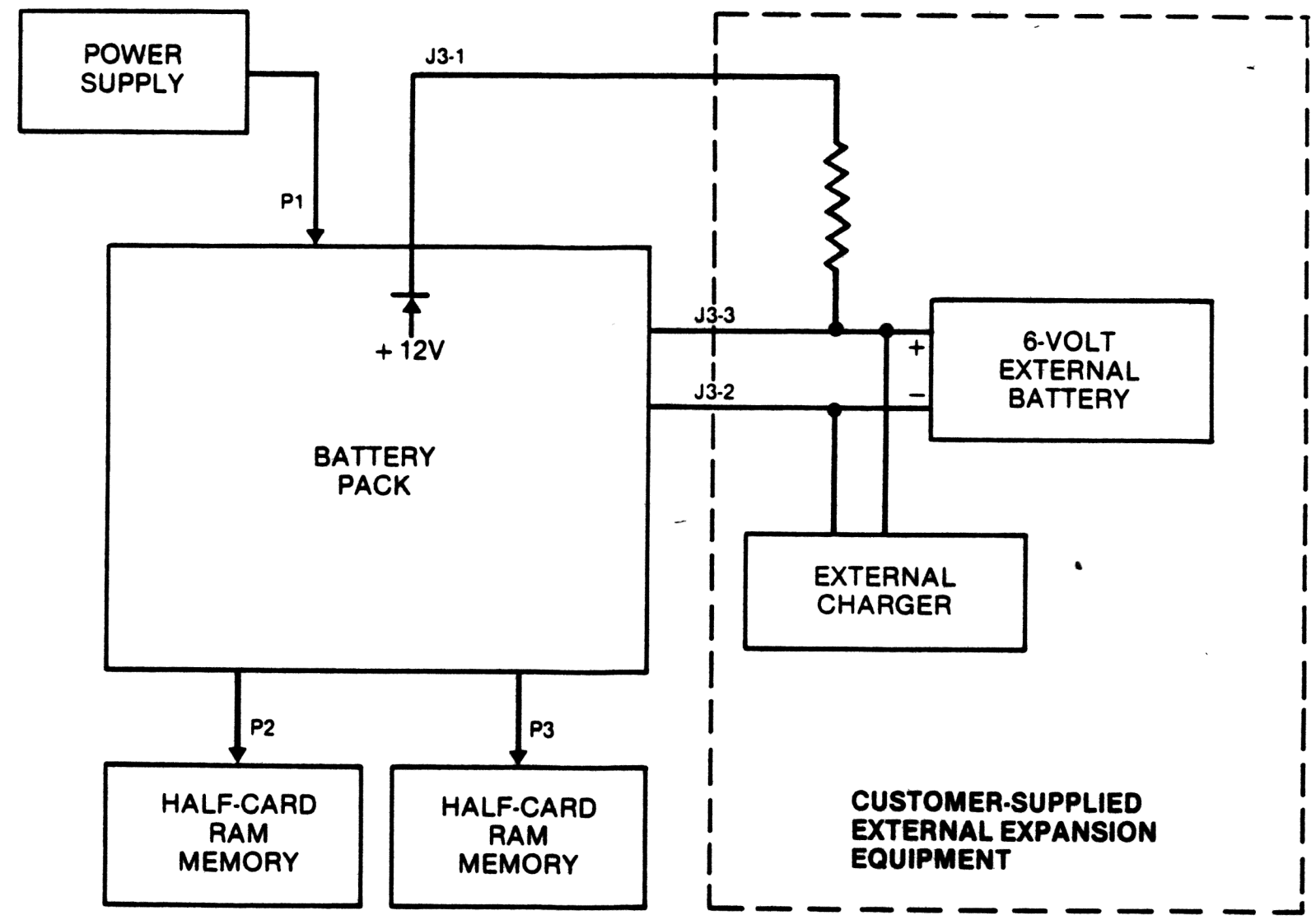


Figure 6-3. On-card Battery Backup Block Diagram

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6.4.1 External Expansion Specifications

Nickel-cadmium or lead-acid batteries can be used for external backup. If an internal charger is used, a nickel-cadmium battery must be used. Batteries can range from 5.4 to 7.5 volts; external batteries exceeding 7.5 volts can cause severe damage to the battery backup circuitry.

Table 6-4 shows the external battery power consumption requirements.

When external battery backup is used, battery undervoltage protection is not required. This protection is provided in the on-card battery backup.

Table 6-4. External Battery Current Consumption

MEMORY MODEL	BATTERY CURRENT CONSUMPTION AMPS x HOUR
11611-16	0.8
11611-32	1.5
11711-16	0.8
11711-32	1.5
53678-39	0.25
53678-59	1.0
53678-69	2.0
53775-16	0.9
53775-32	1.4
53775-64	2.32
53819-16,32,64	2.0

6.4.2 Chargers for External Batteries

This section discusses internal and external chargers for external battery backup.

6.4.2.1 Internal Charger

The internal constant current charger can be used for external nickel-cadmium batteries. The charger operates off the computer's ±12 volt power supply and is therefore limited to 0.25 amps. This charger can be used by connecting a customer-supplied external resistor (R) to the terminals provided (Figure 6-3). This resistor must be selected to regulate the current going to the battery to within five percent of the value C (C = battery current consumption in amp x hour. See Table 6-4). The only exception to this rule is that the 12 volt power supply may not be overloaded. If the total draw on the 12 volt power supply will exceed its rating, then a larger power supply, an external charger, or a lower charging rate should be considered. In any case, the resistor is in series with a 1N4002 diode, which has a 1.1 forward voltage at one amp current.

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Table 6-5 shows typical battery amp x hour ratings, and expected memory data retention in hours. This table provides the user with a quick, simple method of extending the basic two minutes of data retention to 10 hours. This is accomplished by using a three- or four-wire cable, six-volt nickel-cadmium battery, and a power resistor. The external resistor requirements are shown in Table 6-6. Care should be exercised when connecting the resistor so as to protect the -12 volt supply from shorting. Operating notes and cautions are given in this section.

Table 6-5. Memory Retention with External Nickel-Cadmium Battery

	MEMORY RETENTION (Hours per battery rating)			
MODEL	1 amp x hour	2 amp x hour	2.5 amp x hour	4 amp x hour
11611-16	1.25	2.5	3.0	5.0
11611-32	0.7	1.3	1.7	2.7
11711-16	1.25	2.5	3.0	5.0
11711-32	0.7	1.3	1.7	2.7
53678-39	4.0	8.0	10.0	16.0
53678-59	1.0	2.0	2.5	4.0
53678-69	0.5	1.0	1.25	2.0
53775-16	1.1	2.2	2.8	4.4
53775-32	0.7	1.4	1.8	2.8
53775-64	0.4	0.8	1.1	1.6
53819-16,32,64	0.5	1.0	1.25	2.0

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Table 6-6. Resistor for External Nickel-Cadminum Battery

BATTERY RATING (amp-hour)	EXTERNAL RESISTOR	
	VALUE ± 5%	WATTAGE
1	60 ohms	1
2	30 ohms	2
2.5	24 ohms	4
4	15 ohms	5

6.4.2.2 External Chargers

Nickel-cadmium and lead-acid batteries require different external chargers. For nickel-cadmium batteries use a constant-current external charger, and for lead-acid batteries use a constant voltage external charge. Suggested vendors include Mauratron Inc., Globe, Gates, and Cellmate.

6.4.3 Other Configurations

A single external battery can be configured to operate in parallel with the battery pack option. However, the internal charger is limited to a total current draw of 0.25 amps from the Model 12046-03 power supply and 0.45 amps from the Model 20928-00 power supply. These limitations are necessary to ensure that the power supply is left with sufficient ±12 volt power to drive the computer system.

6.5 OPERATING NOTES AND CAUTIONS

Note the following operating points:

1. The INTERNAL/EXTERNAL battery switch should be set to EXTERNAL during storage or shipment to prevent internal battery discharge. Do not operate the INTERNAL/EXTERNAL switch while the system is running on battery, or data can be lost.

2. An external customer-supplied battery can be disconnected while the system is running if the INTERNAL/EXTERNAL battery switch has been set previously to the INTERNAL position. If an INTERNAL/EXTERNAL switch is not present on the backup option, the external battery can not be disconnected.

3. Internal battery recovery is approximately 10 hours after all power outage capability has been exhausted.

4. Fully discharged external batteries should not be attached to a NAKED MINI 4 system power supply when using an internal charger unless the external resistor sufficiently limits power supply for the +12 volt current to the appropriate value defined in Topic 6.4.2.1.

5. An on-card nickel-cadmium battery normally discharges in storage. After 90 days of storage, the battery is fully discharged and should be recharged.

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SECTION 7

MODEL 53909 BATTERY BACKUP

7.0 INTRODUCTION

This section presents information on the Computer Automation, Inc. Battery Backup system (BBU), which guards against data loss during power failure.

7.1 GENERAL INFORMATION

The following paragraphs give general information on the BBU system, which is intended for use with Model 53909 memory (RAM module with error correction and 22-bit addressing).

7.1.1 System Elements

Each BBU system includes an ac Uninterruptible Power Supply (UPS) and a dc Switching Power Supply (SPS), shown in Figure 7-1. The UPS includes two self-contained maintenance-free batteries, a battery charger, and a static inverter which coverts dc battery power to ac power. Figure 7-2 is a block diagram of the BBU system elements.

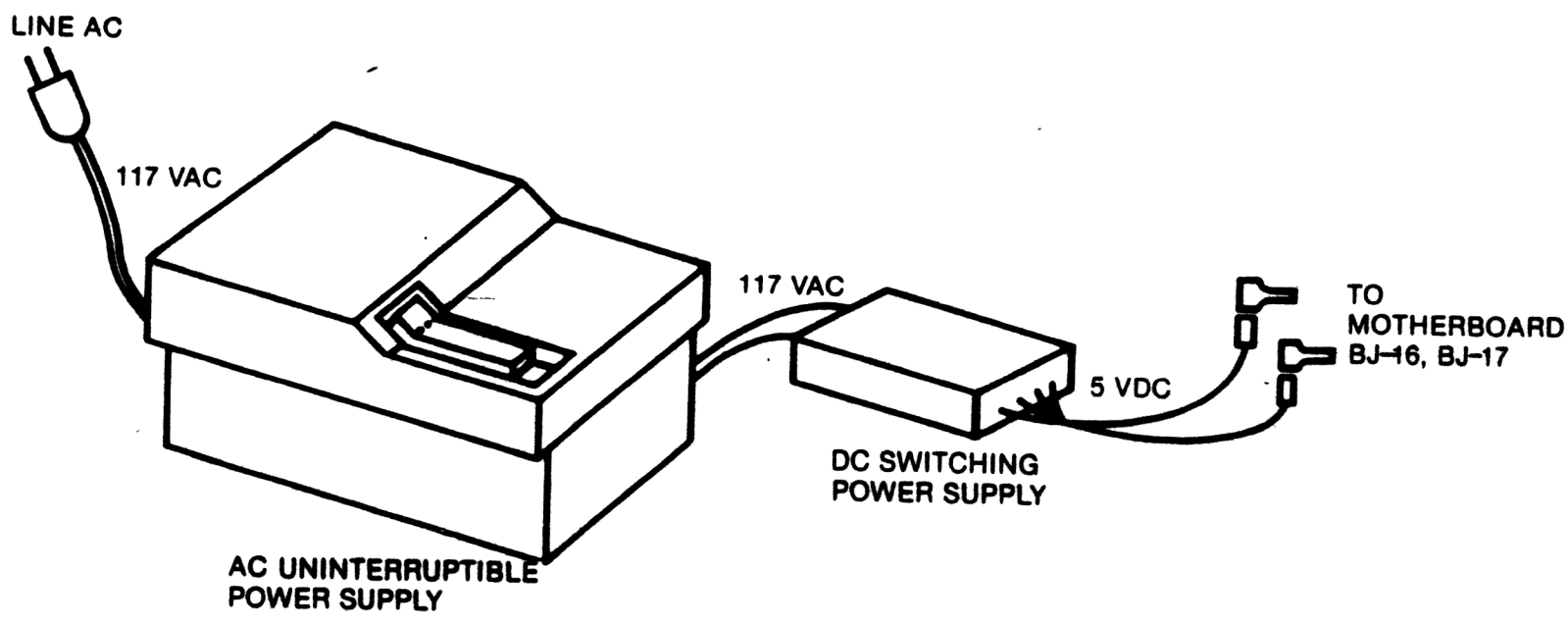


Figure 7-1. BBU System

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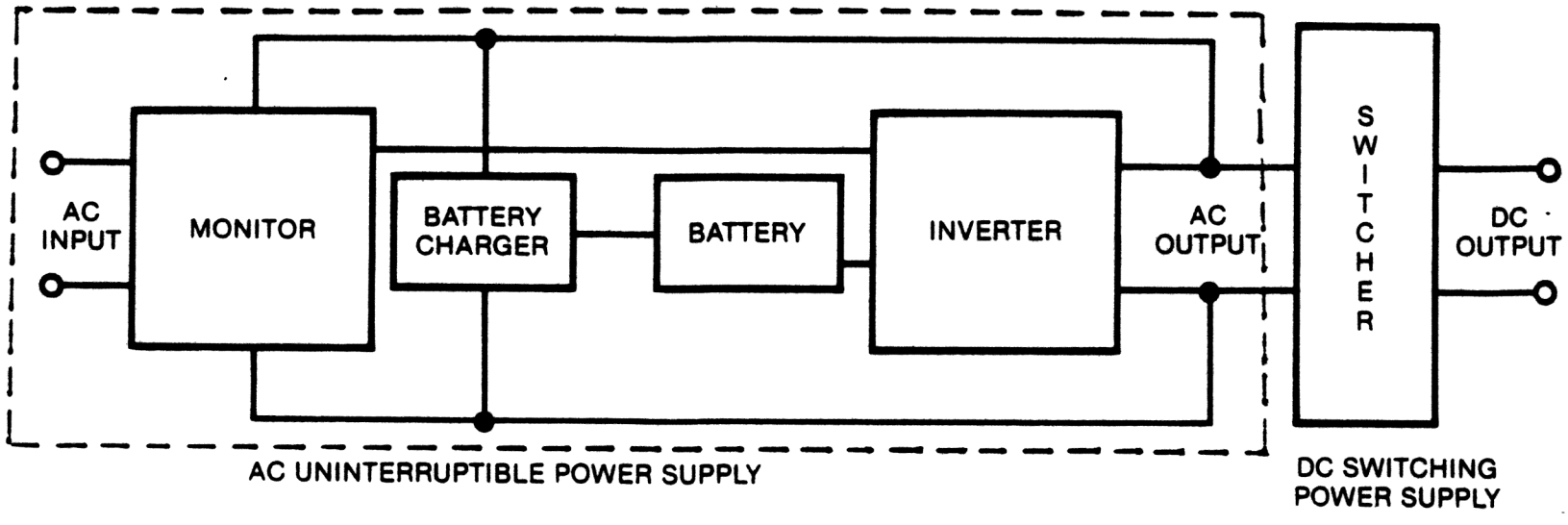


Figure 7-2. BBU Block Diagram

7.1.2 Normal Operation

When utility power is available, it powers the load directly and maintains the charge of the BBU batteries.

7.1.3 Operation at Power Loss

When utility power fails or drops more than 15 percent below nominal, the BBU disconnects its ac input line from its ac output. The monitor circuit senses the voltage drop and activates the inverter. The inverter delivers power from the batteries, which is stepped down and filtered by an Electromagnetic Interference (EMI) filter.

The EMI filter attenuates noise from the power line and the UPS before it is applied to the ac output.

The ac output drives the dc SPS. It is the SPS which maintains the integrity of the memory array.

7.1.4 Termination of Battery Backup

At worst case (8 MB configuration), memory can be maintained for approximately 20 minutes. Less memory can be maintained for a longer period of time. When utility power returns to 90 percent of nominal, BBU reconnects its ac input line to its output, providing a direct path to the load. If battery voltage drops below 19 V ±0.5 V, the BBU will shut down until ac power is restored.

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7.2 INSTALLATION AND OPERATION

This subsection presents information on BBU installation and operation.

7.2.1 Installation

To install the BBU, open the NM4/Series 5 front cabinet door and remove the console to expose the motherboard. Connect the white BBU cables to pins BJ16 (+5 BU) on the motherboard. Connect the black BBU cables to pins BJ17 (+5 BUR) on the motherboard. If any wires get disconnected, consult the wire list in Table 7-1.

Table 7-1. BBU Cable Wire List

WIRE FUNCTION	ORIGIN (SPS)	DESTINATION (MOTHERBOARD)
+5 BU (black)	OUT+	BJ16
+5 BUS (black)	S+	BJ16
+5 BUSR (white)	S-	BJ17
+5 BUR (white)	RTN	BJ17

Model 53909 (RAM module with error correction and 22-bit addressing) is designed for battery backup from an external +5 volt power supply. The external power is brought through the motherboard on pins 109, 110, 209, and 210.

If the memory is configured for battery backup (that is, if both jumpers or both clips are in the BBU position on the memory board), connect the +5 VINT (internal +5 V power) on memory to pins 109, 110, 209, 210 of the motherboard.

If the memory is not configured for battery backup (that is, if both jumpers or both clips are in the NBU position on the memory board), connect the 53909 +5 VINT on memory to pins 113, 114, 213, 214 (system +5 VB) on the motherboard.

The external power supply must be capable of supplying +5 volts ±5% at 100 watts (20 amps), and have a holdup time of 20 milliseconds or more. Battery backup is not insured if supply voltage drops below 4.75 volts.

CAUTION

There are two jumpers or two clips for backup (BU) or nonbackup (NBU) configurations. Both jumpers or both clips must be in the same position (both BU or both NBU). Otherwise, external and system power supplies may short to each other, causing damage to the memory as well the power supplies.

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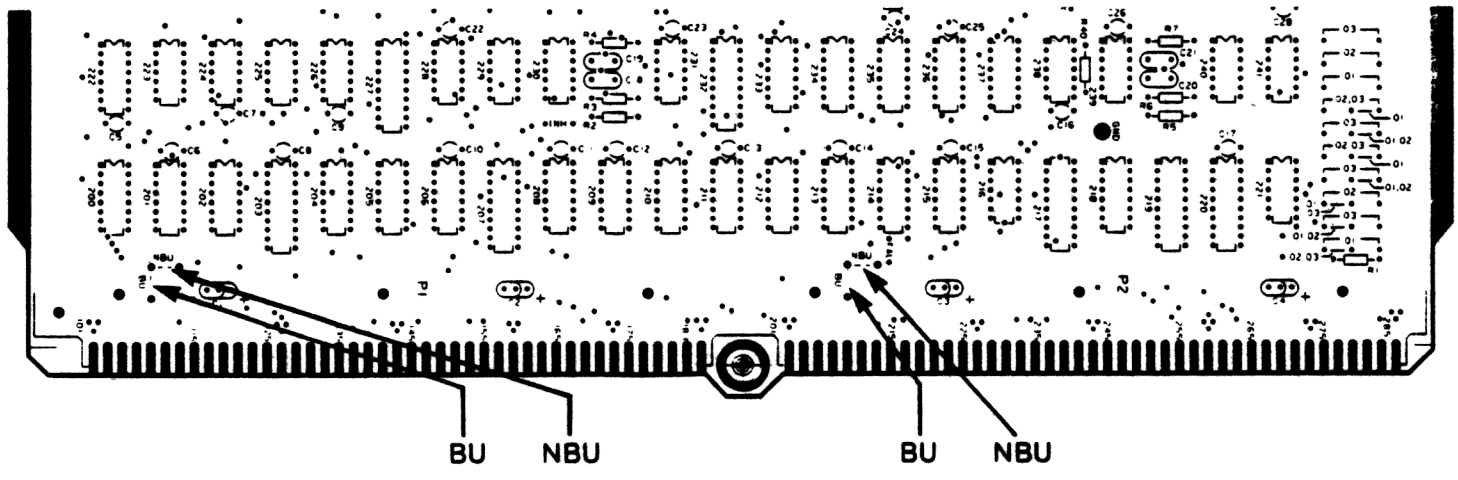


Figure 7-3. BU and NBU Configurations, Model 53909

7.2.2 Operation

Power-up and power-down procedures MUST be performed in the following order:

1. Power-up:
   a. Press UPS on/off switch on.
   b. Turn on main system power.
2. Power-down:
   a. Turn off system main power.
   b. Press UPS on/off switch off.

The BBU will click when the main system returns to utility power. As long as a power fail routine is included in the software, the main system program resumes in a running mode. The program restarts at its location just prior to the power interrupt.

7.3 SPECIFICATIONS

The following paragraphs give specifications for the BBU.

7.3.1 Physical Specifications

The BBU system, including the ac UPS and the dc SPS, is designed to fit into the NAKED MINI 4/Series 5 cabinet. The maintenance free, lead-acid batteries supply 24 volts to the system. Table 7-2 summarizes the physical specifications of the BBU system.

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Table 7-2. BBU Physical Specifications

	UPS	SPS
Length	13.5 in. (34.3 cm)	7.5 in. (19.1 cm) 10 in. (25.4 cm)
Width	10.2 in. (25.9 cm)	4.8 in. (12.1 cm) 5.25 in. (13.3 cm)
Height	8.1 in. (20.6 cm)	2 in. (5.1 cm) 2.3 in. (5.8 cm)
Weight	38.6 lb (17.5 kg.)	approx. 3 lb (1.36 kg.)
Cooling	Nonrestricted air-flow available: Convection cooling is adequate. Confined space: Conduction cooling (moving air) recommended.	

7.3.2 Input Specifications

Two voltage ranges are available on the ac UPS: Model 01 operates on 120 volts; Model 02 operates on 230 volts. The voltage range is selectable at the input barrier strip, and no jumpers are required. The dc SPS is suitable for use with either model. Table 7-3 summarizes the input specifications of the BBU system.

Table 7-3. BBU Input Specifications

	UPS MODEL 01	UPS MODEL 02	UPS BATTERY CHARGER
Standard dual Range (in conjunction with UPS)	90-130 Vac 47-63 Hz single phase	180-260 Vac 47-63 Hz single phase	--
AC input power (in conjunction with SPS)	108-132 V, 60 Hz single phase	198-242 V, 50 Hz single phase	75 W (max), batteries depleted 15 W (max), batteries charged, charger off

7.3.3 Output Specifications

The ac UPS uses an inverter to convert battery power to ac power. The inverter is designed to deliver high peak power while operating at a high frequency over a wide load range. The EMI filter steps down the signal and delivers a low-distortion signal to the dc SPS. The dc SPS output then maintains power to the memory. The BBU system output specifications are summarized in Table 7-4.

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Table 7-4. BBU Output Specifications

	UPS	BATTERY	SPS	BBU SYSTEM
Maximum continuous power	200 volt-amps	8 amp-hours	+5 V ±5%, 20 amps, 100 W (max)	--
Peak power	400 volt-amps	--	--	--
Recharge time	--	8 hours (min.)	--	--
* Backup time	--	--	--	20 min.(min) full load (8 MB)
Output noise Ripple	50 MV P-P (max) 19% P-P	--	--	--
Waveform	sinusoidal, 5% distortion		--	--
Temperature rating	--	--	0° to 50° C at full output current	--
* Backup time (typ.) = 1.20 x backup time (min.)				

7.3.4 Automatic Controls

The BBU system is designed to automatically transfer from utility to backup power and back again and to shut down before the batteries become too depleted to be recharged at the appropriate voltages. BBU automatic controls are summarized in Table 7-5.

Table 7-5. BBU Automatic Controls

	UPS MODEL 01	UPS MODEL 02	BBU INVERTER
Utility-to-BBU transfer	102 VRMS	187 VRMS	--
BBU-to-utility transfer	108 ±1 VRMS	198 ±1 VRMS	--
Transfer interval	3-9 VRMS	4-11 VRMS	--
Time without power during transfer	10.0 ms		--
Shutdown	--	--	19 ±0.5 V
Restart	--	--	When ac power is restored

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7.3.5 Protection Devices and Circuits

The BBU system features several devices and circuits to protect the elements of the system. These protective features are summarized in Table 7-6.

Table 7-6. BBU Protection Devices and Circuits

BBU ELEMENT	PROTECTION
AC input	Fuse
Battery	1. Fuse and fusible resistors 2. Automatic under-voltage shutdown guards against depletion
Inverter output	Current-limiting circuit protects inverter from overload and short-circuit
Burnout protection	Regulation maintained down to 90-108 Vac, full load, with no compromise in performance
Load lead loss	Remote sensing capabilities provided to compensate for load lead losses of 0.5 V max. Open lead protection provided.
DC output	Inherently protected from damage due to reverse polarity voltage across output terminals

7.3.6 Certification

The BBU system ac uninterruptible power supply (Model 01 only) and the dc switching power supply conform to Underwriters Laboratory, Inc., Specification 1012 (Power Supplies). The EMI filter meets Underwriters Laboratory, Inc., standards for conducted EMI noise when tested in conjunction with the ac UPS and the dc SPS.

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PH: (51) 754734/752264/752064
TLX: 214848

JAPAN

Showa Information
Systems Co., Ltd.
Nihon Seimei Bldg.
1-19 Akasaka 8-Chome
Minato-ku, Tokyo 107
Japan
PH: 403-7101
TLX: 2422827

LATIN AMERICA

U.S. Contact
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LUXEMBOURG

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9322 Gijzegem
Belgium
PH: 53/21-4628
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Netherlands
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NEW ZEALAND

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33-35 Rawene Road
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Auckland 10, New Zealand
PH: 488-117
TLX: 2612

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Metric A.S.
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SINGAPORE

Teledata (Singapore) Pte. Ltd.
1593, Block 5071
Ang Mo Kio Industrial Park 2
Singapore 2056
Republic of Singapore
PH: 4568491
TLX: RS 26383

SWEDEN

Scandia Metric AB
Banvaktsvagen 20
Fack S-171, 19 Solna 1
Stockholm, Sweden
PH: 8-820400
TLX: 10766

SWITZERLAND

Datacare AG
Untere Bahnhofstr. 19
9500 Wil/Switzerland
PH: 73/22 05 92
TLX: 883207

TAIWAN

Far East Electronics, Ltd.
No. 9 Nanking East Road,
Sec. 3
Taipei, 104 Taiwan
Republic of China
PH: 5615444
TLX: 11639

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18651 Von Karman, Irvine, California 92713 Tel 714 833 8830 (TWX 910 595 1767)