NAKED MINI® 4 FAMILY
GENERAL MEMORY
REFERENCE MANUAL

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REVISION HISTORY

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A1	Oct. 1978	Incorporates switch SW2 and resistor-pack RP1 modifications for interleaving and sub module 16K and 32K half-card available with 4/10 Processor.
A2	Jan. 1980	Includes a new board, and general revisions.
B0	Sept. 1980	Manual updated to include models 53819 and 53828 memories.

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PREFACE

The NAKED MINI® 4 Family General Memory Reference Manual contains information on core and semiconductor memories for the NAKED MINI® 4 Family computers. Discussions on functional descriptions, specifications, and special installation requirements are included for each type of memory.

In addition, due to the volatile nature of the semiconductor memories and the consequent possibility of data loss related to power interruptions, a Battery Backup section is included. Discussions include types of memories and batteries, charging, battery pack, expansion, and operation hints.

This manual refers to the model numbers for each memory module and Battery Backup module.

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PART A

INTRODUCTION

SECTION A1 MEMORY FEATURES

SECTION A2 MEMORY BANKING AND INTERLEAVING

A2.1 MEMORY BANKING OPTION

A2.2 MEMORY MODULE INTERLEAVING

A2.3 DEFINITIONS

PART A

INTRODUCTION

A1 MEMORY FEATURES

Computer Automation, Inc., produces a wide range of memories which vary both in type and size of memory. The specific type of memory storage used separates the available memory modules into three categories:

- Core random-access read/write memory modules
- Semiconductor random-access read/write memory modules
- Semiconductor combination memory modules with random-access read/write and read-only memory storage capabilities.

CORE MEMORY MODULES

The core memory modules provide the most stable form of memory storage with both read and write capabilities. The integrity of data stored in core memory is retained when power to the memory module is interrupted. Both half-card and full-card core memory modules are available in a variety of storage capacities. The typical memory cycle time for the full-card core memory modules is 850 to 1200 nsec.

SEMICONDUCTOR READ/WRITE MEMORY MODULES

The semiconductor read/write memory modules usually have a faster memory cycle time than core memories. For example, the full-card semiconductor memory module cycle time is 550 to 700 nsec. The memory storage capacity of a semiconductor memory module usually is larger -- often double or more -- than a core memory module of similar physical size. However, data stored in semiconductor read/write memory is volatile; that is, the data loses its integrity when power to the memory is interrupted. Both half-card and full-card semiconductor read/write memory modules are available in a variety of storage capacities.

SEMICONDUCTOR COMBINATION MEMORY MODULES

The combination memory modules primarily are read-only memory modules that can be programmed with permanent or very infrequently changed data. These memory modules usually provide for up to 2K words of read/write memory in addition to the read-only memory capability. This allows use of a single combination memory module in special-purpose, limited memory applications.

The combination memory modules are available in half-card modules only. The maximum storage capacity of these modules, both read/write and read-only, is 10K words.

Each different module is restricted to a specific type (or types) of read-only memory. However, modules are available for the three most popular types of read-only memory:

- Mask-programmed Read-Only Memory (ROM)
- Programmable Read-Only Memory (PROM)
- Ultraviolet Erasable, Programmable Read-Only Memory (EPROM)

BATTERY BACKUP

NAKED MINI® 4 Family semiconductor RAM memories are equipped with invalid data detection logic. This logic monitors the voltage being supplied to the on-board RAM array and senses if this voltage drops below the "safe" level.

An On-card Battery Backup option is offered with several of the NAKED MINI® 4 Family semiconductor memories. This option consists of a rechargeable nickel-cadmium battery and associated voltage regulator and charging circuits. When fully charged, this battery enables the memory to maintain the integrity of the stored data during a short-term loss of power. Normally the On-card Battery Backup, when fully charged, is able to maintain data integrity for a minimum of two minutes.

A2 MEMORY BANKING AND INTERLEAVING

Computer Automation, Inc., includes the memory banking and interleaving options with some of the core and semiconductor memory modules.

A2.1 MEMORY BANKING OPTION

When the memory banking option is used, the total memory installed in a system can exceed the 64K direct addressing limit of the processor. In addition, memory banking enables (makes available) or disables (restricts the availability of) portions of the total memory installed in a system. The integrity of data stored in a disabled portion of memory and the data-transfer timing are not affected by memory banking.

Because of its selective partitioning feature, memory banking is particularly valuable in multi-user applications, wherein individual system users are restricted to a specific portion of memory, or in applications that require large data bases.

The memory banking option is implemented by a controller that supervises the configuration of memory available to the processor. The 32-bit General-Purpose Intelligent Cable is one such controller that meets the requirements to serve as a memory banking controller.

Figure A1-1 shows how the 32-bit General-Purpose Intelligent Cable fits into the system. The processor, memory, and I/O Distributor connect directly with the MAXI-BUS® interface. The 32-bit General-Purpose intelligent Cable receives command signals from the processor via the I/O Distributor and generates the enabling signals required to configure the memory subsystem. Once set, the specified memory configuration is retained until the 32-bit General-Purpose Intelligent Cable receives a new set of command signals.

Some memory modules are internally partitioned using the sub-module memory banking option.

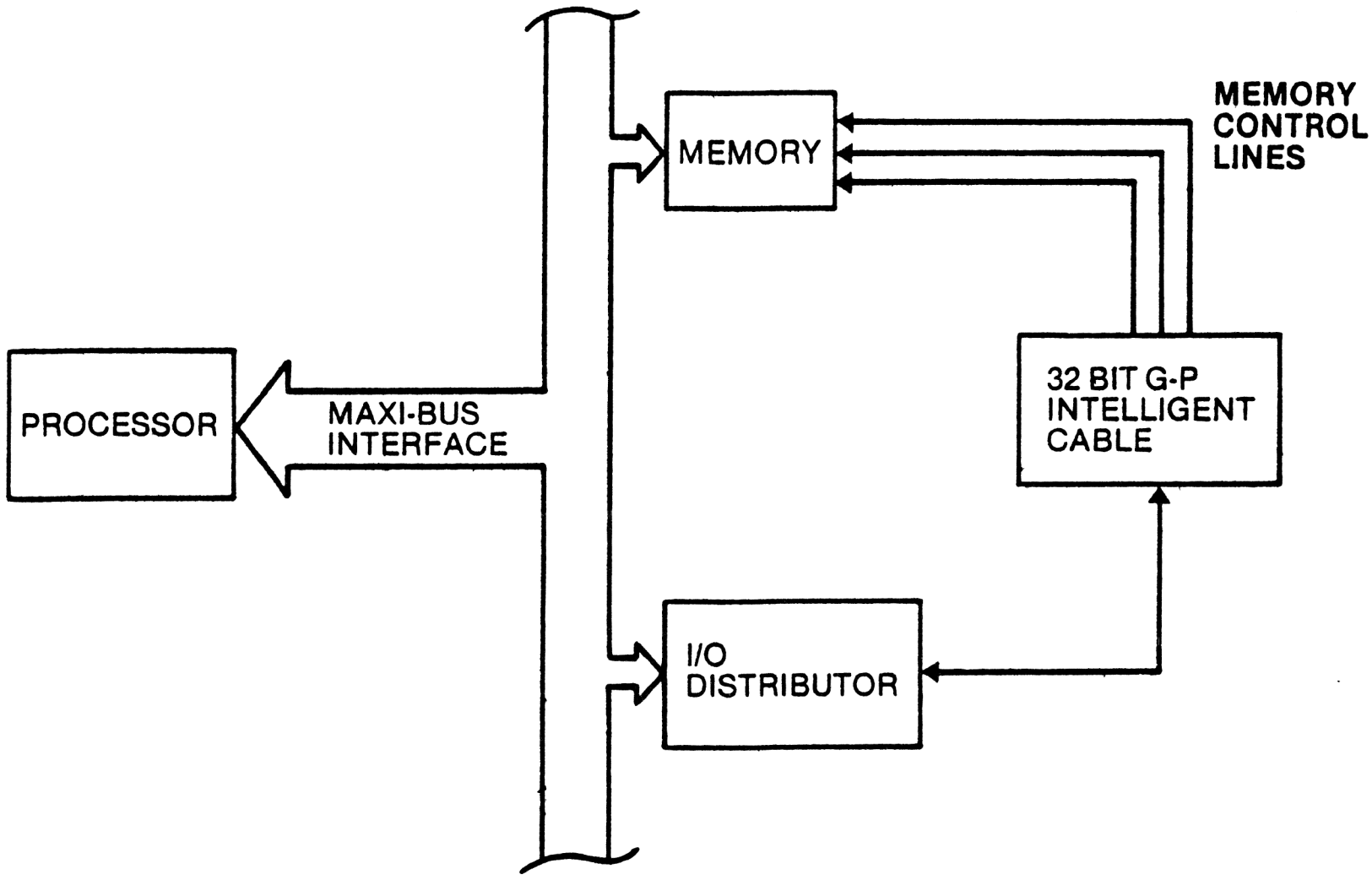


Figure A1-1. Memory Banking System

A2.2 MEMORY MODULE INTERLEAVING

Memory module interleaving is used to decrease the total data transfer time required when blocks of data are being transferred. Single memory transfer times are unaffected by memory module interleaving.

The memory cycle of any memory module can be divided into an access interval and an overhead interval. The access interval is that period of time when data is actually read from or written into memory. The overhead interval is that period of time when the internal logic of the memory module recovers from the access interval. For example, with a core memory read operation, the data is rewritten during the overhead interval.

The memory interleaving feature takes advantage of this memory cycle division to improve data transfer timing. Memory interleaving allows two memory modules to be assigned to the same range of memory addresses. That is, both modules assume the same low limit address. However, one module is strapped to recognize only the even memory addresses and the other is strapped to recognize only the odd addresses. In general, to interleave X words of RAM, use two X/2 word modules. The INTER- and ODD- signals control the module enabling for even and odd memory locations, respectively.

WORD MODE

Figure A1-2 illustrates how a sequence of data transfers affects the interleaved pair of memory modules. Since the access interval for one module can occur during the overhead interval of the other module in the interleaved pair, the effective transfer rate for any given memory module is improved.

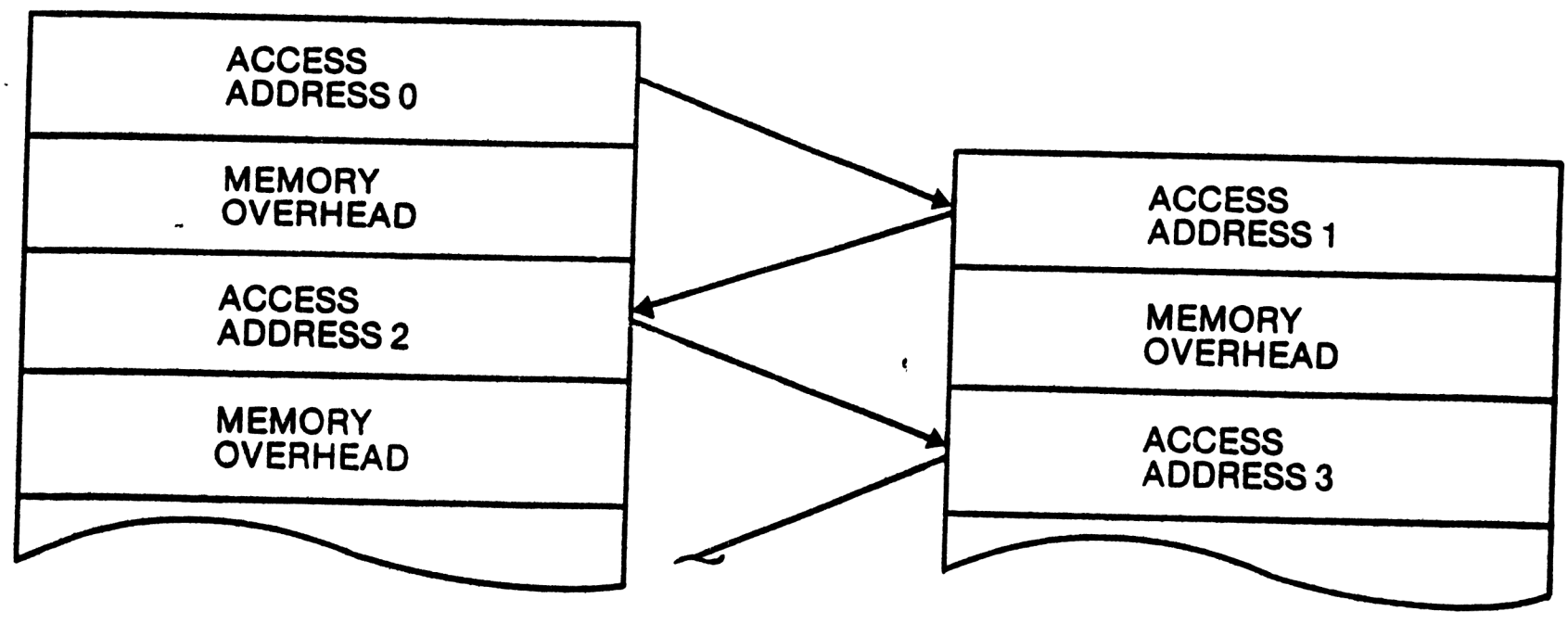


Figure A1-2. Interleaved Memory Access Sequence (Word)

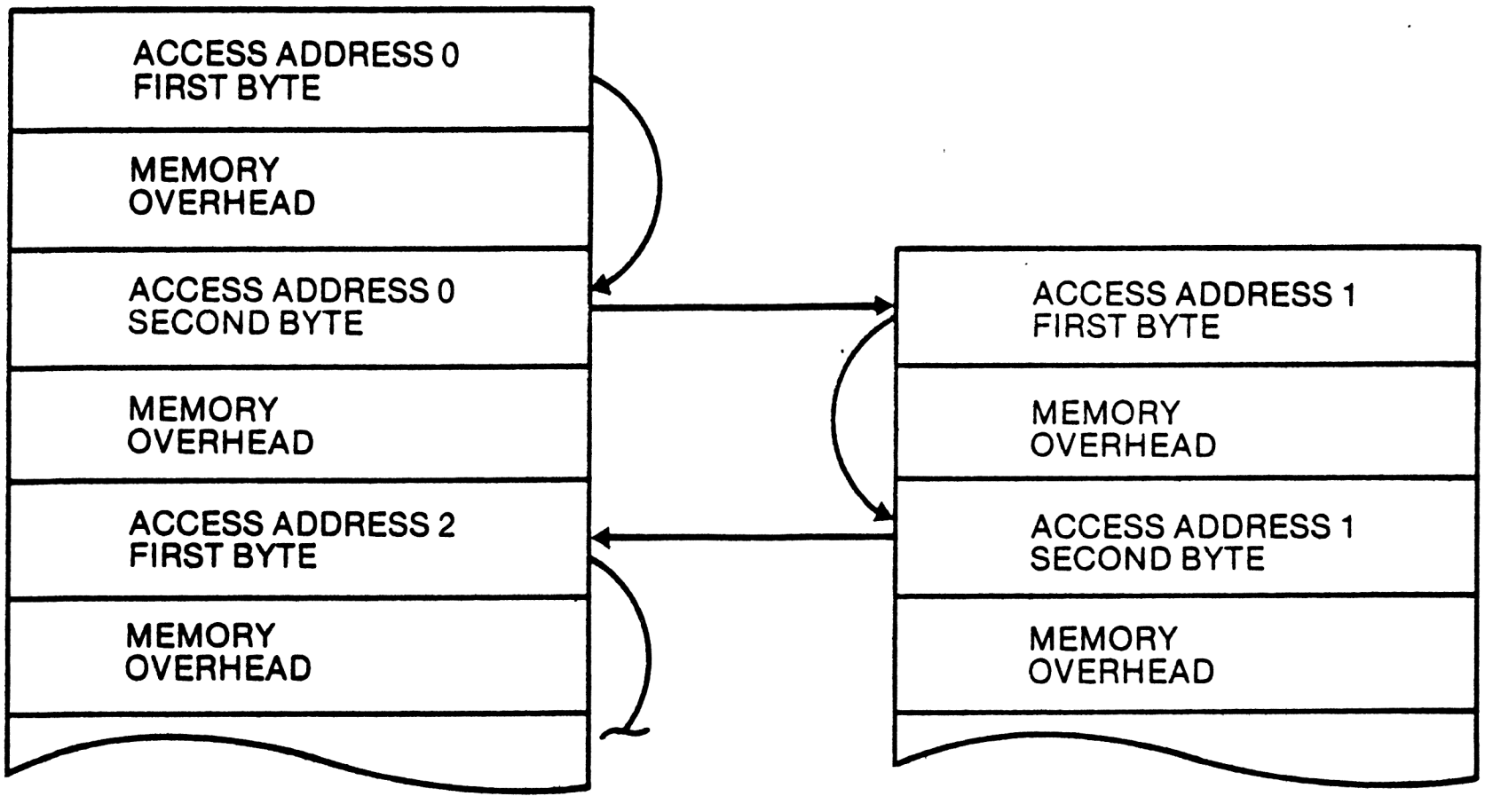


Figure A1-3. Interleaved Memory Access Sequence (Byte)

BYTE MODE

The preceding description of memory interleaving assumed the data transferred was in 16-bit words. When 8-bit bytes are transferred, it is necessary to perform two memory cycles in one memory module before moving to the next memory address in the other memory module of the interleaved pair. This sequence is illustrated in Figure A1-3.

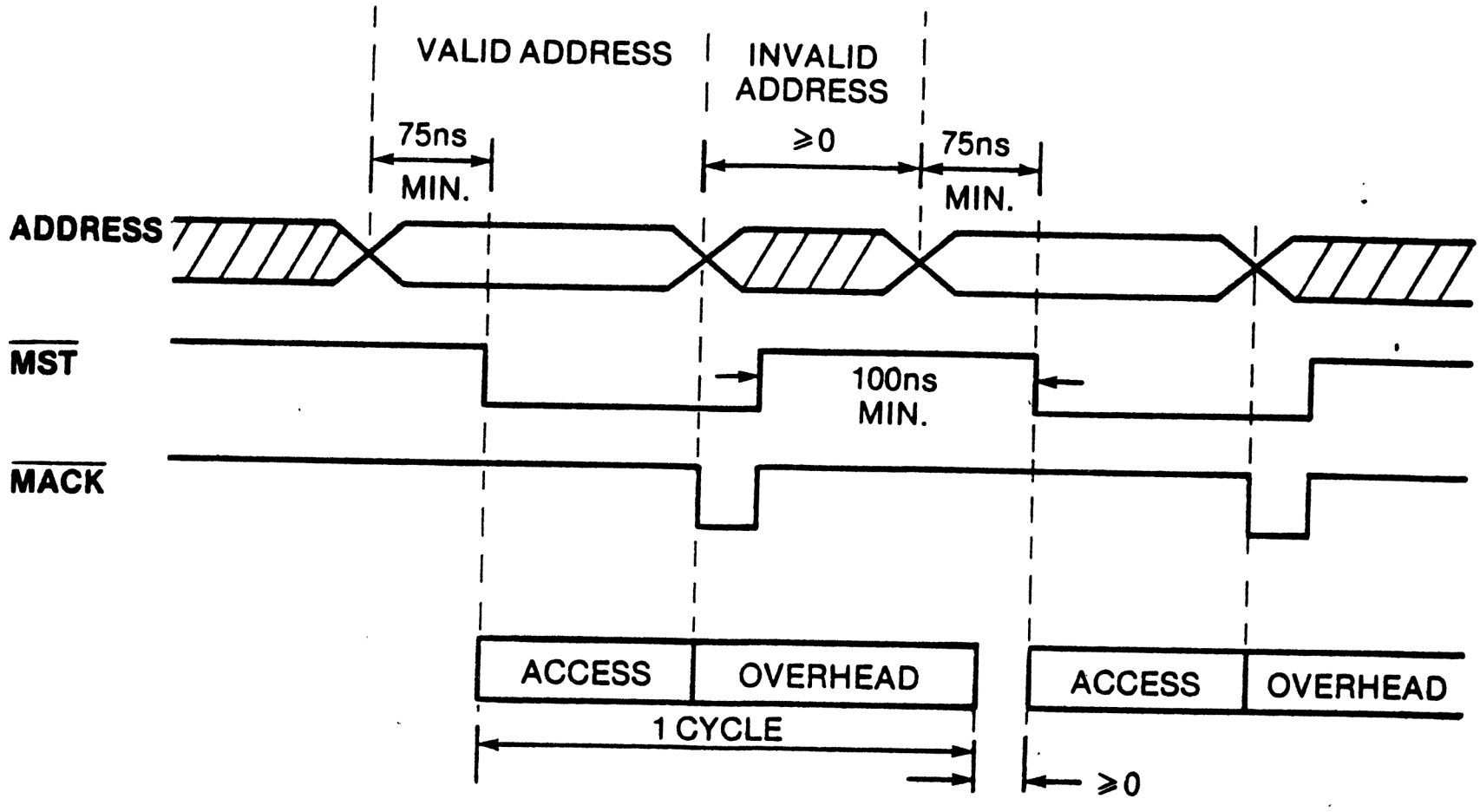


Figure A1-4 . Memory Cycle Timing Without Interleaving

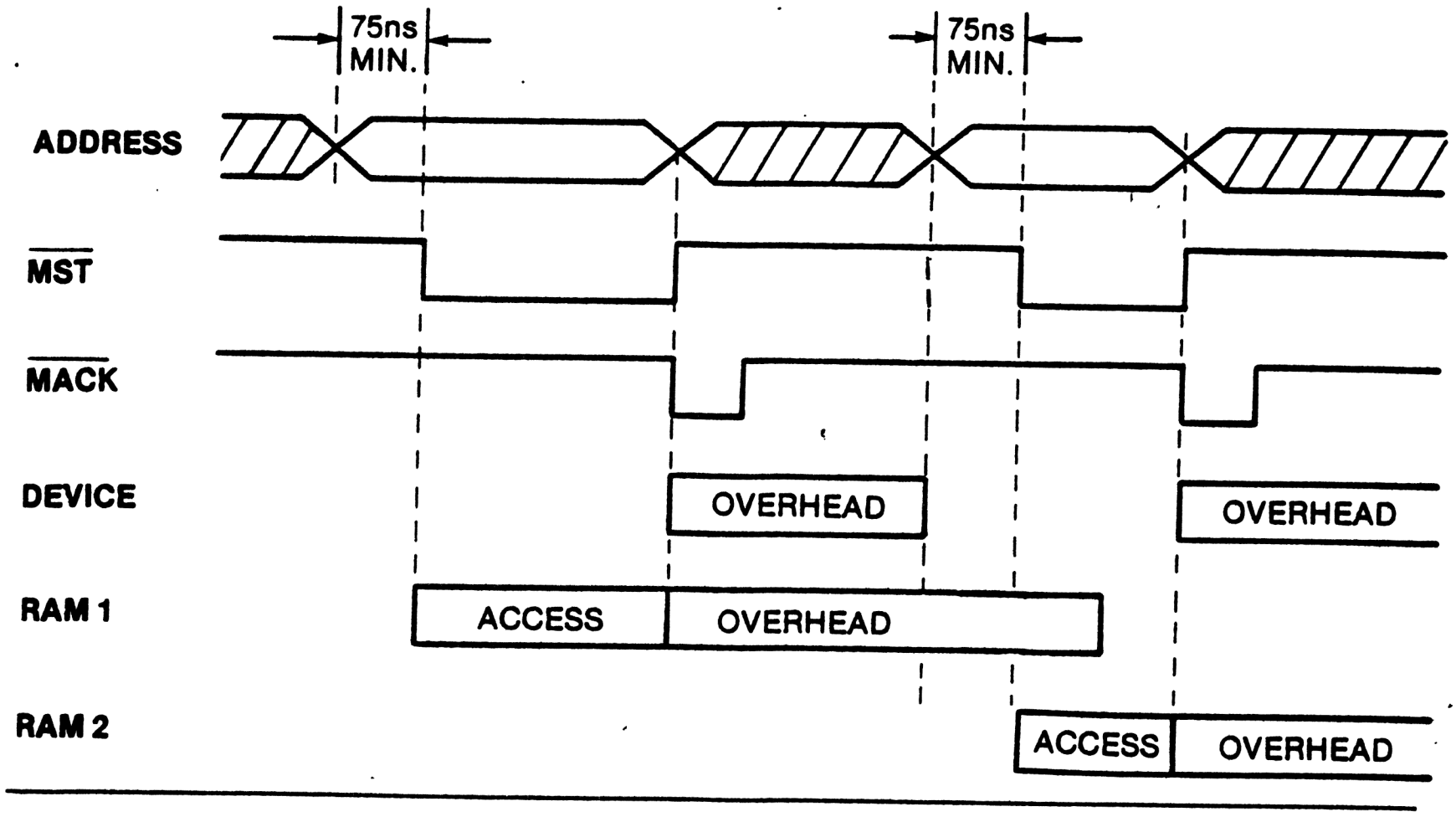


Figure A1-5 . Memory Cycle Timing With Interleaving

A2.3 MEMORY INTERLEAVING TIMING

The effect of using memory interleaving is shown by comparing Figures A1-4 and A1-5. Figure A1-4 shows memory cycle timing when interleaving is not used. As shown in the figure, the processor asserts MST- a minimum of 75 ns after the address on the address bus becomes valid. Asserting MST- initiates the memory access period. The length of the access period, during which data is read from or written into memory, varies with the type of memory. When the access is complete the memory asserts MACK-, indicating to the processor that the bus transfer is complete. The processor then removes MST- and may place the next address on the address bus. This operation may take place in parallel with the RAM1 overhead period.

The MAXI-BUS® Interface imposes the constraint that MST- cannot be reasserted until a minimum of 100 ns after MST- is removed. Because the overhead time is longer than 100 ns for all available memories, this constraint does not effect the memory cycles for non-interleaved memories. If the modules are interleaved, and the next access is to a location in the other of the pair of modules, the access can begin once the 100 ns requirement is met. The timing is shown in Figure A1-5. Typically, the time from MACK- to the next MST- is 200 ns. If the memory overhead is longer than this period, interleaving the memories reduces the apparent cycle time by utilizing part of the overhead time. For memories with a shorter overhead period, no improvement is achieved by interleaving.

A2.4 POWER CONSUMPTION

The meaning of operating and standby power consumption differs for core and semiconductor memories.

For core memories, the maximum operating power consumption refers to the power consumed when the memory is powered, is being accessed by the CPU or a DMA controller, and contains all zero bits. The typical operating power consumption is the amount of power consumed when the memory is powered, is being accessed by the CPU or a DMA controller, and contains an equal number of zero and one bits. Core standby power consumption refers to the power consumed when the memory is powered but is not being accessed.

For semiconductor memories, the operating power consumption is the power consumed when the memory is powered and being accessed by the CPU or a DMA controller. The standby power consumption is the power consumed when the memory is powered but is not being accessed.

PART B

CORE MEMORIES

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B1.2 MEMORY BANKING

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B2.2 8K HALF-CARD - MODEL 11703-08

B2.3 4K FULL-CARD - MODEL 11677-04 AND
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B2.4 16K FULL-CARD - MODEL 11673-16

SECTION B3 CORE INSTALLATION

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B3.2 8K HALF-CARD - MODEL 11703-08

B3.2.1 Joining Requirement
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B3.2.3 Memory Banking Strapping

B3.3 4K FULL-CARD - MODEL 11677-04 AND
8K FULL-CARD - MODEL 11677-08

B3.3.1 Memory Banking Requirements
B3.3.2 Interleaving Requirements
B3.3.3. Interleaving Strapping

B3.4 16K FULL-CARD - MODEL 11673-16

B3.4.1 Memory Banking Requirements
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B3.4.3 Interleaving Requirements

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B1 FUNCTIONAL DESCRIPTION

The storage of digital data requires a device having two stable and distinct states for each bit of data. A core memory uses a torrodial ferrite which has two distinct flux states. The flux state of a core is changed by driving current, with sufficient amplitude, through the wires threaded through the core. The flux remains in either a 0 or 1 state until a current of sufficient amplitude is driven in the opposite direction to cause a change of state.

The core flux direction is detected by driving a current through the core in one direction. If the core changes state, the relatively large flux change is detected by the induced voltage on the sense winding. The reading of a core, therefore, is destructive and will leave the core in a zero state. A write operation then is necessary to restore the data.

The square loop characteristic provides an efficient method of addressing the core. Drive current is provided by two wires threaded through the core with each wire carrying only half the current required to switch the core. A core located at the intersection of the two wires receives full-select current; all other cores receive half-select current.

The sense line is used to detect the switching flux in a read operation and as an inhibit wire during a write. Inhibit current equal in amplitude to the half-select drive current is driven through all cores in one bit when a 0 is to be written; the effect of one of the half-select drive currents is cancelled.

The MAXI-BUS® Interface, an asynchronous negative true bus consisting of address, data, and control signals, provides the computer interface.

The address portion of the MAXI-BUS® Interface consists of lines labeled AB00- through AB15-, Extra Bit of Address (EBA-), and Select Lower Byte (SLB-). Lines AB00- through AB14- and EBA- provide 64K word addressability. Address line AB15- is asserted to perform byte mode addressing. When AB15- is asserted, the SLB- line is valid. When valid, SLB- not asserted selects the upper byte. SLB- asserted selects the lower byte. In byte mode, all data is transmitted on data lines DB00- through DB07-. Data lines DB08- through DB15- are driven high to produce all zeroes.

B2 CORE MEMORY SPECIFICATIONS

B2.1 4K HALF-CARD - MODEL 11671-04

The 4K half-card core memory, Model 11671-04, has a capacity of 4,096 words with 16 bits per word.

The address range of the 4K half-card core memory is :0000 to :7FFF. Extended Addressing cannot be used. For this reason, no address above 32767 should be used in any system with this board. This board will "wrap around" to its address + 32768.

MEMORY CYCLE TIMES (READ AND WRITE, NOMINAL)

Access Interval	0.4 µsec
Overhead Interval	1.6 µsec
Total	3.0 µsec

ENVIRONMENTAL

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Operating Humidity (Percent, Non-Condensing)	10 to 90

NOTE

Free air flow around the unit is required to provide adequate cooling.

PHYSICAL

Length	42.88 cm. (16.88 in.)
Width	19.05 cm. (7.5 in.)
Height	1.52 cm. (0.6 in.)
Weight	1.35 kg. (3 lb.)

ELECTRICAL

Power Dissipation (Maximum, All Voltages)	45 watts
Voltage Regulation (All Voltages)	±2%
Power Consumption	
+12Vdc Typical Operating	0.4a
+12Vdc Maximum Operating	0.4a
+12Vdc Standby	0.3a
-12Vdc Typical Operating	0.2a
-12Vdc Maximum Operating	0.2a
-12Vdc Standby	0.2a
+5Vdc Typical Operating	2.5a
+5Vdc Maximum Operating	3.0a
+5Vdc Standby	1.5a

B2.2 8K HALF-CARD - MODEL 11703-08

The 8K half-card core memory, Model 11703-08, has a capacity of 8,192 words with 16 bits per word.

MEMORY CYCLE TIMES (READ AND WRITE, NOMINAL)

Access Interval	0.4 µsec
Overhead Interval	2.6 µsec
Total	3.0 µsec

ENVIRONMENTAL

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Non-Condensing)	10 to 90

NOTE

Free air flow around the unit is required to provide adequate cooling.

PHYSICAL

Length	42.88 cm.	(16.88	in.)
Width	19.05 cm.	(7.5	in.)
Height	1.52 cm.	(0.6	in.)
Weight	1.35 kg.	(3	lb.)

ELECTRICAL

Power Dissipation (Maximum, All Voltages)	45 watts
Voltage Regulation (All Voltages)	±2%
Power Consumption	
+12Vdc Typical Operating	0.4a
+12Vdc Maximum Operating	0.4a
+12Vdc Standby	0.3a
-12Vdc Typical Operating	0.8a
-12Vdc Maximum Operating	1.4a
-12Vdc Standby	0.2a
+5Vdc Typical Operating	1.8a
+5Vdc Maximum Operating	2.0a
+5Vdc Standby	1.7a

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B2.3 4K FULL-CARD - MODEL 11677-04 AND 8K FULL-CARD - MODEL 11677-08

The 4K full-card core memory, Model 11677-04, has a capacity of 4,096 words with 16 bits per word. The 8K full-card core memory, Model 11677-08, has a capacity of 8,192 words with 16-bits per word.

The following specifications apply to both the 4K- and 8K-memory modules.

MEMORY CYCLE TIMES (NOMINAL)

	READ	WRITE
Access Interval	375 nsec	250 nsec
Overhead Interval	475 nsec	600 nsec
Total	850 nsec	850 nsec
Minimum Interleaved	475 nsec	350 nsec

ENVIRONMENTAL

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Non-Condensing)	10 to 90

NOTE

Free air flow around the unit is required to provide adequate cooling.

PHYSICAL

Length	42.88 cm.	(16.88 in.)
Width	38.10 cm.	(15.0 in.)
Height	1.52 cm.	(0.6 in.)
Weight	1.8 kg.	(4 lb.)

ELECTRICAL

Power Dissipation (Maximum, All Voltages)	96 watts
Voltage Regulation (All Voltages)	±2%
Power Consumption	
+12Vdc Typical Operating	2.5a
+12Vdc Maximum Operating	2.6a
+12Vdc Standby	0.4a
-12Vdc Typical Operating	2.2a
-12Vdc Maximum Operating	4.2a
-12Vdc Standby	0.1a
+5Vdc Typical Operating	2.6a
+5Vdc Maximum Operating	2.8a
+5Vdc Standby	2.5a

B2.4 16K FULL-CARD - MODEL 11673-16

The 16K full-card core memory, Model 11673-16, has a capacity of 16,384 words with 16 bits per word.

MEMORY CYCLE TIMES (NOMINAL)

	READ	WRITE
Access Interval	550 nsec	250 nsec
Overhead Interval	650 nsec	950 nsec
Total	1,200 nsec	1,200 nsec
Minimum Interleaved	650 nsec	350 nsec

ENVIRONMENTAL

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Non-Condensing)	10 to 90

NOTE

Free air flow around the unit is required to provide adequate cooling.

PHYSICAL

Length	42.88 cm.	(16.88 in.)
Width	38.10 cm.	(15.0 in.)
Height	1.52 cm.	(0.6 in.)
Weight	1.8 kg.	(4 lb.)

ELECTRICAL

Power Dissipation (Maximum, All Voltages)	104 watts
Voltage Regulation (All Voltages)	±2%
Power Consumption	
+12Vdc Typical Operating	2.3a
+12Vdc Maximum Operating	2.5a
+12Vdc Standby	0.4a
-12Vdc Typical Operating	2.4a
-12Vdc Maximum Operating	5.2a
-12Vdc Standby	0.1a
+5Vdc Typical Operating	2.65a
+5Vdc Maximum Operating	3.0a
+5Vdc Standby	2.45a

B3 CORE INSTALLATION

There are special installation requirements for memory modules that use interleaving and both module and sub-module memory banking. Both interleaving and memory banking are controlled using the memory control connector; therefore, use of both features at the same time is not recommended due to the resulting installation complications.

B3.1 4K HALF-CARD - MODEL 11671-04

There are no special requirements if the 4K half-card is installed in a half-card chassis. If the 4K half-card module is to be installed in a full-card chassis, the module first must be joined with a half-card processor, an I/O controller, a filler card, or another half-card memory module. When being joined to a half-card processor, the J1 connector on the memory module accepts one end of the 16-pin jumper. Refer to the applicable computer reference manual for information on the joining of half-cards.

The joining of a half-card memory with another half-card module may require modification of the mother board if an expansion chassis is used. Refer to the appropriate computer reference manual if mother board modifications are required.

B3.2 8K HALF-CARD - MODEL 11703-08

B3.2.1 Joining Requirement

There are no special installation requirements if the 8K half-card module is installed in a half-card chassis. If the 8K half-card is to be installed in a full-card chassis, the module first must be joined with a half-card processor, an I/O controller, a filler card, or another half-card memory module. When joined to a half-card processor the J1 connector on the memory module accepts one end of the 16-pin jumper. Refer to the applicable computer reference manual for information on the joining of half-cards.

The joining of a half-card memory with another half-card module requires modification of the mother board if an expansion chassis is used. Refer to the appropriate computer reference manual if mother board modifications are required.

B3.2.2 Memory Banking Requirements

The 8K half-card core module has the memory banking feature which has special installation requirements for the Memory Control Connector, J4.

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B3.2.3 Memory Banking Strapping

The strapping required for memory banking is made on the Memory Control Connector (J2) header (see Figure B3-1). If the memory control cable is changed from primary to alternate or from alternate to primary memory block control, the memory control header must be rewired.

To change from primary to alternate, remove the jumper between pins 8 and 9 and move the enable wire from pin 7 to pin 8.

To change from alternate to primary, move the enable wire from pin 8 to pin 7 and insert a jumper between pins 8 and 9.

Use Metric Gage 3 to 5 (AWG 24-28 solid wire and solder all connections.

Alternate memory modules for a given primary memory module must be located on the MAXI-BUS® interface between the processor and the primary memory.

B3.3 4K FULL-CARD - MODEL 11677-04 AND 8K FULL-CARD - MODEL 11677-08

The 4K full-card core, Model 11677-04, and the 8K full-card core, Model 11677-08, have memory banking and interleaving features; both features require special installation instructions. These instructions apply to both the 4K and 8K full-card modules.

B3.3.1 Memory Banking Requirements

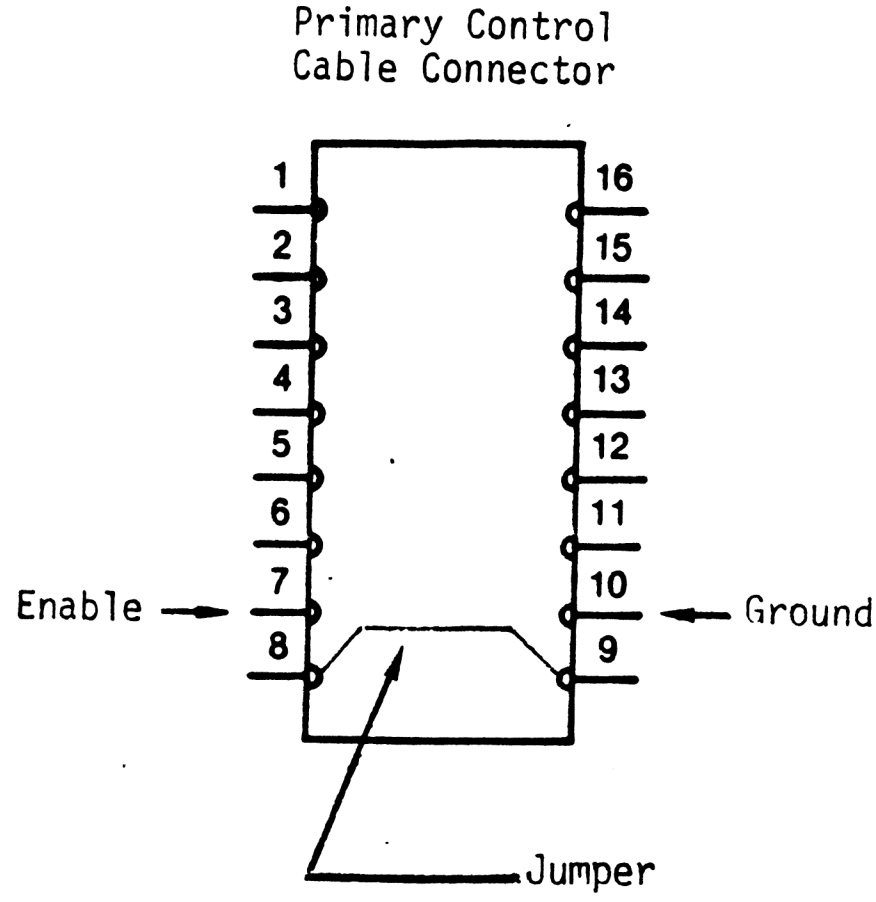
The 4K and 8K full-card core modules have the memory banking feature which has special installation requirements for the Memory Control Connector, J2. The memory banking strapping is detailed in Section B3.2.3.

B3.3.2 Interleaving Requirements

The 4K and 8K full-card core modules have the interleaving feature which has special requirements for the Memory Control Connector, J2.

B.3.3.3 Interleaving Strapping

Each memory module in an interleaved pair is assigned either the odd or even address for the range of addresses covered by the interleaved pair. The two same-sized memory modules are interleaved with the odd memory address module closest to the processor on the MBIN/MBOT priority chain.



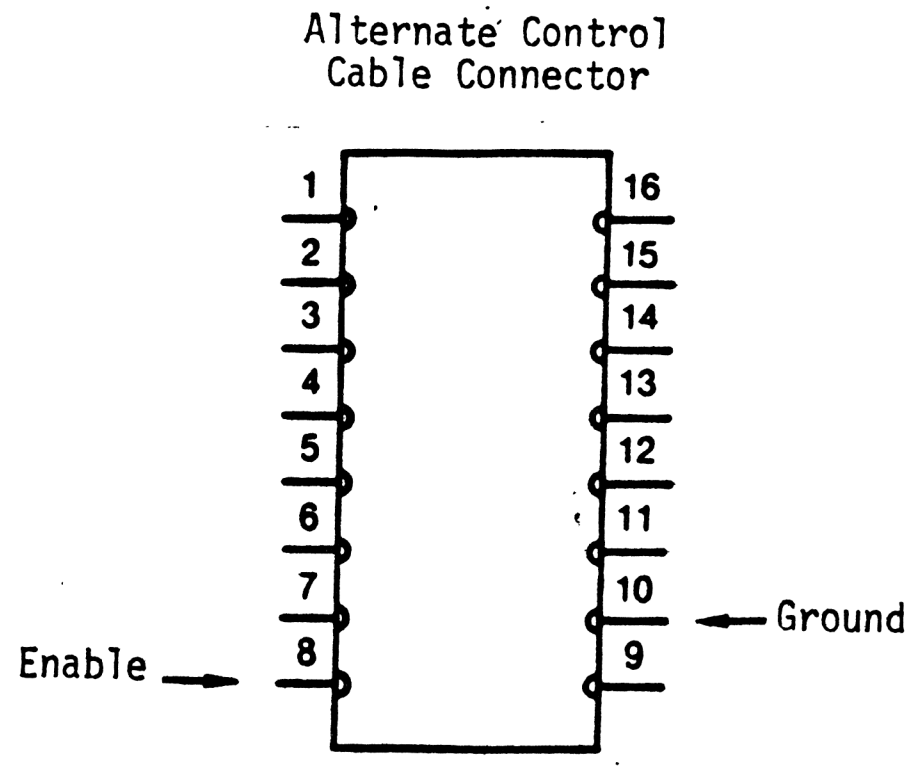


Figure B3-1. Control Cable Connector Wiring

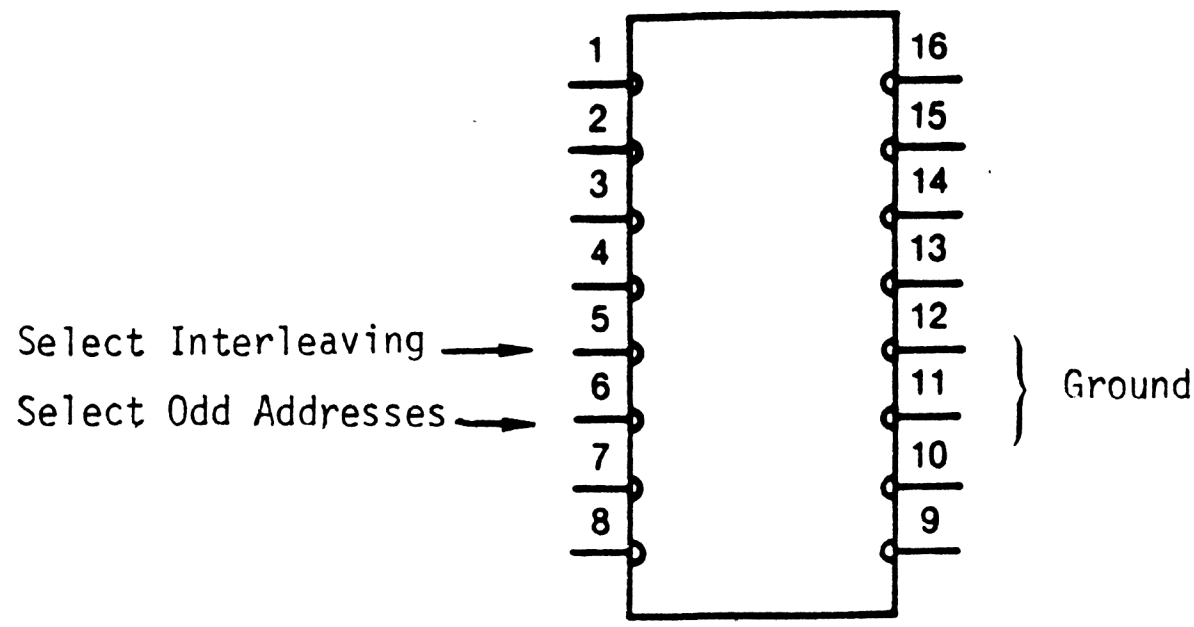


Figure B3-2. Memory Module Interleaving Strapping

The strapping required for interleaving is made on the Memory Control Connector header. Figure B3-2 shows the strapping pin locations on the Memory Control Connector. To select interleaved mode, install a jumper between pins 5 and 12 on each module. One memory module of each interleaved pair of memory modules must be strapped for the odd addresses by installing a second jumper between pins 6 and 11. Use Metric Gage 3 to 5 (AWG 24 to 28) solid wire for the jumpers and solder all connections.

Modules in interleaved mode must be installed in vertically-adjacent slots on the MBIN/MBOT priority chain, with the odd-address module installed closest to the processor. The bottom slot in a chassis is considered adjacent to the top slot in a downstream expansion chassis; however, interleaving of modules should be limited to those modules housed in the primary chassis. The propagation delay induced by the buffer board on the expansion chassis is greater than any timing improvement derived by interleaving.

B3.4 16K FULL-CARD - MODEL 11673-16

The 16K full-card core memory, Model 11673-16, has the module and sub-module memory banking feature. The requirements for the Memory Control Connector, J2, to control module level memory banking are detailed in Section B.3.2.3.

B3.4.1 Sub-Module Memory Banking Strapping

Sub-module memory banking is a feature on the 16K full-card module and has installation requirements for the Memory Control Connector, J2, in addition to those requirements for module level memory banking. Sub-module banking requires either assembly 53673-36, for 2X8K; or assembly 53673-46, for 4X4K banking.

For sub-module memory banking one or two additional wires must be connected to pins 1 and 2 of the Memory Control Connector header to provide the sub-module block selection (see Figure B3-3). The requirements for adding wires are as follows:

Sub-module banking disabled	No wire
Subdivided into two blocks	1 wire (2^1)
Subdivided into four blocks	2 wires (2^1 and 2^0)

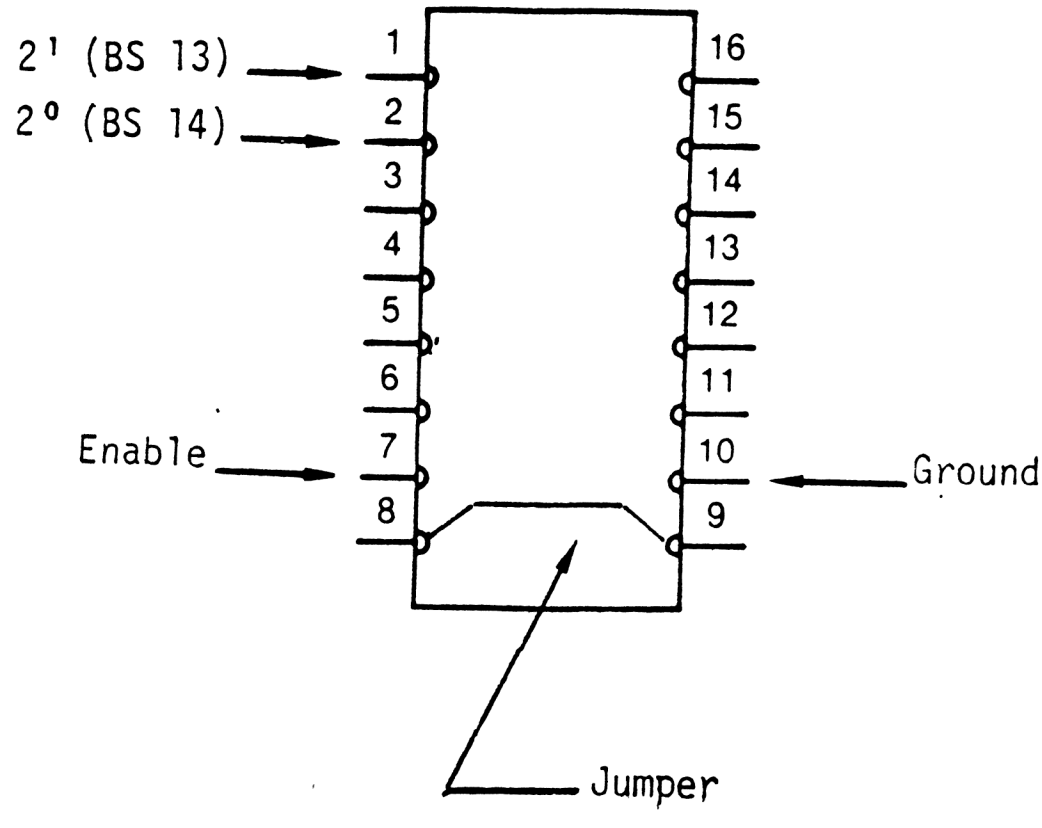
The sub-module block select lines are listed as carrying a binary value that is related to a subdivided block size of 4K words.

B3.4.2 Interleaving Requirements

The 16K full-card module has the interleaving feature which has special installation requirements for the memory control connector, J2. The memory interleaving strapping is detailed in Section B3.3.3.

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PRIMARY CONTROL CABLE CONNECTOR AND STRAPPING



ALTERNATE CONTROL CABLE CONNECTOR AND STRAPPING

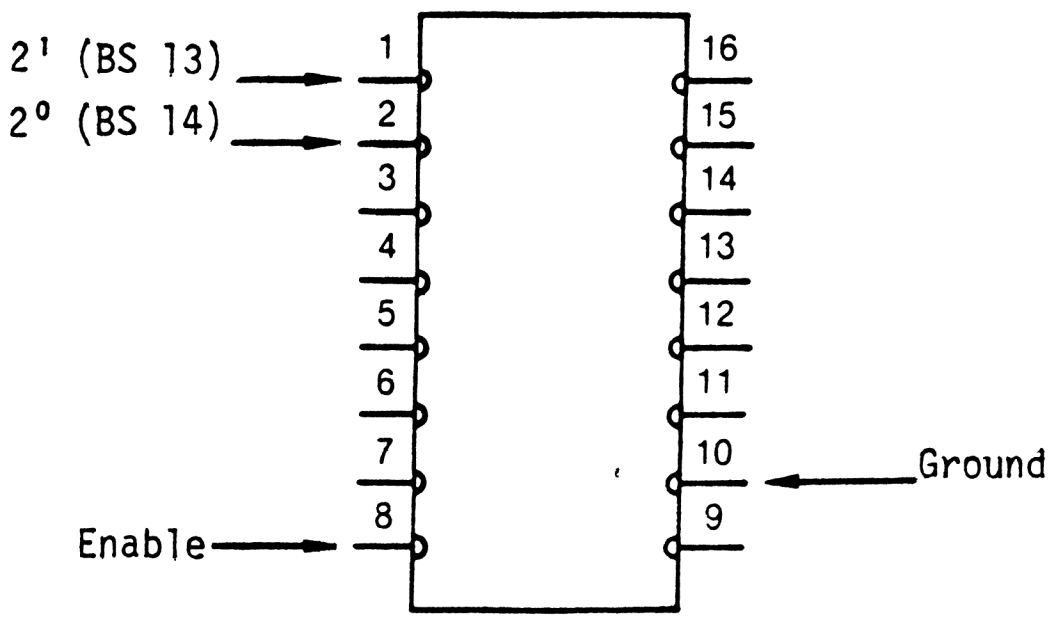


Figure B3-3. Memory Control Cable Connector Wiring

PART C

SEMICONDUCTOR MEMORIES

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- C1.1 INTRODUCTION
- C1.2 SPECIFICATIONS
- C1.3 INSTALLATION
  - C1.3.1 Joining Requirements
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  - C2.3.6 Error Correction Circuitry Testing
- C2.4 MODEL 53828 FULL-CARD SEMICONDUCTOR MEMORY WITH 22-BIT ADDRESSING
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  - C2.4.2 Functional Description

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- C3.1 INTRODUCTION
- C3.2 MODEL 11642 HALF-CARD SEMICONDUCTOR MEMORY MODULE
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- C3.3 MODEL 53775 RANDOM ACCESS SEMICONDUCTOR MEMORY MODULE
  - C3.3.1 Specifications
  - C3.3.2 Installation

C1 COMBINATION SEMICONDUCTOR MEMORY MODULE

C1.1 INTRODUCTION

Computer Automation, Inc., produces semiconductor combination memory modules with up to 2K words of read/write memory (RAM) and sockets for up to 8K words of ultraviolet erasable, programmable read-only memory (EPROM) or mask-programmed, read-only memory. Table C1-1 summarizes the model numbers for the combination memory modules.

The basic storage element is a 256 word by 4 bit n channel static MOS RAM that has a 1 µsec access and cycle time.

The read-only memory (ROM) is a 1K word by 8 bit n channel device with a 450 nsec access and cycle time.

C1.2 SPECIFICATIONS

MEMORY CYCLE TIMES (READ AND WRITE, NOMINAL)

Access Interval	1.4 µsec
Overhead Interval	0 µsec
Total	1.4 µsec

ENVIRONMENTAL

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Non-condensing)	5 to 80

NOTE

Free air flow around the unit is required to provide adequate cooling.

Table C1-1. Combination Memory Model Numbers

WORDS (RAM)	BATTERY BACKUP	
	WITHOUT	WITH
0	53678-00	--
256	--	53678-39
1K	--	53678-59
2K	--	53678-69

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PHYSICAL

Length	42.88 cm.	(16.88	in.)
Width	19.00 cm.	(7.48	in.)
Height	1.52 cm.	(0.6	in.)
Weight	1.35 kg.	(3	lb.)

ELECTRICAL

Power Dissipation (Maximum, All Voltages)	45 watts
Voltage Regulation (All Voltages)	±5%
Power Consumption (No RAM)	
+5Vdc Average Operating	0.9a
+5Vdc Maximum Operating	1.1a
-12Vdc Maximum Operating	2ma
Power Consumption (256 Words RAM)	
+5Vdc Average Operating	1.1a
+5Vdc Maximum Operating	1.3a
-12Vdc Maximum Operating	2 ma
Power Consumption (1K Words RAM)	
+5Vdc Average Operating	1.5a
+5Vdc Maximum Operating	1.78a
-12Vdc Maximum Operating	2ma
Power Consumption (2K Words RAM)	
+5Vdc Average Operating	2.0a
+5Vdc Maximum Operating	2.8a
-12Vdc Maximum Operating	2ma
Addtional Power Consumption Per 1K ROM	
+12Vdc Average Operating	50ma
+12Vdc Maximum Operating	65ma
-12Vdc Average Operating	30ma
-12Vdc Maximum Operating	45ma
+5Vdc Average Operating	6ma
+5Vdc Maximum Operating	10ma

NOTE

When Battery Backup option is used, battery charging results in an additional power consumption at +12Vdc of approximately 12mA.

C1.3 INSTALLATION

C1.3.1 Joining Requirements

There are no special requirements if the combination memory module is installed in a half-card chassis. If the combination memory module is to be installed in a full-card chassis, it first must be joined with a half-card processor, an I/O controller, a filler card, or another half-card memory module. The J1 connector on the memory module (see Figure C1-1) accepts one end of the 16-pin jumper when the half-card combination module is joined to a half-card processor. Refer to the applicable computer reference manual for information on the joining of half-cards.

The joining of a half-card memory with another half-card module could require modification of the mother board if an expansion chassis is used. Refer to the appropriate computer reference manual if mother board modifications are required.

C1.3.2 Switch Settings

There are three sets of switches -- labeled SW1, SW2, and SW3--on the semiconductor combination memory board. SW1 and SW2 are located on the J4 connector: SW1 selects the lower limit of the memory; SW2 selects the memory size. SW3 is located on the P4 plug and selects the battery backup option (see Part D).

SELECTING LOWER LIMIT AND MEMORY SIZE

The lower address limit and memory size are added to form the upper address limit. Each input address received on the Address Bus is compared with the upper and lower address limits. If it is within these limits, the memory board is activated.

Table C1-2 shows how the lower address limit is selected using switches SW1-1 through SW1-6. To select a lower address limit of 32K to 63K, SW1-6 must be in the OFF position, and SW1-1 through SW1-5 remain in the same position as listed in Table C1-2.

Always set the lower address limit 2K below the beginning address of the read-only memory (ROM), regardless of the amount of RAM on the board. If a gap occurs between the end of RAM memory and the beginning of the ROM memory, the gap can be filled using overlap or ghost memory (see Section C1.4.1).

Table C1-3 shows how to specify the memory size using switches SW2-1 through SW2-4. Set the memory size of the configuration equal to or above the actual memory size being used. For example, with 256 words of RAM and a 3K ROM, set the switches as shown for the "X RAM + 4K ROM" configuration.

Table C1-2. Lower Limit Switch Settings

LOWER LIMIT	SW1-6	SW1-5	SW1-4	SW1-3	SW1-2	SW1-1
0	ON	ON	ON	ON	ON	ON
1K	ON	ON	ON	ON	ON	OFF
2K	ON	ON	ON	ON	OFF	ON
3K	ON	ON	ON	ON	OFF	OFF
4K	ON	ON	ON	OFF	ON	ON
5K	ON	ON	ON	OFF	ON	OFF
6K	ON	ON	ON	OFF	OFF	ON
7K	ON	ON	ON	OFF	OFF	OFF
8K	ON	ON	OFF	ON	ON	ON
9K	ON	ON	OFF	ON	ON	OFF
10K	ON	ON	OFF	ON	OFF	ON
11K	ON	ON	OFF	ON	OFF	OFF
12K	ON	ON	OFF	OFF	ON	ON
13K	ON	ON	OFF	OFF	ON	OFF
14K	ON	ON	OFF	OFF	OFF	ON
15K	ON	ON	OFF	OFF	OFF	OFF
16K	ON	OFF	ON	ON	ON	ON
17K	ON	OFF	ON	ON	ON	OFF
18K	ON	OFF	ON	ON	OFF	ON
19K	ON	OFF	ON	ON	OFF	OFF
20K	ON	OFF	ON	OFF	ON	ON
21K	ON	OFF	ON	OFF	ON	OFF
22K	ON	OFF	ON	OFF	OFF	ON
23K	ON	OFF	ON	OFF	OFF	OFF
24K	ON	OFF	OFF	ON	ON	ON
25K	ON	OFF	OFF	ON	ON	OFF
26K	ON	OFF	OFF	ON	OFF	ON
27K	ON	OFF	OFF	ON	OFF	OFF
28K	ON	OFF	OFF	OFF	ON	ON
29K	ON	OFF	OFF	OFF	ON	OFF
30K	ON	OFF	OFF	OFF	OFF	ON
31K	ON	OFF	OFF	OFF	OFF	OFF

Table C1-3. Memory Size Switch Settings

MEMORY SIZE	SW2-4	SW2-3	SW2-2	SW2-1
1K RAM ONLY	ON	ON	ON	OFF
2K RAM ONLY	ON	ON	OFF	ON
X RAM + 2K ROM	ON	OFF	ON	ON
X RAM + 4K ROM	ON	OFF	OFF	ON
X RAM + 6K ROM	OFF	ON	ON	ON
X RAM + 8K ROM	OFF	ON	OFF	ON

Table C1-4. Option Switch Settings - SW2-5 is unused

OPTION	SWITCH	SETTING
1K Overlap	SW1-7 SW1-8	ON OFF
2K Overlap	SW1-8 SW1-7 SW2-8	ON OFF OFF
Ghost Memory	SW2-8	ON
Automatic Start-up	SW2-7 SW2-6	ON ON

SELECTING MEMORY OPTIONS

The semiconductor combination memory options include overlap, ghost memory, and Automatic Start-up. Table C1-4 summarizes the switch settings used to select a memory option.

C1.4 MEMORY OPTIONS

C1.4.1 Overlap and Ghost Memory

If the semiconductor combination memory module has less than 2K words of RAM, a gap will exist between the end of the RAM and the beginning of the ROM. The gap will vary between zero words (with 2K of RAM memory on the board) and 2K words (with no RAM memory on the board). The gap is filled in either of two ways: overlap or ghost memory.

If the combination memory module is not the first (lowest address) memory in the system, the gap can be filled by overlapping with the preceding (lower address) memory. The preceding memory must be large enough to cover the gap. Switch settings for overlap are shown in Table C1-4.

The ghost memory feature when enabled to fill the gap, spreads whatever RAM is on the board (256, 1K, or 2K words) across the entire 2K area allotted for RAM. For example, if there are 256 words of RAM, the ghost memory feature causes a given RAM location to respond to eight different addresses, each address 256 words from the adjacent address. Ghost memory does not affect the addressing of the read-only memory. For example, the same location could be addressed as :X064, :X164, :X264, or :X364 (assuming 256 words are installed and ghosted).

It should be noted that only integer power of two amounts of RAM may be installed if the user wishes to use ghosting. Thus, while 256 words, or 512 words of RAM could be used, with the rest of the addressing space ghosted or overlapped, 768 words could not be used ($768 = 2^{9.58}$). It is possible, say, to install 768 words in the upper K of the RAM space, and eliminate the the lower K by overlapping, but the 256 word gap cannot be eliminated.

NOTE

The ghost memory feature does not increase the amount of memory, but makes existing on-board RAM easier to address. Since each RAM location responds to two or more addresses, depending upon the amount of on-board RAM, care must be taken to avoid accidentally writing over data stored previously at the same RAM location.

C1.4.2 Automatic Start-Up

Automatic Start-up (ASU) initiates execution of a power-up service routine at initial power on time and upon resumption of power following a power failure. The read-only (ROM) portion of memory can be used to store a custom or user AutoLoad program in lieu of an optional AutoLoad Read-Only Memory. The Auto-Load program is contained in the lowest ROM memory location in the system. This ROM must be in a lower address space than any core location in the system.

To initiate ASU manually, place the computer in the Run enable mode and depress AUTO (on the programmer's console) or START (on the operator's console). Pressing one of these switches sets the Invalid Data Detect (IDD) flip-flop which disables the RAM memory. In addition, the IDD flip-flop forces a power-fail sequence by firing a 15-millisecond one shot power surge. When the one shot surge has timed out, the processor will initiate a power-up sequence. The processor then begins executing instructions at :0080. This location must be in semiconductor RAM. Since RAM is disabled, all RAM locations will be interpreted as zeros (no-op instructions). The processor will pass or bubble through each RAM location until the first ROM location is reached. This location must contain either a jump instruction to an ASU routine or the first instruction in the ASU routine.

To enable RAM, a store instruction must occur somewhere within the AutoLoad program. After the processor has addressed the ROM section or after a write (store) operation has been performed, the IDD flip-flop will be reset and RAM will be enabled.

ASU can be initiated automatically at power-up. Applying power to the computer will set the IDD flip-flop, which disables RAM and causes the processor to "bubble" through RAM to the first instruction in ROM.

C1.5 EPROM MEMORY ARRAY

C1.5.1 Description of EPROM

The socketed EPROM array is designed to accomodate up to 16 Intel 2708 Erasable, Programmable Read-Only Memory chips (or equivalent), where each Intel 2708 provides 1K by 8 bits of storage. The metal-masked ROM version of this chip, Intel 2308, (or equivalent) also can be used if desired. These chips are not included with the Memory Board and must be ordered directly from the manufacturer.

Table C1-5 shows the correlation between the 16 possible EPROMs and portions of a user's EPROM program (by address relative to the Lower Limit).

A low at an EPROM address input corresponds to a logical zero in the computer system. A low at an EPROM data output corresponds to a logical one in the computer system. Intel ships its 2708 and 2308 chips with all their data written as high levels (logical zeros) to the system.

Table C1-5. EPROM Socket Locations

ADDRESS ABOVE LOWER LIMIT (HEXADECIMAL)	EPROM FOR DATA BITS 8-15	EPROM FOR DATA BITS 0-7
:0800-:0BFF	86	87
:0C00-:0FFF	88	89
:1000-:13FF	90	91
:1400-:17FF	92	93
:1800-:1BFF	94	95
:1C00-:1FFF	96	97
:2000-:23FF	98	99
:2400-:27FF	100	101

C1.5.2 ROM/PROM Format Generator

The ROM/PROM Format Generator, ROMGEN, is a Computer Automation, Inc., utility program for generating input patterns required by the following vendors in the manufacture of ROMs, PROMs (EPROMs):

Data I/O - Universal PROM Programmer
Electronic Arrays
Intel
Monolothic Memories
Signetics
Texas Instruments

The ROMGEN program is supplied on paper tape (Part Number 00-96060-40),or on floppy disk (93060-02)in standard Computer Automation, Inc., object format, which can be loaded via any NAKED MINI® 4 binary loader. It requires a minimum of 4K words of memory, and a terminal for operator communication and (or) input; a tape reader (e.g., ASR-33 TTY) can, alternately, be used for input.

The formatted output is to a high-speed paper tape punch, the TTY punch or EBCDIC patterns on magnetic tape, which are card images that can be used to produce a card deck.

For more information, see the ROM/PROM Format Generator (ROMGEN) Manual (93060-90).

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C1.6 POWER FAIL SEQUENCE

Semiconductor RAM memories are volatile in nature. That is, they can lose data if the supply voltage from the computer drops below a preset "safe" level. For this reason, all NAKED MINI® 4 Family memories that contain semiconductor RAM are equipped with invalid data detection logic. If the voltage being supplied to the board drops below the "safe" level, the invalid data detection logic indicates whether the integrity of the data has been maintained.

If the supply voltage does drop below this level, the memory disable signal will switch the board to Battery Backup power, if this option is installed (see Part D). If Battery Backup is not present, or is exhausted, the invalid data detection logic will set an internal memory flip-flop, called Invalid Data Detect (IDD).

The IDD flip-flop disables RAM on the board, and causes it to respond to any subsequent memory read operation by putting all zeros (no-op instructions) on the data bus. Read operations from ROM are not affected.

All LSI 4 Series memories are "connected" together by the ALSP- line. If one memory loses RAM power, the IDD flip-flop is set, and the ALSP- line is driven low. Each semiconductor memory in the system receives the ALSP- line and sets its own IDD flip-flop.

When power returns, the RAM will remain disabled until the IDD flip-flop is reset. This resetting can be accomplished by a COPY (store) to memory instruction to any location in installed RAM. Once IDD is reset, normal operation is resumed.

C2 RANDOM ACCESS FULL-CARD SEMICONDUCTOR MEMORY MODULES

C2.1 INTRODUCTION

Computer Automation, Inc., produces three full-card semiconductor RAM memory modules designed for interface with all LSI Series and NAKED MINI® 4 Family computers. The modules are designated 53707, 53819, and 53828, and are described in subsections C2.2, C2.3, and C2.4, respectively.

C2.2 MODEL 53707 FULL-CARD SEMICONDUCTOR MEMORY MODULE

The Model 53707 memory module is available in two basic models, one of which uses a medium speed and the other a high speed RAM. Each basic model is available in configurations of from 16K byte to 32K byte, and with optional battery back-up, with or without parity. Interleaving and memory module banking are standard features on all models. The 11600-08, 11611-32, and 11701-32 models allow sub-module memory banking. Table C2-1 summarizes the available models.

C2.2.1 Specifications

MEMORY CYCLE TIMES

A minimum cycle time occurs if a refresh signal (see Section C2.4.2) is sent at the end of a normal memory cycle. A "worst case" or maximum cycle time occurs if a refresh signal is sent at the beginning of a normal memory cycle. Refresh cycle time is equal to normal memory cycle time; the maximum cycle time is double the minimum cycle time.

Table C2-1. Memory Identification

MODEL	DESCRIPTION	XX*
11600-XX	Medium Speed RAM	8, 16, 32
11601-XX	Medium Speed RAM with BBU	8, 16, 32
11611-XX	Medium Speed RAM with BBU and Parity	16, 32
11700-XX	Fast Speed RAM	16, 32
11701-XX	Fast Speed RAM with BBU	16, 32
11711-XX	Fast Speed RAM with BBU and Parity	16, 32

*08 = 16K byte capacity, 16 = 32K byte capacity, 32 = 64K byte capacity

The minimum cycle times for read and write operations and the minimum cycle time using interleaved modules are as follows:

Models 11600-XX and 11601-XX

Access Interval	420 ns
Overhead Interval	285 ns
Total	705 ns
Minimum Interleaved	520 ns

Model 11611-XX

Access Interval	495 ns
Overhead Interval	210 ns
Total	705 ns
Minimum Interleaved	595 ns

Models 11700-XX and 11701-XX

Access Interval	315 ns
Overhead Interval	235 ns
Total	550 ns
Minimum Interleaved	415 ns

Model 11711-XX

Access Interval	380 ns
Overhead Interval	170 ns
Total	550 ns
Minimum Interleaved	480 ns

ENVIRONMENTAL

Operating Temperature Range (Degrees Celsius)	0 to +50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Non-Condensing)	5 to 80

NOTE

Free air flow around the unit is required to provide adequate cooling.

PHYSICAL

Length	42.88 cm.	(16.88 in.)
Width	38.10 cm.	(15 in.)
Height	1.52 cm.	(0.6 in.)
Weight	1.3 kg.	(3.5 lb.)

ELECTRICAL

Voltage Regulation (All Voltages)	±5%
Power Consumption - 550 nsec	
+12Vdc Typical Operating	1.25 A
+12Vdc Maximum Operating	2.0 A
+12Vdc Standby	0.8 A
-12Vdc Typical Operating	0.02 A
-12Vdc Maximum Operating	0.2 A
-12Vdc Standby	0.02 A
+5Vdc Typical Operating	1.5 A
+5Vdc Maximum Operating	2.0 A
+5Vdc Standby	1.5 A
Power Consumption - 705 nsec	
+12Vdc Typical Operating	1.20 A
+12Vdc Maximum Operating	2.0 A
+12Vdc Standby	0.8 A
-12Vdc Typical Operating	0.02 A
-12Vdc Maximum Operating	0.2 A
-12Vdc Standby	0.02 A
+5Vdc Typical Operating	1.5 A
+5Vdc Maximum Operating	2.0 A
+5Vdc Standby	1.5 A

C2.2.2 Installation

The random access read/write memory (RAM) is a full-card module, as shown in Figure C2-1. Special installation requirements are described in the following paragraphs. Both interleaving and memory banking are controlled using the Memory Control Connector; therefore, use of both features at the same time is not recommended due to the resulting installation complications.

CAUTION

The RAM memory board has on-board MOS memory devices that are sensitive to static electricity. Caution should be used when handling or installing the module to insure the highest degree of reliability.

C2.2.2.1 Module Installation

Prior to removing or installing modules with the battery backup feature in a chassis, it is necessary to set the INT/EXT switch S3 to INT and ensure that no external batteries are connected to the external battery connectors P3 and P4. Then set the INT/EXT Switch S3 to EXT, and proceed with the installation or removal.

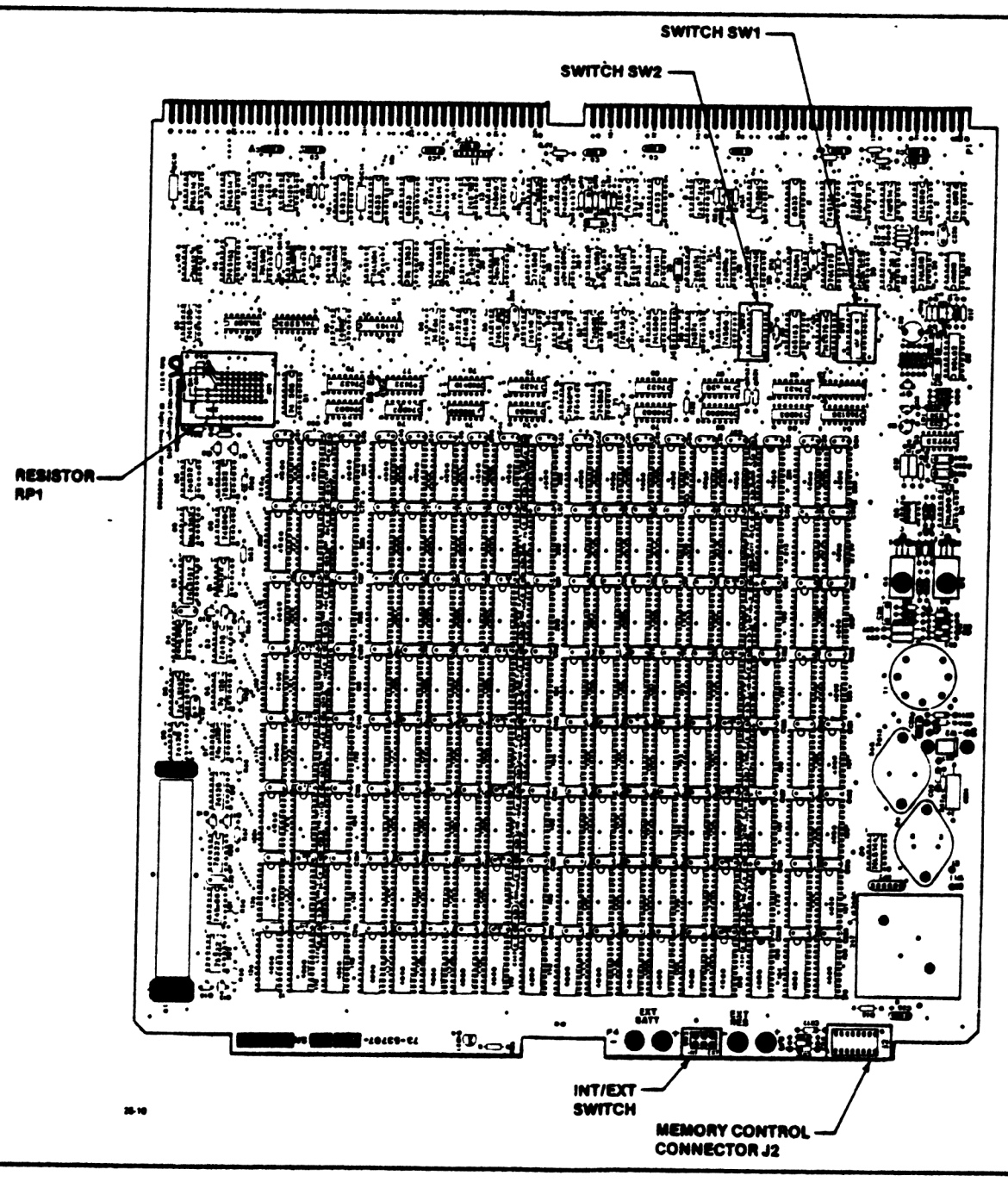


Figure C2-1. Random Access Full-Card Memory Module

CAUTION

Failure to disconnect external backup batteries and/or internal battery backup prior to removing/installing module in chassis may result in damage to the module.

Each memory module in an interleaved pair is assigned either the odd or even address for the range of addresses covered by the interleaved pair. The two same size memory modules are interleaved with the odd memory address module closest to the processor on the MBIN/MBOT priority chain.

The strapping required for interleaving is made on the Memory Control Connector header. Figure C2-2 shows the strapping pin locations on the Memory Control Connector. To select interleaved mode, install a jumper between pins 5 and 12 on each module. One memory module of each interleaved pair of memory modules must be strapped for the odd addresses by installing a second jumper between pins 6 and 11. Use AWG 24 to 28 (Metric Gage 3 to 5) solid wire for the jumpers and solder all connections.

Modules in interleaved mode must be installed in vertically-adjacent slots on the MBIN/MBOT priority chain, with the odd-address module installed closest to the processor. The bottom slot in a chassis is considered adjacent to the top slot in a downstream expansion chassis. However, interleaving of modules should be limited to those modules housed in the primary chassis; the propagation delay induced by the buffer board on the expansion chassis is greater than any timing improvement derived by interleaving.

C2.2.2.2 Memory Banking Requirements

The RAM memory module has module and sub-module memory banking features which both require special installation procedures for the Memory Control Connector, J2.

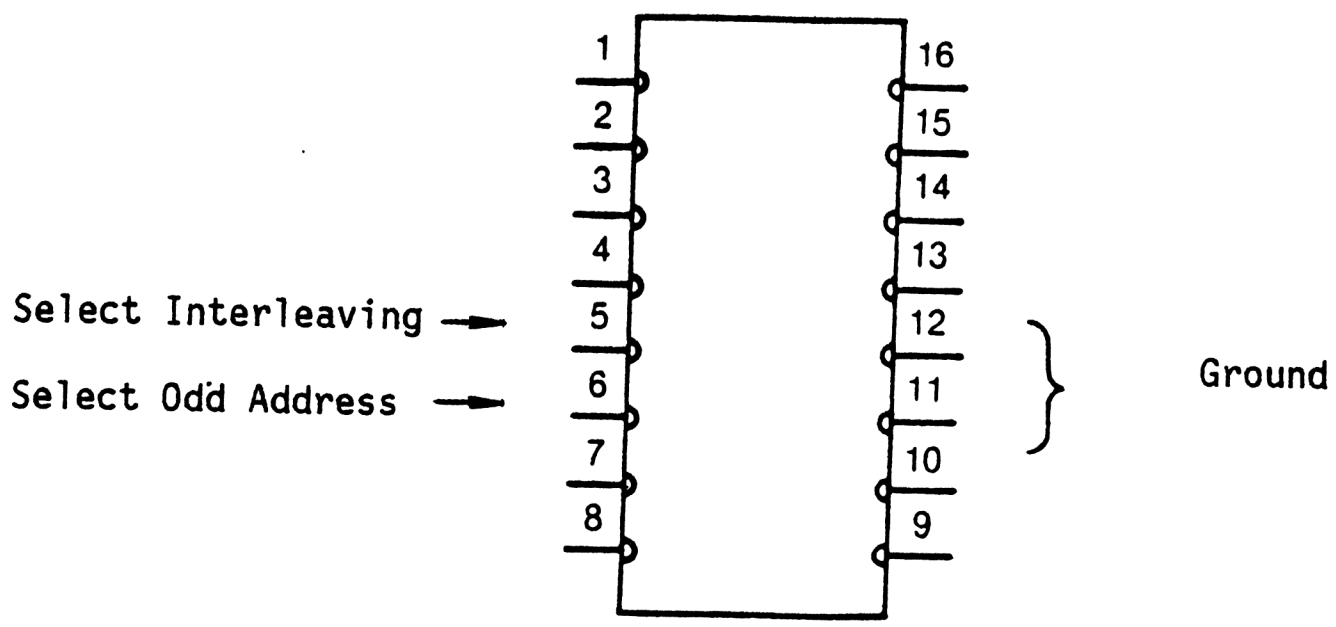
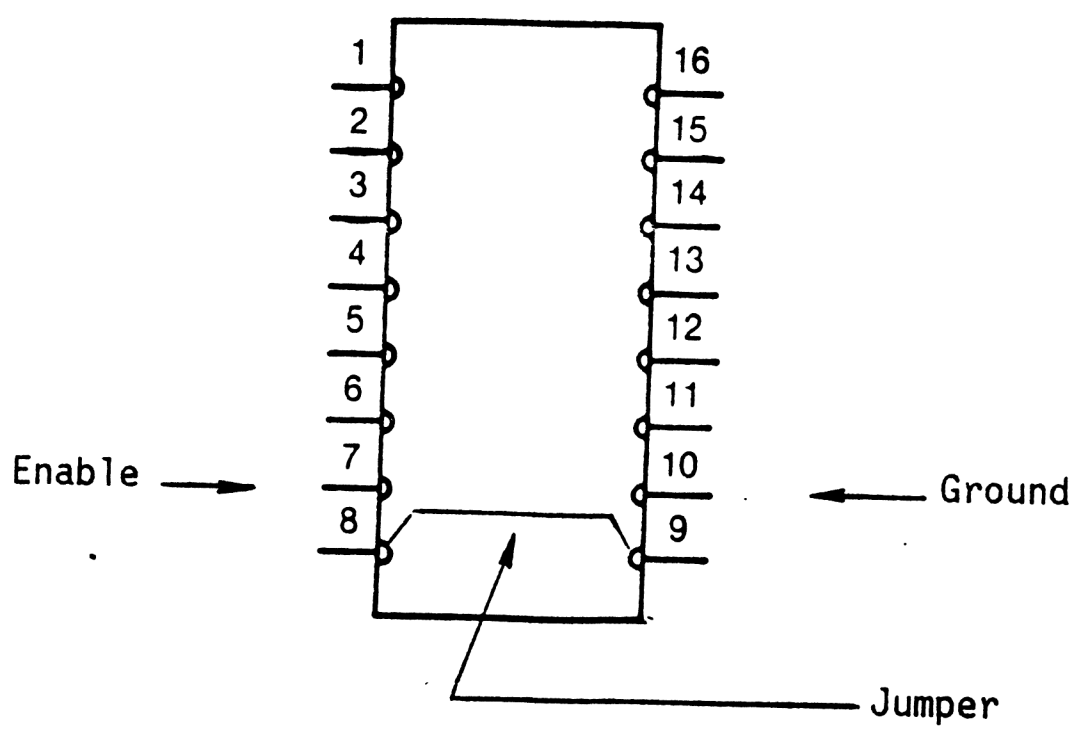


Figure C2-2. Memory Module Interleaving Strapping

MODULE MEMORY BANKING STRAPPING

The strapping required for memory banking is made on the Memory Control Connector header (see Figure C2-3). If the memory control cable is changed from primary to alternate or from alternate to primary memory block control, the memory block must be rewired.

PRIMARY CONTROL CABLE CONNECTOR



ALTERNATE CONTROL CABLE CONNECTOR

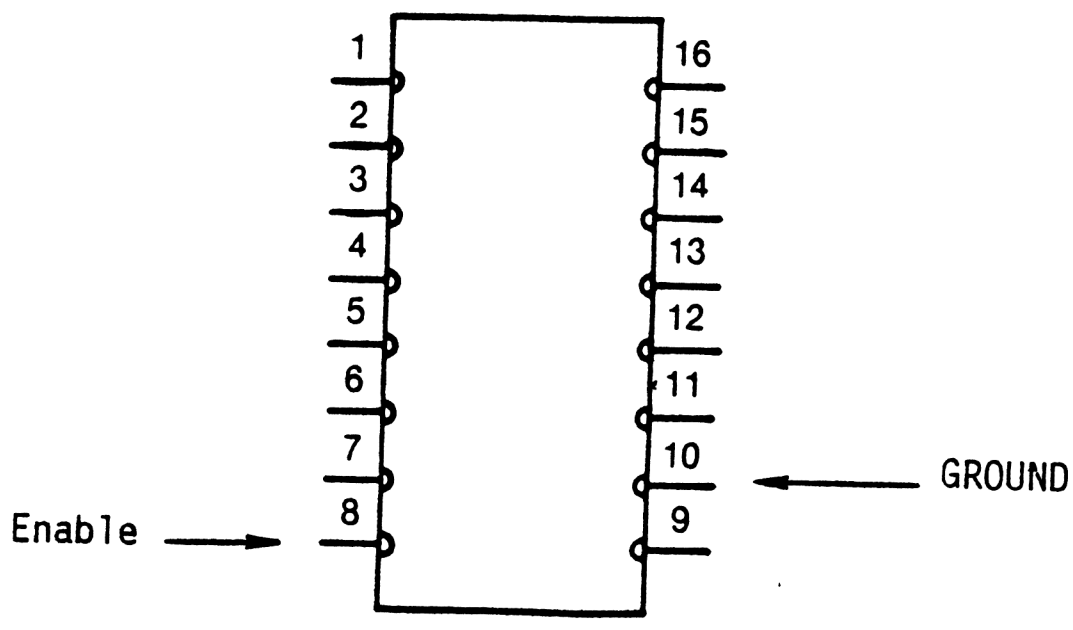


Figure C2-3. Control Cable Connector Wiring

To change from primary to alternate, remove the jumper between pins 8 and 9, and move the enable wire from pin 7 to pin 8.

To change from alternate to primary, move the enable wire from pin 8 to pin 7, and insert a jumper between pins 8 and 9.

Use AWG 24 to 28 (Metric Gauge 3 to 5) solid wire and solder all connections.

Alternate memory modules for a given primary memory module must be located on the MAXI-BUS® Interface between the processor and the primary memory.

SUB-MODULE MEMORY BANKING STRAPPING

Sub-module memory banking requires additional modification to those required for module level memory banking.

To provide the sub-module block selection, up to three additional wires must be connected to pins 1, 2, and 3 of the Memory Control Connector, J2, (see Figure C2-4).

The requirements for adding wires are as follows:

Sub-module Banking Disabled	No Wires
Subdivided into two blocks	1 wire (2^1)
Subdivided into four blocks	2 wires (2^1 and 2^0)
Subdivided into eight blocks	3 wires (2^1,2^0, and 2^2)

The sub-module block select lines are listed as carrying a binary value that is related to a subdivided block size of 8K bytes.

Sub-module memory banking is implemented by connecting the external bank select lines, BS12- to BS14-, to the Memory Control Connector, J2 and by installing Resistor Pack 1. Table C2-2 shows the switch settings required to provide the sub-module banking configuration, and the switch setting to select operation in a LSI-2 series or NAKED MINI® 4 environment.

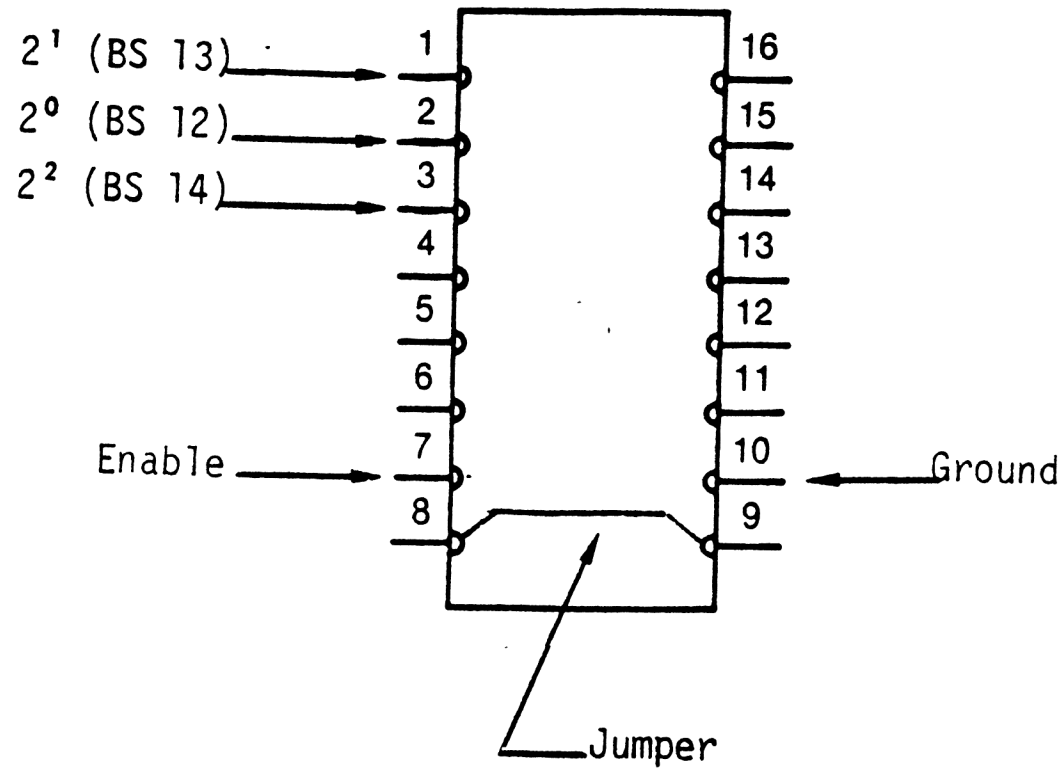
Table C2-2. Sub-Module Memory Banking Switch Settings

BANKING CONFIGURATIONS	SW1-1	SW1-2	SW1-3	SW1-4	SW1-5	SW1-6
2 x 4K	ON	OFF	OFF	ON	OFF	ON
4 x 4K	ON	OFF	ON	OFF	OFF	ON
8 x 4K	ON	OFF	ON	OFF	ON	OFF
2 x 8K	OFF	ON	ON	OFF	OFF	ON
4 x 8K	OFF	ON	ON	OFF	ON	OFF
2 x 16K	OFF	ON	OFF	ON	ON	OFF
NO BANKING	OFF	ON	OFF	ON	OFF	ON

ALL CONFIGURATIONS	SW2-1	SW2-2	SW2-4	SW2-5	SW2-6	SW2-7	SW2-8
	ON	OFF	OFF	*	OFF	OFF	ON

*SW2-5 is OFF for LSI-2, LSI-3 systems, ON for LSI-4 systems.

PRIMARY CONTROL CABLE CONNECTOR



ALTERNATE CONTROL CABLE CONNECTOR

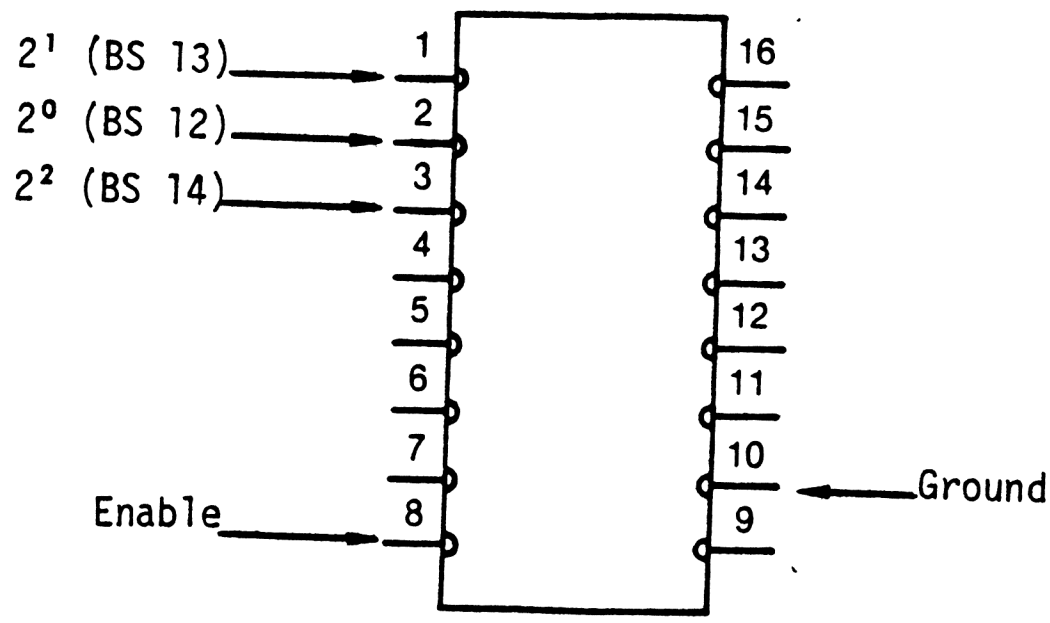
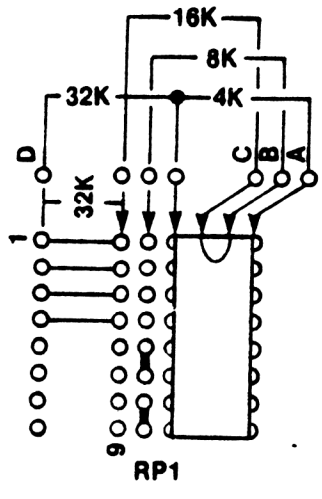
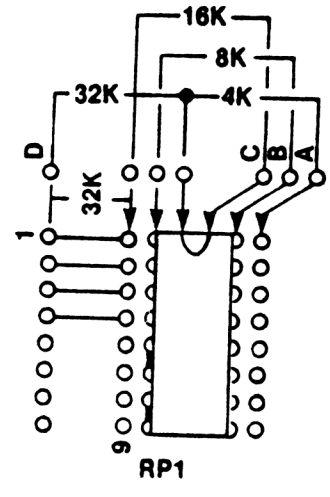


Figure C2-4. Memory Control Cable Connector Wiring

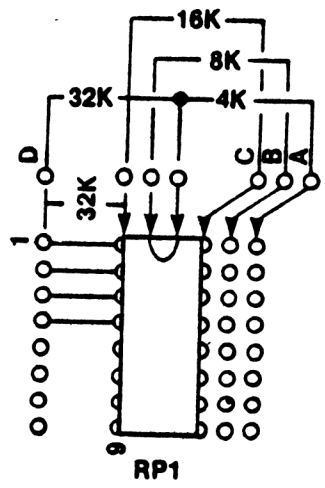
To implement sub-module memory banking, resistor pack RP-1 must be installed in the position corresponding to the desired size of each bank. See Figure C2-5 for detail, and C2-1 for the location of the resistor pack on the card. Use of sockets for the resistor pack is recommended under two conditions. The first condition is where the use of the soldering tool on the resistor pack directly may result in heat damage to it, and the second is where the user wishes to retain the ability to re-configure the module. In the latter case particularly the use of seven 8 pin SIP (Single In-line Pin) sockets is recommended. RP1 is a ten ohm 8 resistor device. Use Dale LD16-01-100J or equivalent.



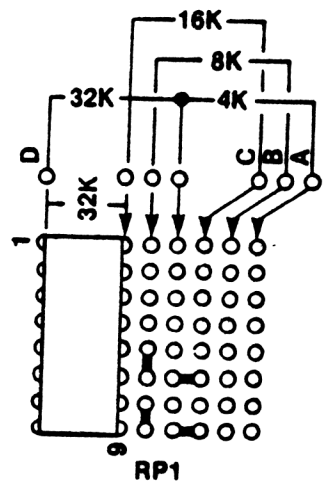
MODULO 4K



MODULO 8K



MODULO 16K



MODULO 32K

Figure C2-5. Sub-Module Memory Banking Resistor-pack Configuration

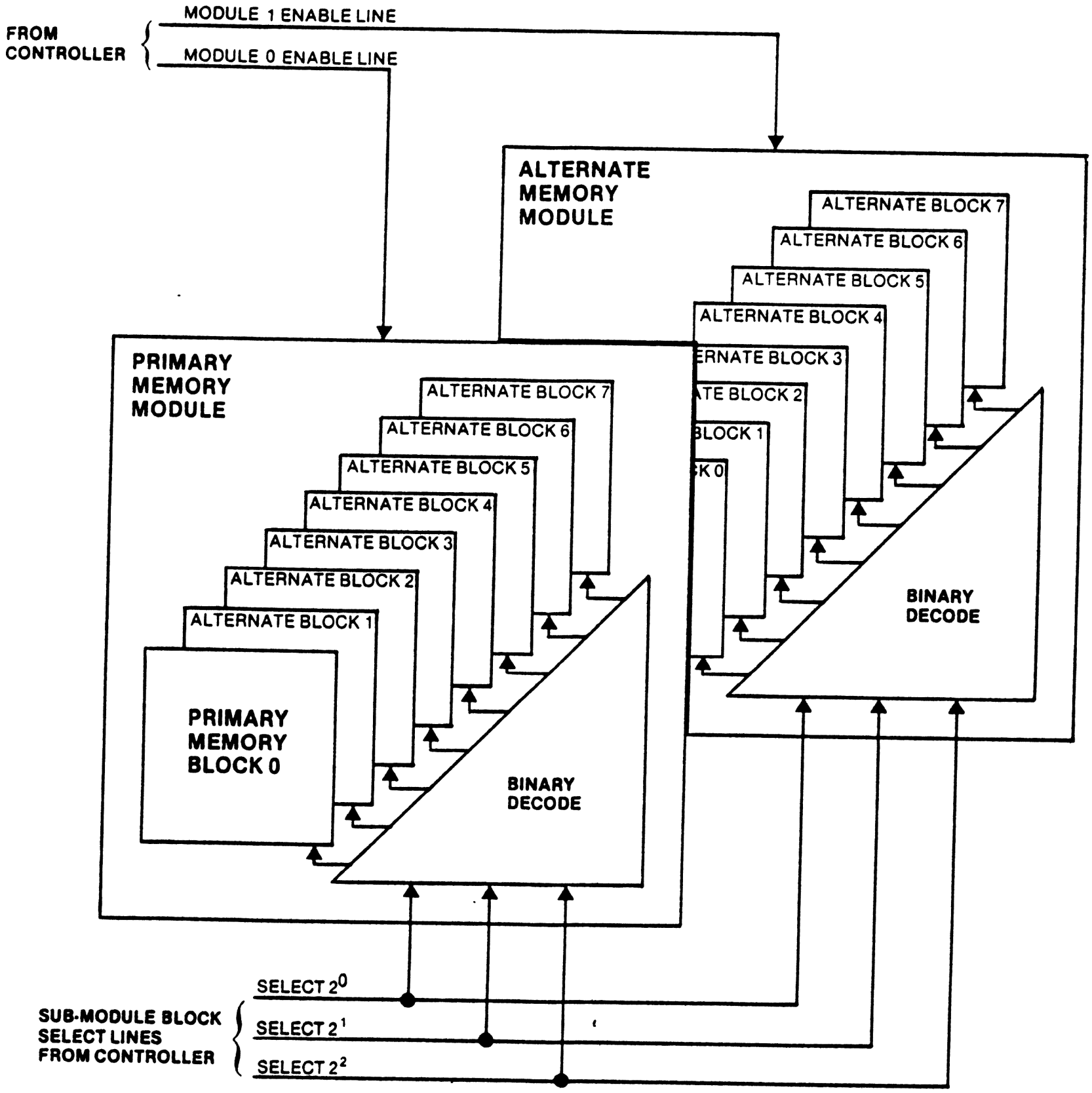


Figure C2-6. Module and Sub-Module Banked Memory Selection

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C2.2.3 Memory Options

C2.2.3.1 Parity

The parity option, which is used where the highest degree of reliability in stored data is required, allows for a single bit of error detection by the memory module. The parity option can be used in two different ways:

- As a normal internally-generated and internally-checked parity
- As an 18 bit memory storing bits from an external source and supplying all 18 bits when read by the same source with no checking

The normal internally-generated and -checked parity method receives the 16 bits of data from the memory controlling source (processor or DMA controller) and internally reads the 16 bits of data, recomputes parity and compares it to the stored parity bits. It supplies only the 16 bits to the controlling device. If an error occurs, the memory is inhibited from responding with MACK.

The external parity selection operates when the EXEC- signal is driven low at the same time as the MST- signal. The memory receives externally generated parity along with the 16 bits of data and stores all the bits like a normal operation.

When reading data from the memory, the EXEC- signal must again be driven low to allow the memory controlling device to read its supplied parity data bits along with the 16 data bits. The memory module does no parity checking in the external mode.

C2.2.3.2 Refresh

The memory board uses cycle stealing refresh which is asynchronous to normal memory operation.

A memory busy flip-flop indicates a memory cycle, either refresh or normal, is underway. If a refresh clock signal occurs while the memory is busy with normal operation, it is stored. At the end of a normal memory cycle the refresh cycle is started. If the memory is not busy with a normal cycle when the refresh clock signal occurs, the refresh cycle is started without delay.

The refresh clock has a period of approximately 25 µsec.

The memory supplies a refresh address and retains the new refresh address for the next refresh cycle.

C2.2.4 Power Fail Sequence

Semiconductor RAM memories are volatile in nature. That is, they can lose data if the supply voltage from the computer drops below a preset "safe" level. For this reason, all NAKED MINI® 4 Family memories that contain semiconductor RAM are equipped with invalid data detection logic. If the voltage being supplied to the board drops below the "safe" level, the invalid data detection indicates whether the integrity of the data has been maintained.

If the supply voltage does drop below this level, the memory disable signal will switch the board to Battery Backup power, if this option is installed (see Part D). If Battery Backup is not present, or has elapsed, the invalid data detection logic will set an internal memory flip-flop, called Invalid Data Detect (IDD).

The IDD flip-flop disables RAM on the board and causes it to respond to any subsequent memory read operation by putting all zeros (no-op instructions) on the data bus.

All NAKED MINI® 4 Family memories are "connected" together by the ALSP- line. If one memory loses RAM power, the IDD flip-flop is set, and the ALSP- line is driven low. Each semiconductor memory in the system receives the AL- line and sets its own IDD flip-flop.

When power returns, the RAM will remain disabled until the IDD flip-flop is reset. This resetting can be accomplised by executing any store instruction. Once IDD is reset, normal operation is resumed.

C2.3 MODEL 53819 FULL-CARD ERROR-CORRECTING SEMICONDUCTOR MEMORY

Computer Automation, Inc., produces a RAM semiconductor memory with error correction, built on a standard full-card. The board is available with 32, 64, or 128K bytes of memory installed. The boards are assigned marketing numbers 53819-16, 53819-32, and 53819-64, respectively. Board level banking can be implemented on all models. Sub-module banking and interleaving features are available on the 53819-32 board. Memory interleaving is available on the 53819-16 board. Sub-module banking is available on the 53819-64 board. All boards are equipped with battery back-up.

C2.3.1 Specifications

MEMORY CYCLE TIMES

The maximum cycle times for read and write operations depend on whether error correction is required. Write operation cycle times also depend on whether the operation is performed in word or byte mode. In addition, all times assume that the operation does not overlap a refresh cycle. The cycle times are as follows:

Read

Access (without correction)	380 ns
(with correction)	495 ns
Overhead (without correction)	140 ns
(with correction)	185 ns
Total (without correction)	520 ns
(with correction)	680 ns
Minimum Interleaved	480 ns

Write (word)

Access	220 ns
Overhead	240 ns
Total	460 ns
Mimimum Interleaved	320 ns

Write (byte)

Access	380 ns
Overhead	350 ns
Total	730 ns
Mimimum Interleaved	480 ns

ENVIRONMENTAL

Operating Temperature Range (Degrees Celsius)	0 to 50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Relative Humidity (Percent, Non-Condensing)	10 to 90

NOTE

Free air flow around the unit is required to provide adequate cooling.

PHYSICAL

Length	42.88 cm (16.88 in.)
Width	38.10 cm (15.00 in.)
Height	1.52 cm (0.6 in.)
Weight	1.1 kg (2.5 lbs.)

ELECTRICAL

Voltage Regulation (All Voltages)	±5 percent
Power Consumption - 53819-64	
+5V Maximum Operating	4.75 A
+12V Standby	1.4 A
+12V Maximum Operating	1.7 A
-12V Maximum Operating	0.04 A
Power Consumption - 53819-32	
+5V Maximum Operating	4.50 A
+12V Standby	1.3 A
+12V Maximum Operating	1.6 A
-12V Maximum Operating	0.04 A
Power Consumption - 53819-16	
+5V Maximum Operating	4.50 A
+12V Standby	1.2 A
+12V Maximum Operating	1.5 A
-12V Maximum Operating	0.04 A

C2.3.2 Functional Description

The Full-Card Error-Correcting Semiconductor Memory consists of the following functional units: memory ICs and associated addressing circuitry; error correction logic; memory refresh circuitry; memory banking and interleaving circuitry; battery back-up circuitry; and MAXI-BUS® Interface logic.

C2.3.2.1 Memory ICs

The memory ICs are 16K x 1 RAMs, 21 RAMs per word, installed to a maximum capacity of 128K bytes. The 21 bit word length includes 16 data bits and 5 error checking bits. Only the 16 data bits are available on the MAXI-BUS® Interface.

C2.3.2.2 Error Correcting Circuitry

The error correcting circuitry generates 5 error check bits from the 16 data bits. A word is stored as 21 bits where the 5 appended bits are error bits E0 through E4. The error correcting algorithm maximizes two bit error detection and minimizes error bit generation and checking delays. The error correcting circuitry can be disabled for test purposes using a switch on the board.

The error check bits are generated at the time that the data word is written into memory. Error checking is performed when the word is read. All single bit errors are detected and corrected. If a single bit error is detected, corrected data is placed on the data bus. Correction of the data written in memory does not take place at this time. Correction is performed instead during a refresh cycle. The circuitry cannot determine the bit locations of double or multiple bit errors. If a multiple bit error is detected a memory configured for operation with NAKED MINI® 4 processors does not acknowledge the access. A memory configured for operation with LSI-2 processors generates a parity error.

Error checking is also carried out when a write operation is performed in byte mode. Before writing the byte, the error correcting circuitry checks the entire word already written in the addressed location for errors. If a single bit error is detected, a correction is made. The new byte is then substituted for the old, and the entire word written back into memory. If a multiple bit error is detected, processors and DMA devices react in the same manner as when a multiple bit error is detected during a word read operation. Because of the checking required, byte mode write operations require longer cycle times than word mode write operations. The cycle time for write operations in byte mode is identical whether or not an error is found.

C2.3.2.3 Memory Refresh and Error Correction

A refresh cycle is performed an average of once every 15 microseconds. In addition, one word of memory is selected and checked for bit errors. Detection of a single bit error extends the refresh cycle to a read/modify/write cycle during which the word is corrected and written back into memory. Detected double bit errors are ignored. An error checking/correcting operation is

performed on each word of memory approximately once a second on the 53819-64 board. On the 53819-32 board the time is 1/2 second and on the 53819-16 board 1/4 second. A detected error pulses a light on the rear of the board. A single bit hard error in one word will therefore pulse the light once every error checking/correcting cycle.

C2.3.2.4 Memory Banking and Interleaving

The memory banking circuitry permits both external and internal memory banking. Memory interleaving can be implemented if installed memory on the 53819 module does not exceed 64K bytes, and total system memory does not exceed 128K bytes. Implementation of these features is described in the Installation Section. Interleaving and internal banking should not be implemented at the same time. Doing so produces undefined operation. Interleaving and external memory banking is permissable.

C2.3.2.5 Battery Back-Up

The Full-Card Error-Correcting Semiconductor Memory has an on-board battery back-up unit that functions automatically in the event power is interrupted. The battery back-up unit has a 7.2 volt battery which can provide enough power to retain data for a minimum of two minutes. Alternatively, the user can attach an external 6V source. Use of the internal or external source is switch selectable on the board.

A green LED lights when power is applied to the board +5V internal line. The source of the power can be the chassis supply or the battery back-up unit. The LED remains lit whenever power is within specifications.

C2.3.2.6 MAXI-BUS® Interface

The MAXI-BUS® Interface contains the memory addressing circuitry, and the data bus transceivers.

C2.3.3 Installation

The Full-Card Error-Correcting Semiconductor Memory is a full-card module, as shown in Figure C2-7. Special installation requirements for the module are described in this subsection.

C2.3.3.1 Module Installation

The source of battery back-up power is selected using Switch 1 (SW1). The switch is set to INT to select the on-board battery and EXT to select an external source. When removing modules from or installing modules in the chassis SW1 should first be set to INT. Ensure that a battery is not connected to the external battery connectors J4 and J5. With any external batteries disconnected, SW1 is set to EXT. Insertion of the board in or removal of the board from the chassis can then be carried out.

CAUTION

Failure to disconnect external backup batteries and/or internal battery backup prior to removing/installing the module in the chassis may result in damage to the module. Chassis power should always be turned off when inserting boards in or removing boards from the system.

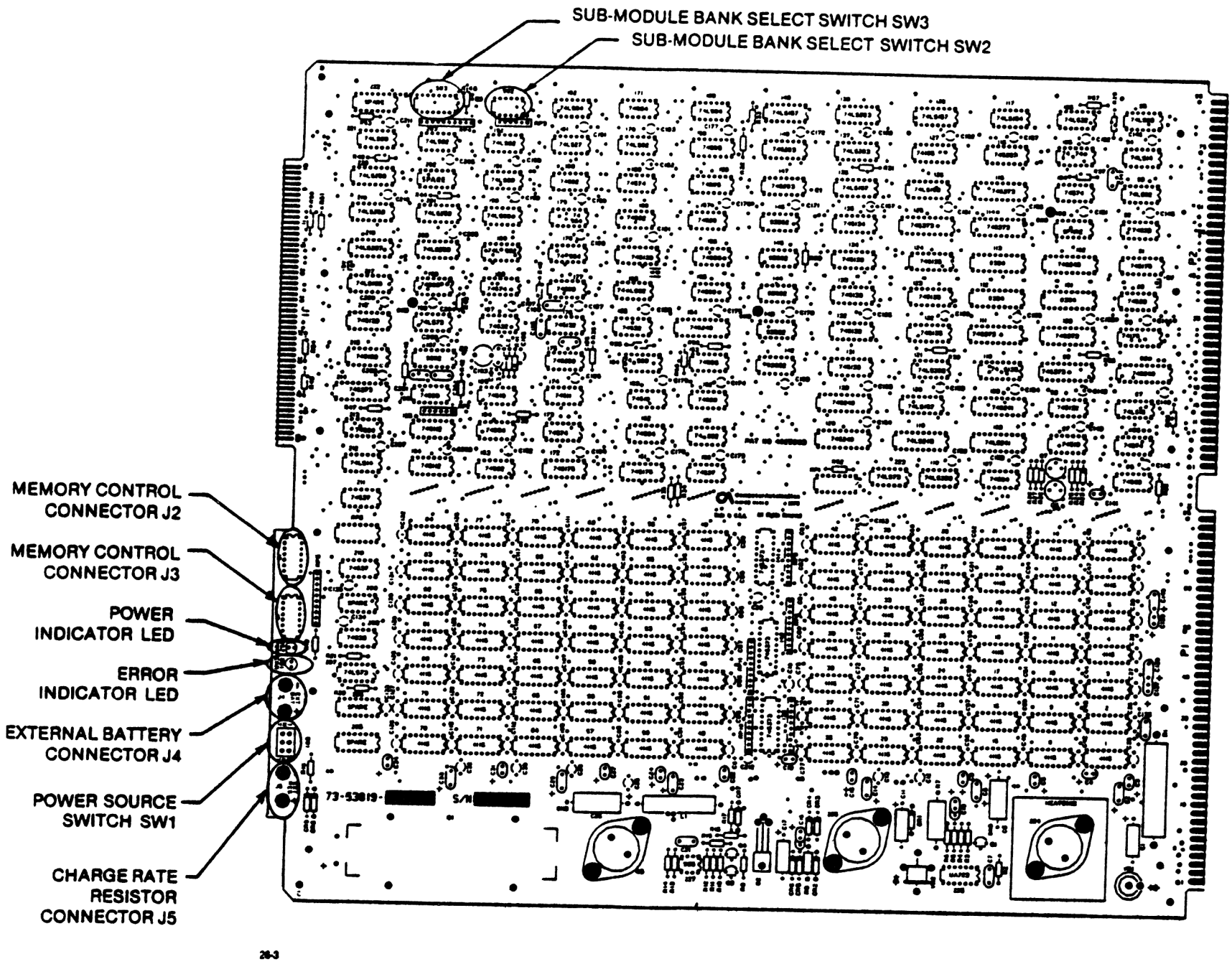


Figure C2-7. Full-Card Error-Correcting Semiconductor Memory Board

C2.3.3.2 Interleaving Procedures

Each memory module in an interleaved pair is assigned either the odd or even addresses for the range of addresses covered by the interleaved pair. Two memory modules of the same size are interleaved with the odd memory address module closest to the processor on the MBIN/MBOT priority chain.

The strapping required for interleaving is made on the memory control connector header, J2. Figure C2-8 shows the strapping pin locations. To select interleaved mode, install a jumper between pins 5 and 12 on each module. One memory module of each interleaved pair of memory modules must be strapped for the odd addresses by installing a second jumper between pins 6 and 11. Use AWG 24 to 28 (Metric Gage 3 to 5) solid wire for the jumpers and solder all connections.

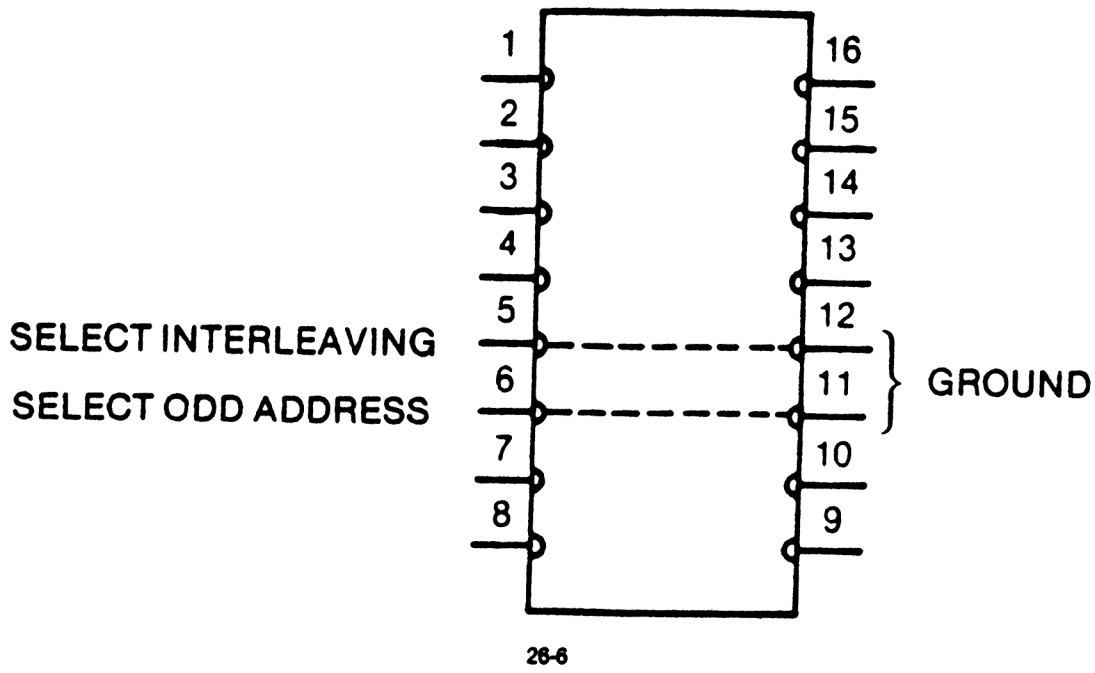


Figure C2-8. Memory Module Interleaving Strapping

C2.3.3.3 Memory Banking Procedures

The 53819-64 memory with 128K bytes of RAM memory is internally constructed as two 64K byte modules. The internal modules are designated A and B. The 53819-32 memory and the 53819-16 memory are depopulated versions of the 53819-64 memory. The 53819-32 memory contains A module memory only. The 53819-16 memory contains half the A module memory. The 53819-64 memory can be strapped as a primary or alternate module. Alternatively, the A module can be designated a primary module and the B module an alternate module. Switch settings on the board make various sub-module banking configurations within the A and B modules possible. The 53819-32 module can be strapped as a primary or alternate module, with switch selected sub-module banking configurations possible within the module. The 53819-16 memory allows board level banking as a primary or alternate module. Sub-module banking is not possible on the 53819-16 board.

C2.3.3.4 Module Memory Banking Strapping

The strapping required for memory banking is made on the memory control connector header(s). The 53819-64 memory uses memory control connectors J2 and J3 to establish primary and alternate modules. If both connectors are strapped identically the board acts as a primary or alternate module, depending on the strapping used. If modules A and B are to act as primary and alternate modules, module A must be strapped as the primary and module B as the alternate. The strapping of connector J2 determines the status of module A. The strapping of J3 determines the status of module B. The 53819-32 board is configured using connector J2 only. The strapping required to establish a module as primary or alternate is shown in Figure C2-9.

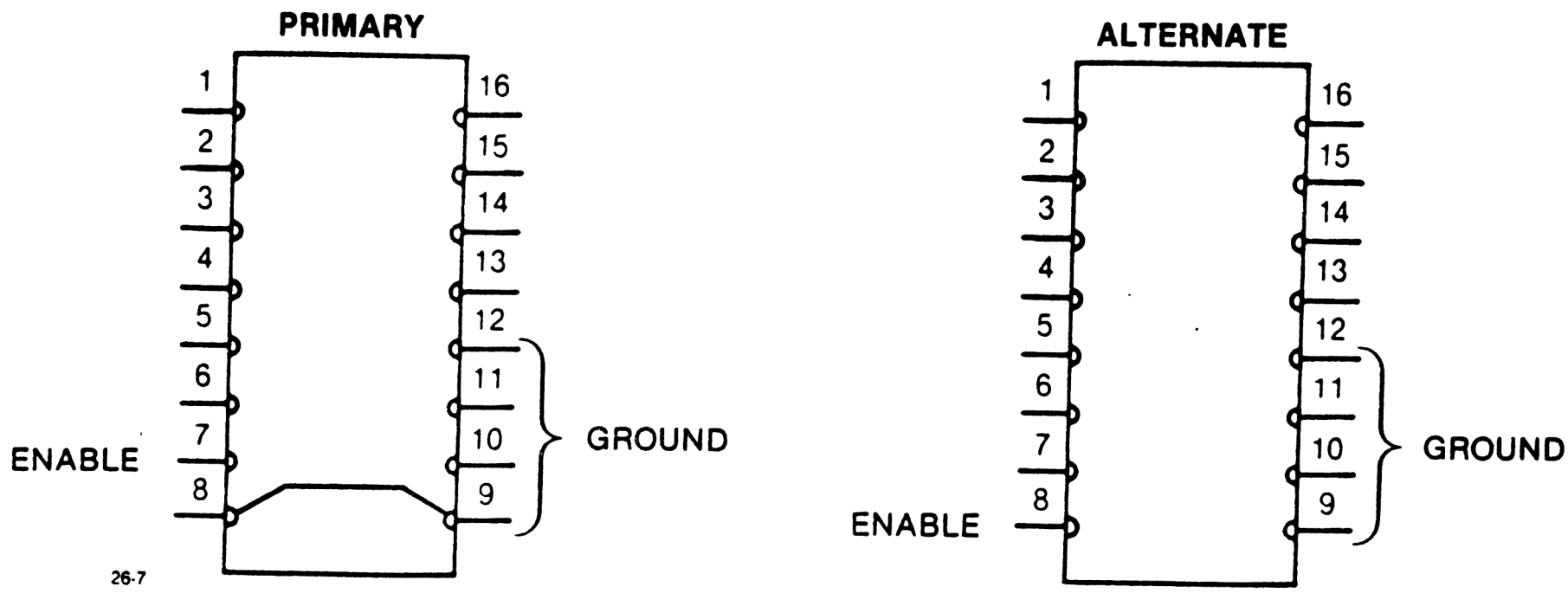


Figure C2-9. Control Cable Connector Wiring

To change from primary to alternate, remove the jumper between pins 8 and 9, and move the enable wire from pin 7 to pin 8.

To change from alternate to primary, move the enable wire from pin 8 to pin 7, and insert a jumper between pins 8 and 9.

Use AWG 24 to 28 (Metric Gauge 3 to 5) solid wire and solder all connections.

C2.3.3.5 Sub-Module Memory Banking

Sub-module banking on the 53819-64 memory is controlled through switches SW2 and SW3. The 53819-32 memory uses SW3 only. The functions controlled by the switch elements on SW3 and SW2 are shown in Figures C2-10 and C2-11, respectively.

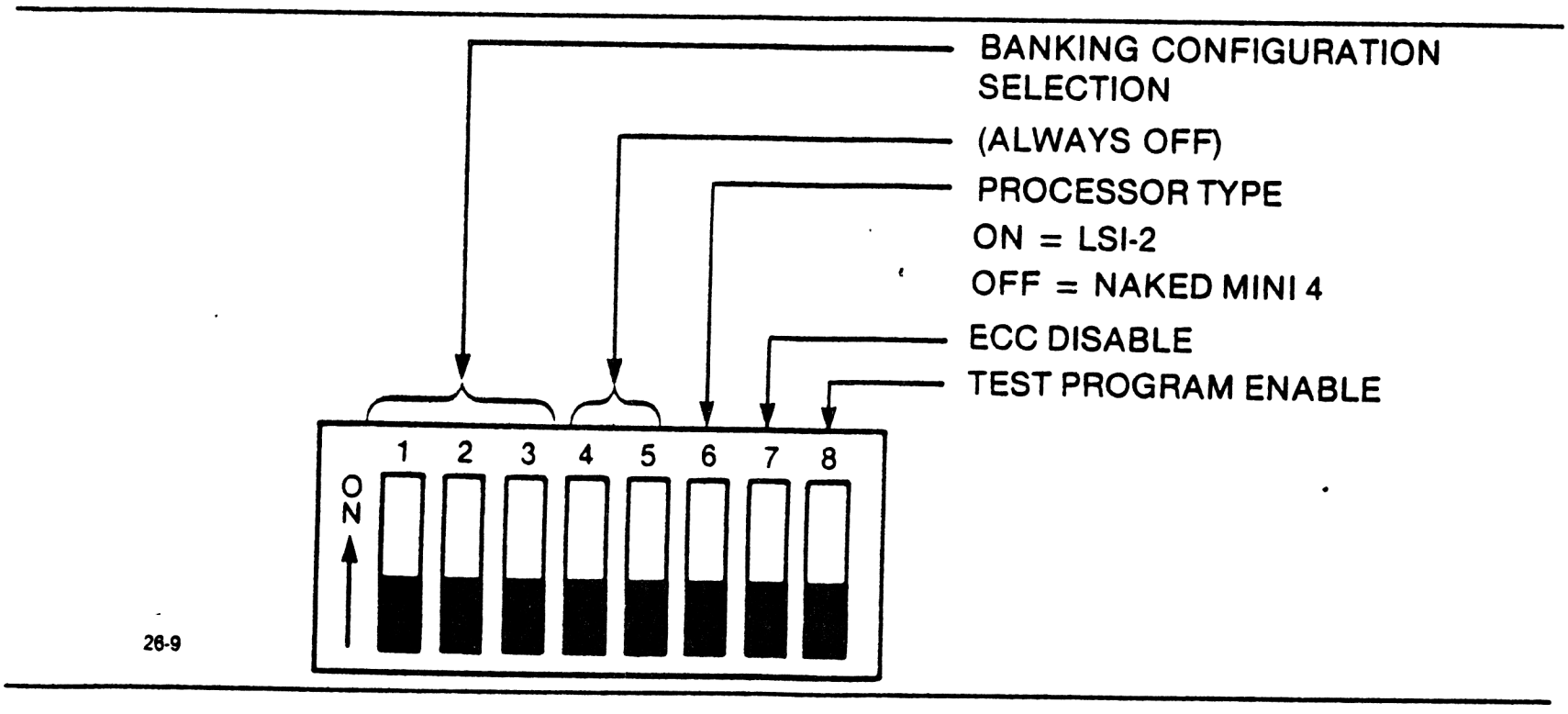


Figure C2-10. SW3, A Module Banking Control Switch Block

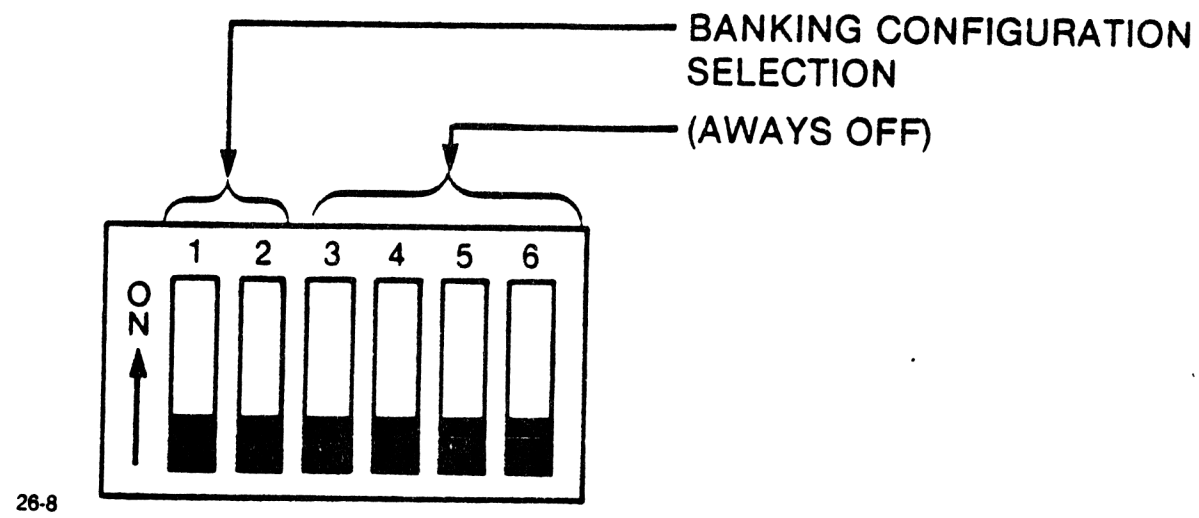


Figure C2-11. SW2, B Module Banking Control Switch Block

Elements 1, 2 and 3 on SW3, and elements 1 and 2 on SW2, are used to control the sub-module banking configurations. The smallest block of addresses that can be selected through sub-module banking is 16K bytes. Sub-module banking configurations are built by designating some 16K byte blocks as primary and others as alternate memory. Only those blocks designated primary add to the total range of addresses allocated. The possible banking configurations for the A and B modules are shown in Figure C2-12. The switch settings required to implement each configuration are shown in Table C2-3. Any combination of switch settings not shown in the table produces undefined results. Configurations A, B, and C can be implemented independently in the A and B modules on the 53819-64 board. Configuration D combines the modules into one configuration. Each configuration adds the amount of address space shown only if the module enable line is asserted. If the enable line is not asserted, all blocks are banked as alternates. When using the D configuration, only the A module enable line is valid. The J2 connector may be strapped as primary or alternate memory. The strapping of the J3 connector is ignored.

Configuration B, when implemented on the A module, requires that switch element SW3-3 be ON. The corresponding element on SW2 is not required to implement this feature on the B module, and should be OFF. Whenever the B configuration is used, the corresponding banking controller connector must have pins 1 and 3 jumpered together (connector J2 for the A module; connector J3 for the B module.)

Other switch elements are used as follows:

Element SW3-6 must be set to correspond with the processor used. The switch is set ON when using an LSI-2 Series processor. The switch is set OFF when using a NAKED MINI® 4 Family processor.

Element SW3-7 is set ON to disable the error correction feature during testing. The element should be OFF during normal operation.

Element SW3-8 is set ON to enable the error correction test features of the test program. The element must be OFF for normal operation.

All other switch elements should be OFF. Setting other elements ON produces undefined results.

Table C2-3. Sub-Module Banking Switch Settings

CONFIGURATION	ADDRESS SPACE SIZE	SW2-1	SW2-2	SW3-1	SW3-2	SW3-3
A	64K bytes	OFF	OFF	OFF	OFF	OFF
B (2x16K)	32K bytes	ON	OFF	ON	OFF	ON
C (4x8K)	16K bytes	OFF	ON	OFF	ON	OFF
D (8x8K)	(See Text)	ON	ON	OFF	ON	OFF

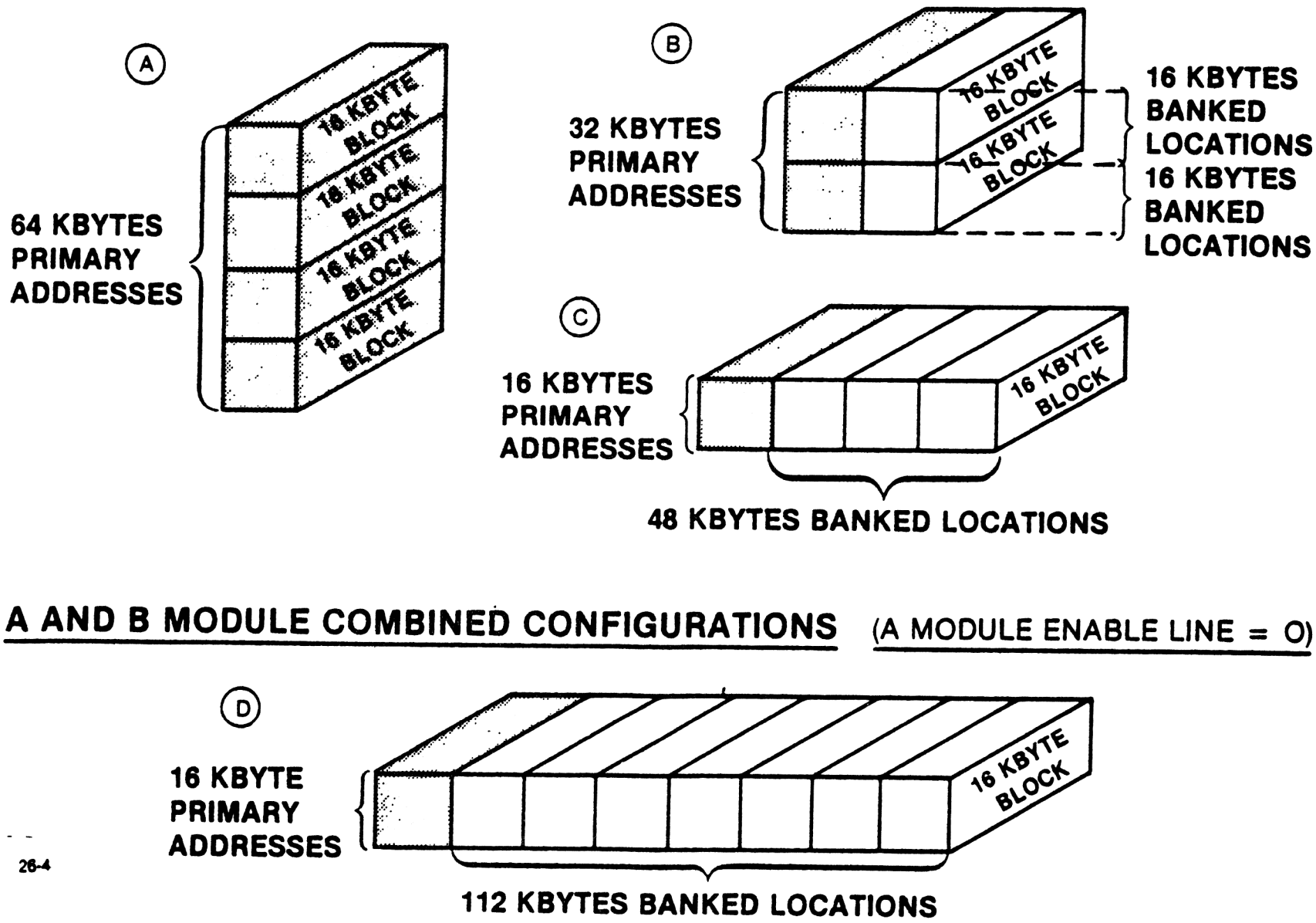


Figure C2-12. A and B Module Banking Configurations

C2.3.3.6 Sub-Module Banking Selection

Individual sub-modules are addressed through the bank select lines wired to the memory bank controller connectors. The J2 controller is used to select between A module sub-modules, and between all sub-modules in the 16K byte x 8 configuration (configuration D). Three bank select lines are used with configuration D. BS15A should not be used in any other configuration. Using BS15A in the A, B, or C configurations will interfere with memory operation. The J3 controller is used to select between B module sub-modules. The location of the bank select lines on the memory banking controller connectors is shown in Figure C2-13. The requirements for adding wires are as follows:

Sub-module Banking Disabled	No Wires
Subdivided into two blocks	1 wire (2^1)
Subdivided into four blocks	2 wires (2^1 and 2^2)
Subdivided into eight blocks	3 wires (2^1, 2^2, and 2^3)

The figures shown in parenthesis are the relative binary values of the data bits used to address the bank select lines.

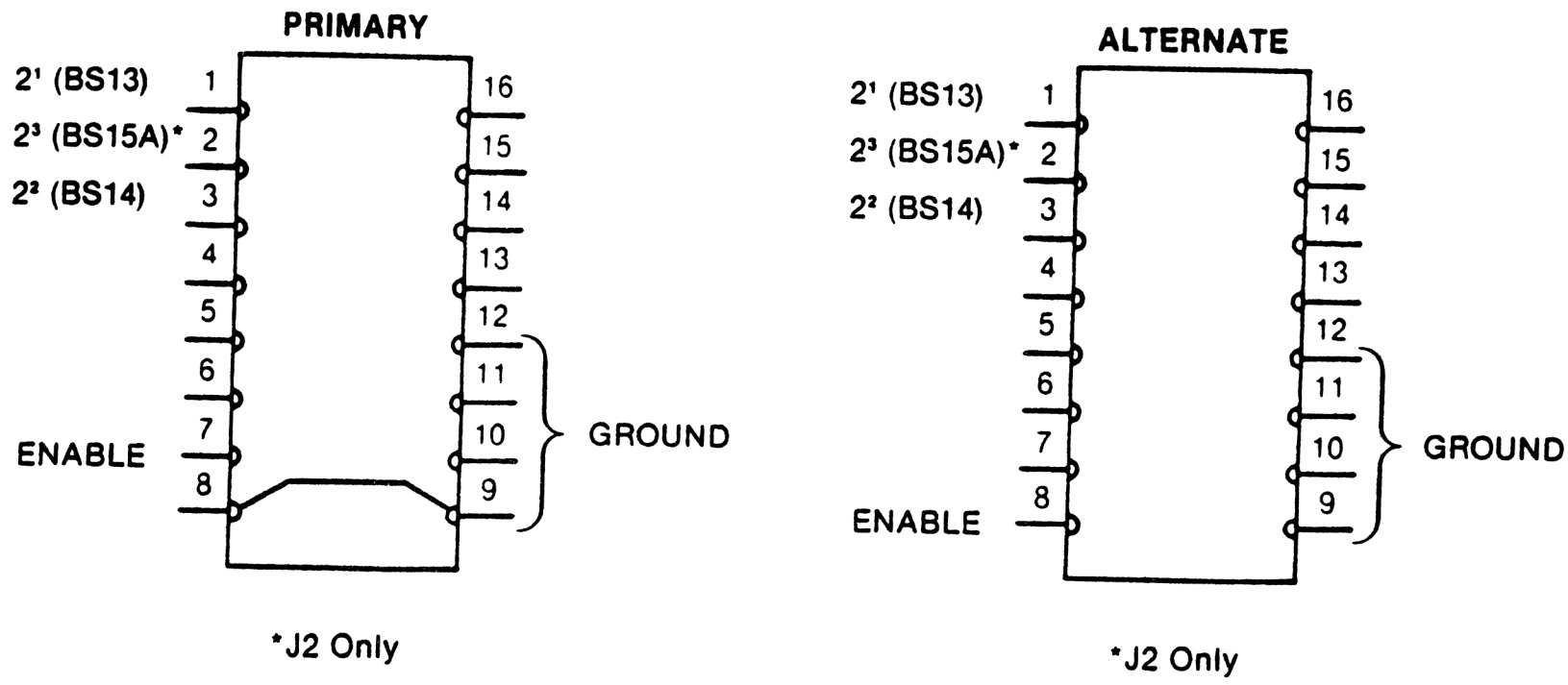


Figure C2-13. Bank Select Lines, Memory Banking Connectors

C2.3.3.7 Module Enables

The state of the module enable signals depends on the inputs to pins 7 and 8 on the memory banking connectors J2 (module A) and J3 (module B). The pins are wired so that the modules are enabled if the pins are unconnected. If the pins are driven by the memory controller, the signals on pin 8 (enable high) and pin 7 (enable low) must not conflict or undefined operation, and possible damage to the memory controller, can occur. The input buffer configurations for the module enable signals are shown in Figure C2-14. The buffers are open collector.

C2.3.4 Power Fail Sequence

Semiconductor RAM memories are volatile in nature. That is, they lose data if the supply voltage from the computer drops below a preset level. For this reason, all NAKED MINI® 4 Family memories that contain semiconductor RAM are equipped with invalid data detection logic. If the voltage supplied to the board drops below the "safe" level, the invalid data detection indicates whether the integrity of the data has been maintained.

If the supply voltage does drop below this level, the memory disable signal will switch the board to Battery Backup power. If Battery Backup is exhausted the invalid data detection logic will set an internal memory flip-flop, called Invalid Data Detect (IDD).

The IDD flip-flop causes the memory to respond to any subsequent memory read operation by putting all zeros (no-op instructions) on the data bus.

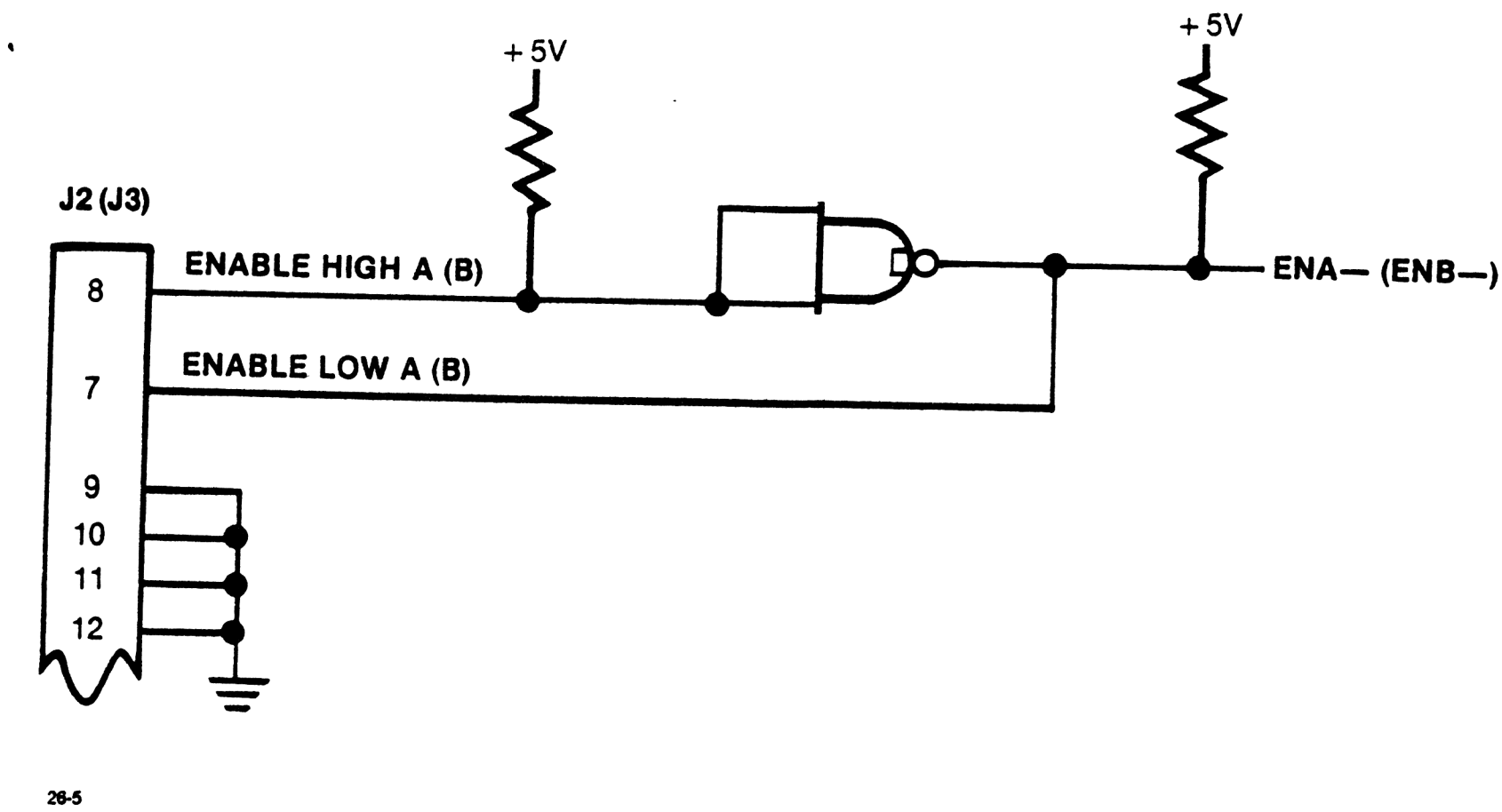


Figure C2-14. Module Enable Signal Logic

All NAKED MINI® 4 Family memories are "connected" together by the ALSP- line. If one memory loses RAM power, the IDD flip-flop is set, and the ALSP- line is driven low. Each semiconductor memory in the system receives the ALSP- line and sets its own IDD flip-flop.

When power returns, memory will continue to return all zeroes until the IDD flip-flop is reset. This resetting can be accomplished by executing any store instruction to an installed memory location in RAM. Once IDD is reset, normal operation is resumed.

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C2.3.5 Test Mode Programming

The 53819 memory board can be placed in a test mode in which the error correcting bits are written independently of the data bits. The test mode is enabled by placing switch element SW3-8 in the ON position. The write error correcting bits only feature is then turned on and off using appropriate select and present instructions. Select and present instructions have the following format:

```
SELP  R,Device Address + Function Code
```

R = the A, Q, X, or Y register. The device address has an absolute value of 1 and the function code a value of 0. In machine language the device address and function code occupy the lower byte of the instruction word. The function code occupies the three least significant bits and the device address the upper five. Consequently, an absolute device address value of 1 means setting bit three of the instruction word. To establish the correct value, the following assembly language statements can be used.

```
ADBAS  EQU  1
ADFNL  EQU  ADBAS%3
```

The first statement equates the mnemonic ADBAS to the value 1. The second statement equates the mnemonic ADFNL to ADBAS shifted left three places. The select and present instruction then takes the form

```
SELP  R,ADFNL
```

Alternatively, the statement

```
SELP  R,8
```

can be used. It is important to note that the device address 1 is not a dedicated address. Any device in the system that responds to a select and present instruction and is assigned device address 1 responds to the instruction shown. For this reason caution must be exercised to avoid a conflict between two identically addressed devices.

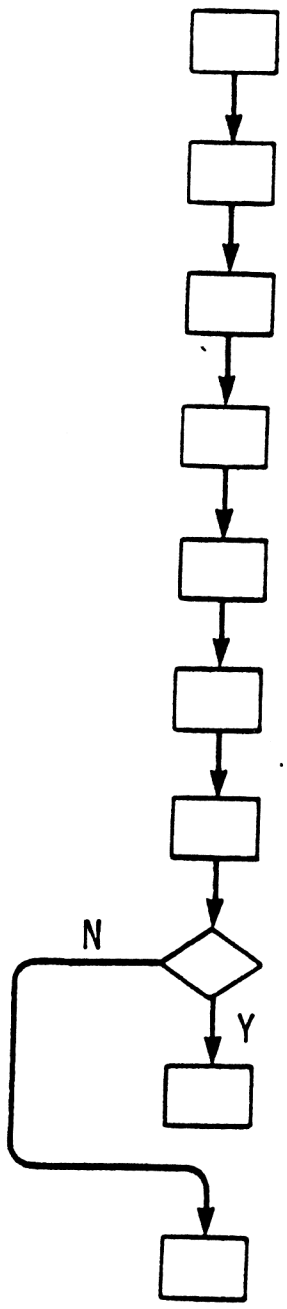
The write error correction bits only function is turned on by setting the most significant bit of the selected register to 1 and outputting it using the select and present instruction shown. The function is turned off by resetting the register bit to 0 and outputting it with the same instruction.

C2.3.6 Error Correction Circuitry Testing

The proper functioning of the error correction test circuitry can be tested in two ways. By turning on the write error correction bits only function, the error correction bits can be changed to correspond to a value one bit different than actually stored at a given location. A read operation should cause the data to be "corrected" to the value indicated by the error bits. Syndrome codes can also be used to generate specific error correction bit values. When the error bits are written with a syndrome code, a read operation should cause the error bits to be corrected to correspond with the value of the data word at that memory location. A flowchart of the first procedure is shown in Figure C2-15. A flowchart of the second procedure is shown in Figure C2-16. The syndrome codes are given in Table C2-4. The procedure shown in Figure C2-16 "walks" a bit across the error correcting bits. Combinations of error bit settings can be generated by exclusive ORing of the codes.

Table C2-4. Error Correction Bit Syndrome Codes

Error Correction Bit	Syndrome Code
0	:70
1	:0E
2	:0D
3	:0B
4	:07



Enable write error correction bits only function (switch SW3-8 on).

Turn function off with select and present instruction (selected register DB15=0).

Write selected memory location with data pattern :0000.

Turn function on with select and present instruction (selected register DB15=1).

Write selected memory location with data pattern :0000

Turn function off with select and present instruction (selected register DB15=0).

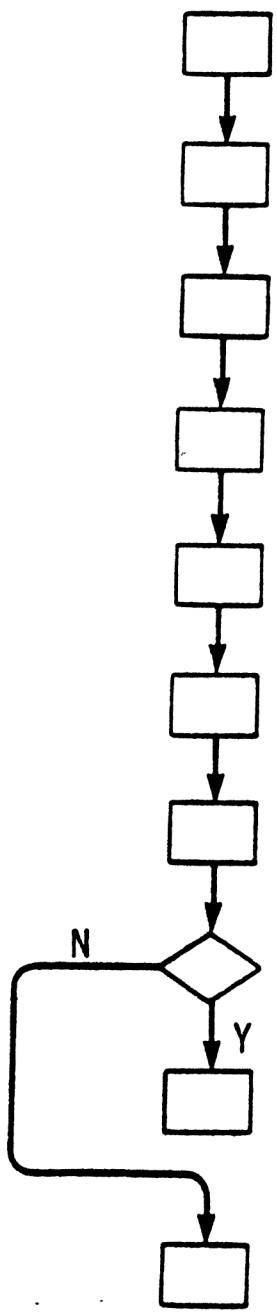
Read selected memory location?

Does the data pattern read :0000?

Write selected memory location with next data pattern .

Error correcting circuit failure indicated.

Figure C2-15. Error Circuitry Checking Through Data Pattern Correction



Enable write error correction bits only function (switch SW3-8 on).

Turn function off with select and present instruction (selected register DB15=0).

Write selected memory location with data pattern :0000

Turn function on with select and present instruction (selected register DB15=1).

Write selected memory location with syndrome code :70

Turn function off with select and present instruction (selected register DB15=0).

Read selected memory location?

Does the data pattern read :0000?

Write selected memory location with next data pattern.

Error correcting circuit failure indicated.

Figure C2-16. Error Correction Circuitry Syndrome Test

C2.4 MODEL 53828 FULL-CARD SEMICONDUCTOR MEMORY WITH 22-BIT ADDRESSING

Computer Automation, Inc., produces a RAM semiconductor memory with error correction and 22-bit addressing, designed for use in a chassis with a memory management unit. The memory is built on a standard full-card and is available with 128K bytes or 256K bytes installed. The boards are assigned marketing numbers 53828-01 and 53828-02, respectively. Each memory board module is equipped with a 4-word micro-cache, which significantly improves memory response times.

C2.4.1 Specifications

MEMORY CYCLE TIMES

The maximum cycle times for read and write operations depend on whether error correction is required and whether the word is found in the micro-cache. Write operation cycle times also depend on whether the operation is performed in word or byte mode. In addition, all times assume that the operation does not overlap a refresh cycle. The cycle times are as follows:

Read	From Memory	From Micro-Cache
Access (without correction)	370 ns	70 ns
(with correction)	510 ns	115 ns
Overhead (without correction)	185 ns*	185 ns*
(with correction)	185 ns*	185 ns*
Total (without correction)	555 ns	255
(with correction)	695 ns	300

* = limited by system factors external to memory

Write (word)	
Access (without correction)	55 ns
Overhead (without correction)	380 ns
Total (without correction)	435 ns

Write (byte)	
Access (without correction)	435 ns
Overhead (without correction)	270 ns
Total (without correction)	705 ns

ENVIRONMENTAL

Operating Temperature (Degrees Celsius)	0 - 50
Non-Operating Temperature Range (Degrees Celsius)	-40 to +80
Humidity (Percent Non-condensing)	10 - 90

NOTE

Free air flow around the unit is required to provide adequate cooling

PHYSICAL

Length	42.88 cm	(16.88 in.)
Width	38.10 cm	(15.00 in.)
Height	1.52 cm	(0.6 in.)
Weight	1.1 kg	(2.5 lbs.)

ELECTRICAL

Voltage Regulation (All Voltages)	±5 percent
Power Consumption - 53828-01	
+5V Maximum Operating	7.5 A
+12V Standby	0.15 A (IDLE)
+12V Maximum Operating	0.55 A (ACTIVE)
-12V Maximum Operating	0.25 A
Power Consumption - 53828-02	
+5V Maximum Operating	7.5 A
+12V Standby	0.3 A
+12V Maximum Operating	1.1 A
-12V Maximum Operating	0.5 A

C2.4.2 Functional Description

The Model 53828 memory module consists of the following functional units: memory ICs and associated addressing circuitry; error correction logic; memory refresh circuitry; micro-cache; and MAXI-BUS® Interface logic.

C2.4.2.1 Memory ICs

The memory ICs are 16K x 1 RAMs, 21 RAMs per word, installed to a maximum capacity of 128K. The 21 bit word length includes 16 data bits and 5 error checking bits. Addressing circuitry is provided to allow 256K byte addressibility. The 16 data bits are available on the MAXI-BUS® Interface. NAKED MINI® 4/Series 5 processors can read or write the error correcting bits for test purposes. The procedure is described in the NAKED MINI® 4/Series 5 Principals of Operation Manual, 53817-91.

C2.4.2.2 ECC Circuitry

The error correcting circuitry generates 5 error check bits from the 16 data bits. A word is stored as 21 bits where the 5 appended bits are error bits E0 through E4. The error correcting algorithm maximizes two bit error detection and minimizes error bit generation and checking delays. The error correcting circuitry can be disabled for test purposes using a switch on the board.

The error check bits are generated at the time that the data word is written into memory. Error checking is performed when the word is read. All single bit errors are detected and corrected. If a single bit error is detected, corrected data is placed on the data bus. Correction of the data written in memory does not take place at this time. Correction is performed instead during a refresh cycle. The circuitry cannot determine the bit locations of double or multiple bit errors. If a multiple bit error is detected a memory configured for operation with NAKED MINI® 4 processors does not acknowledge the access. A memory configured for operation with LSI-2 processors generates a parity error.

Error checking is also carried out when a write operation is performed in byte mode. Before writing the byte, the error correcting circuitry checks the entire word already written in the addressed location for errors. If a single bit error is detected, a correction is made. The new byte is then substituted for the old, and the entire word written back into memory. If a multiple bit error is detected, processors and DMA devices react in the same manner as when a multiple bit error is detected during a word write operation. Because of the checking required, byte mode write operations require longer cycle times than word mode write operations. The cycle time for write operations in byte mode is identical whether or not an error is found.

C2.4.2.3 Memory Refresh and Error Correction

A refresh cycle is performed an average of once every 15 microseconds. In addition, one word of memory is selected and checked for a bit errors. Detection of a single bit error extends the refresh cycle to a read/modify/write cycle during which the word is corrected and written back into memory. Detected double bit errors are not corrected. An error checking/correcting operation is performed on each word of memory approximately once every two seconds on the 53828-02 board, and once every second on the 53828-01 board. A detected error pulses a light at the rear of board. A single bit hard error in one word will therefore pulse the light once every error checking/correcting cycle.

C2.4.2.4 Micro-Cache

A four word, parallel loaded micro-cache is provided for each memory board. The micro-cache contains four words of data read from memory during a read operation in which the requested data word was determined to be within the memory module but not contained within the four word micro-cache. When updated the micro-cache is loaded with the contents of four sequential memory locations, the two least significant bits of the address being ignored. For example, if memory access is requested at location :FC9C, and :FC9C is not one of the four words already loaded in the micro-cache, the micro-cache is loaded with the contents of memory location :FC9C, :FC9D, :FC9E, and :FC9F. The micro-cache provides increased access speeds for approximately 35 percent of all memory read cycles not cached by the memory management unit in the split chassis. Writing to a micro-cache location, byte writes to any on-board location, and any on-board refresh cycle, cause the micro-cache to be marked as invalid and require a read to update the micro-cache.

C2.4.2.5 MAXI-BUS® Interface

The MAXI-BUS® Interface contains the memory addressing ciruitry, and the data bus drivers and receiver. Because the 53828 memory board has 22 address lines, it can be installed only in chassis that have a memory management unit, i.e., the S9 and S17 chassis.

C3 RANDOM ACCESS HALF-CARD SEMICONDUCTOR MODULES

C3.1 INTRODUCTION

Computer Automation, Inc. produces two full-card semiconductor RAM memory modules designed for interface with all NAKED MINI® 4 Family computers. The modules are designated 11642 and 53775 and are described in subsections C3.2 and C3.3, respectively.

C3.2 MODEL 11642 HALF-CARD SEMICONDUCTOR MEMORY MODULE

Computer Automation, Inc., produces a half-card random access (RAM) read/write memory module. This half-card RAM memory is available in both a 4K module (Model 11642-14) and an 8K module (Model 11642-18). Both half-card modules are designed for interface with all NAKED MINI® 4 Family computers.

Memory features include Refresh and Automatic Start-up. Automatic Start-up initiates a power-up service routine. An optional AutoLoad Read-only Memory or customer AutoLoad program can be used. The AutoLoad program must be stored in the lowest read-only memory location in the system; when RAM is disabled, the processor will "bubble" through RAM to the first location of any read-only memory installed in the system. This location will contain the first instruction of the AutoLoad program. RAM is enabled after any write operation occurs.

The half-card RAM modules are volatile in nature. That is, they can lose data if the power supply is interrupted or drops below a "safe" level. The Battery Pack, Model 12048-01, can be installed in a half-card chassis to provide a minimum of two minutes of data retention for one or two half-card RAM modules. The Battery Pack is detailed in Section D3.

The half-card RAM modules can be installed in either a half-card or a full-card chassis. If the half-card RAM module is to be installed in a half-card chassis, no special installation requirements are necessary. If the half-card RAM module is to be installed in a full-card chassis, the module must first be joined with a half-card processor, an I/O controller, a filler card, or another half-card processor and propagation requirements of the MBIN/MBOT chain must be observed. Refer to the Chassis Configuration Reference Manual and Installation Guide, 21426-91 for information on the joining of half-cards.

The joining of a half-card memory with another half-card module requires modification of the motherboard if an expansion chassis is used. Refer to the appropriate computer reference manual if motherboard modifications are required.

C3.2.1 Specifications

MEMORY CYCLE TIMES

A minimum cycle time occurs if a cycle-stealing refresh signal is sent at the end of a normal memory cycle. A "worst-case" or maximum-cycle time occurs if a refresh signal is sent at the beginning of a normal access cycle time. Since refresh cycle time is equal to normal memory cycle time, the maximum cycle time is equal to double the total minimum cycle time.

The minimum cycle times are as follows:

Read

Access Interval	540 ns
Overhead Interval	300 ns
Total	840 ns

Write

Access Interval	390 ns
Overhead Interval	450 ns
Total	840 ns

ENVIRONMENTAL

Operating Temperature Range (Degrees Celcius)	0 to +50
Non-operating Temperature Range (Degrees Celcius)	-30 to +90
Relative Humidity (Percent, Non-condensing)	0 to 95

NOTE

Free air flow around the unit is required to provide adequate cooling.

PHYSICAL

4K Half-Card - Model 11642-14

Length	42.88 cm. (16.88 in.)
Width	19.05 cm. (7.5 in.)
Height	1.52 cm. (0.6 in.)
Weight	1.35 kg. (3 lb.)

8K Half-Card - Model 11642-18

Length	42.88 cm. (16.88 in.)
Width	38.10 cm. (15.0 in.)
Height	1.52 cm. (0.6 in.)
Weight	1.8 kg. (4 lb.)

ELECTRICAL

Voltage Regulation (All Voltages)	±5%
Power Consumption - 4K Half-Card	
+12Vdc Maximum Operating	1.4 A
-12Vdc Maximum Operating	461 mA
+5Vdc Maximum Operating	18 mA

Power Consumption - 8K Half-Card

+12Vdc Maximum Operating	1.16 A
-12Vdc Maximum Operating	479 mA
+5Vdc Maximum Operating	18 mA

C3.3 MODEL 53775 RANDOM ACCESS SEMICONDUCTOR MEMORY MODULE

Computer Automation, Inc., produces 16K, 32K, and 64K random access (RAM) semiconductor read/write memory modules on a standard half-card. The models available are listed in Table C3-1.

These cards feature CPU-transparent refresh, and are designed to work with the power-up features of the NAKED MINI® 4 processors. In the event of a power failure where memory integrity is lost, the RAM card presents NOP instructions (:0000) to the CPU, thereby forcing it to "bubble up" to the first non-ram location in memory above the card. This location, then, should contain the restart sequence. However, on a 64K RAM system, the CPU would continue to cycle through NOPs, until the outside world stopped it. The RAM is enabled by a write to the module.

C3.3.1 Specifications

MEMORY CYCLE TIMES

A minimum cycle time occurs if a cycle-stealing refresh cycle is started at the end of a normal memory cycle. A "worst-case" or maximum-cycle time occurs if a refresh cycle is started at the beginning of a normal cycle time. Since refresh cycle time is equal to normal memory cycle time, the maximum cycle time is equal to double the total minimum cycle time.

The minimum cycle times are as follows:

Access Interval	470 ns
Overhead Interval	110 ns
Cycle Time	580 ns

ENVIRONMENTAL

Operating Temperature Range (Degrees Celcius)	0 to +50
Non-operating Temperature Range (Degrees Celcius)	-30 to +90
Relative Humidity (Percent, Non-condensing)	5 to 90

NOTE

At least 200 linear feet per minute of free air flow around the unit is required to provide adequate cooling.

PHYSICAL

Length	42.88 cm (16.88in.)
Width	19.05 cm (7.5 in.)

Table C3-1. Model Identification

MODEL	DESCRIPTION
53775-16	32K Byte RAM with Battery Backup
53775-32	64K Byte RAM with Battery Backup
53775-64	128K Byte RAM with Battery Backup

ELECTRICAL

Voltage Regulation (All Voltages)	±5%
Power Consumption with BBU	
+12Vdc Operating	1.2 A
Standby	1.0 A
-12Vdc Operating	0.1 A
Standby	0.1 A
+5Vdc Operating	1.6 A
Standby	1.6 A
Power Consumption without BBU	
+12Vdc Operating	0.5 A
Standby	0.1 A
-12Vdc Operating	0.1 A
Standby	0.1 A
+5Vdc Operating	0.8 A
Standby	0.8 A

C3.3.2 Installation

Prior to removing or installing a module, it is essential to remove all power from the system. After powering down, any battery backup must be removed. Set the battery select switch, INT/EXT, S1, to INT. Then remove all battery connectors from the external battery connectors, P3 and P4. Then switch the select switch to the EXT position.

CAUTION

Failure to disconnect battery backup power from a RAM module will result in damage to it.

The RAM memory board has on-board MOS memory devices that are sensitive to static electricity. Caution should be used when handling or installing the module to insure the highest degree of reliability.

These modules are half-card modules, and can be installed in either half-card or full card chassis. If it is to be installed in a half-card chassis, no special preparation is needed for that purpose. However, for installation in a full card chassis, the module must first be joined with another half-card, such as another memory module or a half-card processor card and propagation requirements of the MBIN/MBOT chain must be observed. Refer to the Chassis Configuration Reference Manual and Installation Guide, 21426-91, for information on the joining of half-cards.

PART D

BATTERY BACKUP

SECTION D1 INTRODUCTION

SECTION D2 FUNCTIONAL DESCRIPTION

D2.1 TYPES OF SEMICONDUCTOR MEMORIES

D2.2 BATTERIES

D2.3 CHARGING METHODS

D2.3.1 Charging Nickel-Cadmium Batteries
D2.3.2 Charging Lead-Acid Batteries
D2.3.3 Undervoltage Protection

D2.4 BATTERY EXAMPLES

SECTION D3 BATTERY PACK - MODEL 12048-01

D3.1 INTRODUCTION

D3.2 MECHANICAL DESCRIPTION

D3.3 EXTERNAL BATTERY BACKUP

SECTION D4 ON-CARD BATTERY BACKUP

SECTION D5 EXTERNAL EXPANSION

D5.1 FUNCTIONAL DESCRIPTION

D5.2 EXTERNAL EXPANSION SPECIFICATIONS

D5.3 CHARGERS FOR EXTERNAL BATTERIES

D5.3.1 Internal Charger
D5.3.2 External Chargers

D5.4 OTHER CONFIGURATIONS

SECTION D6 OPERATING NOTES AND CAUTIONS

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D1 INTRODUCTION

Semiconductor memories are volatile by nature, and may lose stored data if primary power is interrupted. To guard against such losses, Computer Automation, Inc., offers an option called Battery Backup. Battery Backup supplies a continuation of power to its associated memory module(s) during interruptions, providing data retention for a minimum of two minutes.

Battery Backup is available in two different forms: On-board Battery Backup (in which the backup battery is mounted on the memory module) and the Battery Pack option (in which the backup battery is mounted in a half-card chassis power supply). Both options permit a user-supplied battery to be added to extend the data retention capability beyond the minimum two minutes supplied by the on-board battery. Table D1-1 shows the memory modules that include on-board Battery Backup.

The Battery Pack option, Model 12048-01, is used with the random access half-card memory module, Model 11642-XX.

The Battery Backup option, Model 53686-02, is used for the LSI 4/10 on-board RAM memory. Refer to the LSI 4/10 Computer Reference Manual for more information on this Battery Backup option.

D2 FUNCTIONAL DESCRIPTION

The Computer Automation, Inc., Battery Backup option increases data integrity of semiconductor memories with the use of a wide range of batteries and charge rates.

D2.1 TYPES OF SEMICONDUCTOR MEMORIES

Semiconductor memories are available in both static and dynamic MOS; each type requires different battery backup considerations. Static memories normally require a single voltage source for memory retention, whereas dynamic memories are more complex and require up to three different voltages (generally, ±5Vdc and +12Vdc) to operate their timing, logic, and refresh circuitry. However, Computer Automation, Inc., provides a DC-to-DC converter and regulator as a part of the basic Backup option which is effectively used to simplify the number and types of batteries required. Using this technique, a single common 6-volt battery can be used to supply the multiple voltage and current requirements.

Table D1-1. Memories With On-Card Battery Backup

MEMORY TYPE	MODEL NUMBER
RAM Memories, 700 nsec Full-Card	11601-XX (without Parity), or 11611-XX (with Parity)
RAM Memories, 580 nsec Half-Card	53775-XX
RAM Memories, 550 nsec Full-Card	11701-XX (without Parity), or 11711-XX (with Parity)
RAM/ROM/EPROM Memories, Half-Card	53678-XX (except 53678-00)
RAM Memory With Error Correction	53819-XX

Typical backup power required for an 8K by 16-bit dynamic memory module is approximately 5 watts, while an equivalent static memory module requires four times as much power.

D2.2 BATTERIES

The most common types of commercially available batteries are Alkaline, Manganese, Mercuric Oxide, Zinc Air, Silver Zinc, Lead-Acid and Nickel-Cadmium. Lead-Acid and Nickel-Cadmium are most commonly used in uninterruptible power systems.

Standard commercial Lead-Acid batteries are rechargable and are currently available in sealed and unsealed configurations, with expected battery life times of 3 to 5 years. Batteries can be obtained from many battery manufacturers, including Gates, Gould, Globe, Eagle, and Prichard. The most popular of these batteries is the sealed gelled electrolyte type, which does not require routine maintenance of adding liquid or checking liquid levels. These batteries are very small and compact and usually can be mounted in tilted or inverted positions.

WARNING

Most Lead-Acid batteries are temperature tolerant and generally exceed the environmental requirements of the computer system; however, adequate ventilation must be considered for unsealed batteries during fast charging utilization, since hydrogen and oxygen gases sometimes are released and could cause an explosion if a spark is introduced.

Nickel-Cadmium batteries also are useful where longer life is required. These batteries generally are smaller in size, have a battery life of 9 to 12 years, are maintenance free, emit no gas during operation, and can be operated in any position without affecting performance. Computer Automation, Inc., Battery Backup products use Nickel-Cadmium batteries rated at a temperature of 50 C rather than the more common 40 C rating.

Six volts is a popular, economical, readily obtained battery voltage, and is used in most semiconductor battery backup applications. Full environmental and application data for batteries can be obtained from most battery manufacturers.

Since batteries should be recharged after use, a small commercial charger is also recommended.

D2.3 CHARGING METHODS

A variety of charge methods are capable of effectively charging Lead-Acid or Nickel-Cadmium batteries. These methods all accomplish the same end: putting enough energy into the battery to provide the required amount of discharge energy. The methods differ in the time it takes to accomplish the task, the complexity of circuitry used, and the techniques used to provide the charging function in a safe and reliable manner.

This section discusses methods for charging Nickel-Cadmium and Lead-Acid batteries.

D2.3.1 Charging Nickel-Cadmium Batteries

The maximum charge current which may be used in the constant-current charge method is determined by the cell overcharge capability. This charge current level is typically some fraction of the nominal capacity of the cell. Standard Nickel-Cadminum sealed cells can tolerate 0.1C (C is defined as the battery amp/hour rating) overcharge for extended periods of time without damage or serious performance deterioration. Special batteries with higher overcharge current capability are also available, but the 0.1C overcharge capability is standard, most economical, and most often used.

Charging at the 0.1C rate--which is a slow charge rate often referred to as "overnight charging"--requires approximately 10 to 14 hours to restore a full charge in Nickel-Cadmium batteries. Although slow, the 0.1C charge rate has the following advantages:

- It permits the use of smaller, generally more economical, chargers than those for higher charge rates.
- It permits the use of the least expensive batteries.
- It minimizes cell temperature rise and internal pressure during charging.

The charging rate is usually 0.1C whenever 10 hours of recharging time is available for full recharge of the battery. Chargers designed for slow rate charging are the simplest and least expensive of all Nickel-Cadmium battery chargers. See Table D2-1 for battery charging methods and rates.

Table D2-1. Nickel-Cadmium Rates for Charging and Discharging

CHARGING METHODS	CHARGE RATE	
	CURRENT RATE	HOUR RATES
Trickle	0.01 C	100-hour
	0.02 C	50-hour
	0.03 C	33-hour
Slow	0.04 C	25-hour
	0.05 C	20-hour
	0.06 C	17-hour
	0.07 C	14-hour
	0.10 C	10-hour
Quick	0.20 C	5-hour
	0.50 C	2-hour
Fast	1 C	1-hour
	2 C	30-minutes
	3 C	20-minutes

The Computer Automation, Inc., On-card Battery Backup options use a slow 0.1C constant current diode and resistor charger circuit. (See Figure D2-1.) To determine the proper charge rate, divide by 10 the current drain rate that will discharge the battery in one hour. This type of slow charger normally can be left connected for long periods of time without damaging the battery.

Many user applications require three or more partial or full discharges per day. Such applications, obviously, cannot accept a recharge time of 10 hours. Recharge time can be decreased by using batteries with three or more times the capacity (amp/hour) required for the particular memory. However, the added battery size and cost may be unsuitable for all applications, and a quick or fast charge can be a better solution. A quick charge usually is defined as charging a battery in two to five hours at a charge rate of 0.2C to 0.5C. This charge rate is ideal for applications requiring many partial or complete discharges per day. A fast charge can be defined as charging a battery at a rate of 0.5C or greater. When using fast charging techniques, it is necessary to terminate the high charge rate before the battery goes into excessive overcharge.

Quick or fast charging circuits are possible with a split-rate approach. Split-rate charging is a technique where the battery is charged initially at a fast rate. Then, at the appropriate time--generally when the battery goes into overcharge--the charging is switched to a low or trickle rate.

The term "trickle rate" identifies a standby rate, approximately 0.01C to 0.03C, which is just high enough to keep a charged battery fully charged, and low enough that the battery can withstand being charged at this rate indefinitely. However, the trickle rate is too low to efficiently charge a discharged battery.

D2.3.2 Charging Lead-Acid Batteries

Lead-Acid batteries can be charged in several different ways: constant voltage, constant current, and taper current. Of these, the constant voltage technique generally is the most efficient and fastest method of charging Lead-Acid batteries. Therefore, subsequent discussions are limited to this approach.

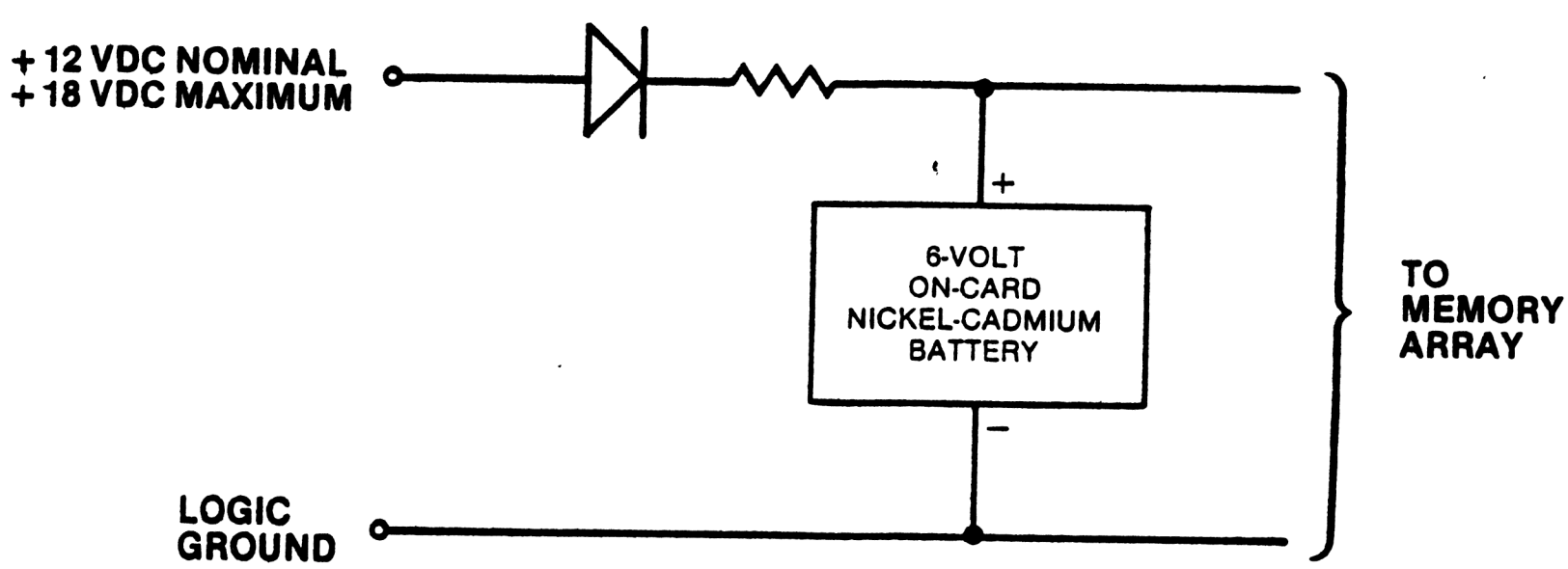


Figure D2-1. Simple Constant Current Charge

The magnitude of the constant voltage applied to the battery during charging, as well as the current capabilities of the charging source, dictate how long it will take to charge the battery. A Lead-Acid battery can be recharged in approximately two hours. Approximately 80 to 90% of the battery capacity expended during a discharge can be returned to the battery in about 30 to 45 minutes. The charger power source furnishes a 6C charge rate at a constant voltage of approximately 7.5 volts. Chargers rated at 1C to 10C could take as long as 4 to 10 hours to recharge a battery. Consult the charger and battery manufacturer's specifications to determine the proper charger and respective recharge time requirements.

In using the constant voltage recharging technique, the battery normally accepts charge current at its own rate; the current is necessary to maintain full battery capacity. Proper battery chargers can be left on, connected to the battery, while the system is running. A simple constant voltage charging source is shown in Figure D2-3. Battery manufacturers can supply customers with application notes for all types of chargers, complete with schematics and parts lists. Commercially available automotive battery chargers should not be used, since they usually do not include a voltage regulator and can cause severe memory damage or reduced battery life. Other satisfactory and inexpensive commercial float chargers are available from manufacturers such as Mauratron, Gates, Globe, and Cellmate.

D2.3.3 Undervoltage Protection

Most rechargable batteries require some type of undervoltage protection to prevent irreversible battery damage during excessive or deep discharges. Computer Automation, Inc., provides this needed protection on all Battery Backup options for external and internal batteries. This undervoltage protection is normally set at about 4.6 volts.

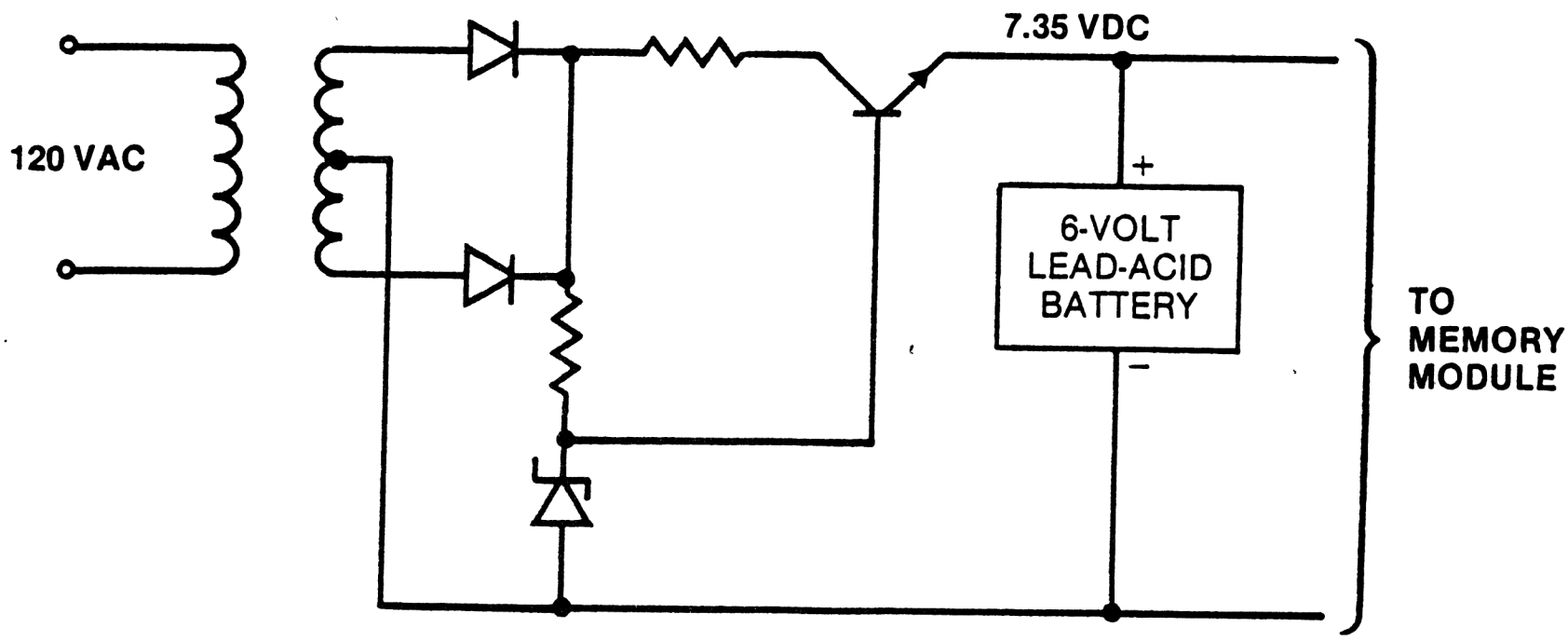


Figure D2-2. Simple Constant Voltage Source

D2.4 BATTERY EXAMPLES

An example of a battery might be, in an extreme case, a Lead-Acid automotive battery rated at 300 ampere-hours. This battery would provide a typical 8K by 16-bit MOS dynamic memory module with emergency power for 9 weeks. This emergency power undoubtedly would be sufficient to carry through short power interruptions as well as power brown-outs and black-outs.

A more reasonable battery supplying six ampere-hours typically would be smaller than 2 by 3 by 3 inches and would provide seven hours of emergency service. Generally, this is sufficient for most user's applications.

It is necessary to purchase the appropriate Computer Automation, Inc., memory backup options, even when an external battery and charger must be added to extend the basic memory retention time. This is primarily because power saving features, voltage sensing, power failure detection, and automatic switching are difficult, if not impossible, to mechanize externally from memory modules and computer equipment.

D3 BATTERY PACK - MODEL 12048-01

D3.1 INTRODUCTION

The Battery Pack is an optional unit, Model 12048-01, designed to provide battery backup support for half-card RAM memories (Model 11642-XX). When installed in an LSI-3/05 or NAKED MINI® 4 Half-Card Chassis Power Supply (Models 12046-XX and 20928-00), the Battery Pack provides a minimum of two minutes of data retention for one or two half-card RAM memory modules.

Further, these modules support for even longer power outage intervals with a user-supplied external battery.

The Battery Pack includes these features:

- Battery undervoltage protection for internal/external battery
- On-Pack 100 ma/hr Nickel-Cadmium battery
- Automatic constant current battery charger for internal/external Nickel-C admium battery
- Switch to select external battery expansion
- DC-to-DC converter, which converts 6 volts to +5, +12 and -10 volts
- Voltage regulators

With a fully-charged battery, the Battery Pack provides a minimum of six minutes (12 minutes typical) of memory retention for one half-card RAM memory, and a minimum of three minutes (six minutes typical) of memory retention for two half-card RAM memories.

D3.2 MECHANICAL DESCRIPTION

The Battery Pack option is contained on a 4.5 by 5 inch printed circuit board, and mounts in the Half-Card Chassis Power Supply. It is connected to the RAM memory modules with a 5-wire cable, supplied with the option.

D3.3 EXTERNAL BATTERY BACKUP

External Battery Backup is described in detail in Section D5, but Figure D3-1 shows a functional block diagram of how this capability can be added to a system having the Battery Pack option.

The external cable should be less than 3 meters (10 feet) long, and should be constructed of two (Metric Gage 5 to 8) AWG 22 to 26 stranded wires. A Molex connector is supplied with the option.

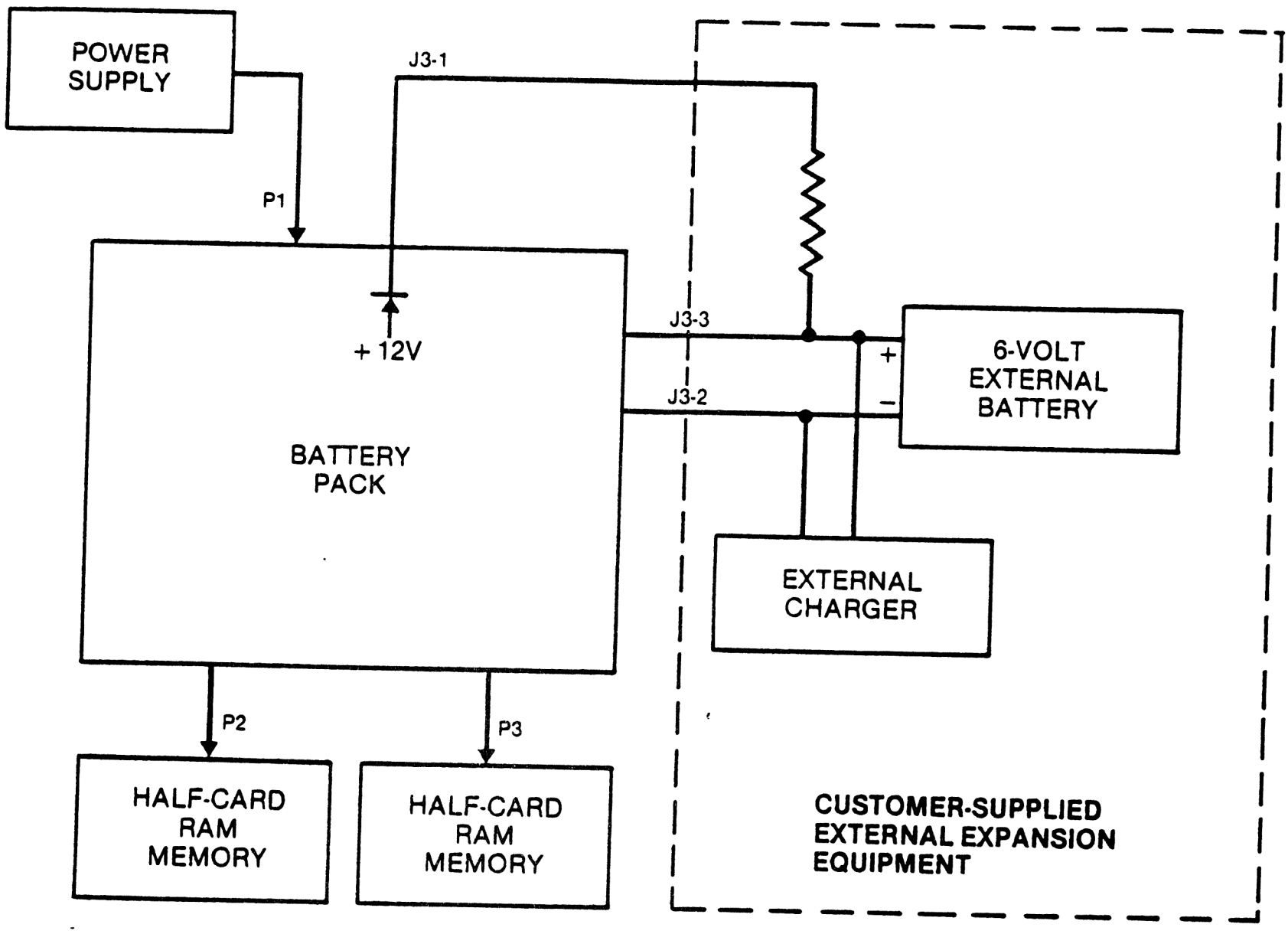


Figure D3-1. Battery Pack Block Diagram

D4 ON-CARD BATTERY BACKUP

During a primary power outage, the on-card Battery Backup option provides a minimum of two to nine minutes of data retention for the memory card on which it is mounted. Further, boards with on-card Battery Backup can be supported for even longer power outage intervals with a user-supplied external battery. On-card Battery Backup uses a 100 mA/hr Nickel-Cadmium Battery. An on-card switch to external expansion are included.

To connect the on-board battery, switch SW3 must be set in the INT position. This switch is located on the P4 plug at the rear end of the combination memory board.

Table D4-1 shows the memory retention characteristics for each memory module with on-card Battery Backup.

Table D4-1. Memory Retention with On-card Battery Backup

MEMORY MODULE	MINIMUM TIME (Minutes)	TYPICAL TIME (Minutes)
11601-08	5.0	8.0
11601-16/11611-16	3.0	5.0
11601-32/11611-32	2.0	3.0
11701-16/11711-16	3.0	3.25
11701-32/11711-32	2.0	2.5
53678-39	9.0	19.0
53678-59	2.0	4.0
53678-69	1.5	3.0
53775-16	2.0	
53775-32	2.0	
53775-64	2.0	
53819-16	2.0	6.0
53819-32	2.0	6.0
53819-64	2.0	6.0

On-card Battery Backup includes these features:

- Automatic power sensing and switching and invalid data detection
- Undervoltage protection and internal constant-current charger for internal/external battery

CAUTION

When removing a combination memory board with on-card Battery Backup from a chassis, the internal/external Battery Backup selection switch must be set in the EXT position to avoid severe machine damage. This switch SW3, is located at the rear of the memory board. Also, any external battery must be disconnected. During such disconnection, SW3 must be on INT.

External Battery Backup is described in detail in Section D5, but Figure D4-1 shows a functional block diagram of how this capability can be added to a memory module with on-card Battery Backup. The external battery charger is not required if an internal charger is used.

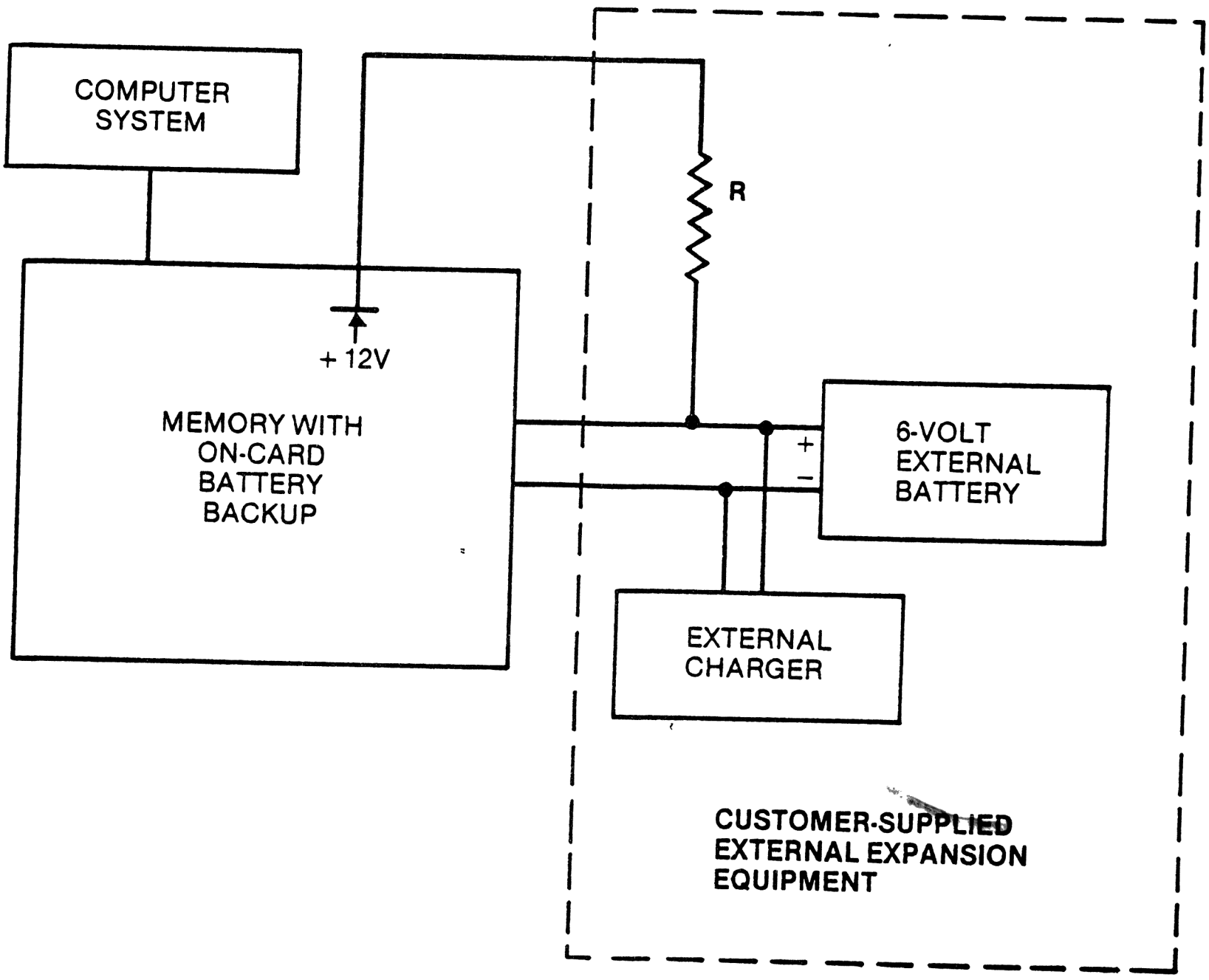


Figure D4-1. On-card Battery Backup Block Diagram

The external battery cable should be less than 10 feet long, and should be constructed of two AWG 22 to 26 (Metric Gage 5 to 8) stranded wires (four wires if internal charger is used). The connector should be Herman Smith #1234 or Keystone Electronics #72.

D5 EXTERNAL EXPANSION

D5.1 FUNCTIONAL DESCRIPTION

Both On-Card Battery Backup and Battery Pack can be expanded to provide additional memory retention by attaching a separate external battery and cable. An internal charger is incorporated into the basic Backup option for an external Nickel-Cadmium battery. This feature eliminates the external charger requirements for most expansion applications. An external charger can be connected where battery recharge ability is required and the internal charger is not adequate.

D5.2 EXTERNAL EXPANSION SPECIFICATIONS

Nickel-Cadmium or Lead-Acid batteries can be used for external backup. If an internal charger is used, a Nickel-Cadmium battery must be used. Batteries can range from 5.4 to 7.5 volts; however, external batteries exceeding 7.5 volts can cause severe damage to the Battery Backup Circuitry.

Table D5-1 shows the external battery power consumption requirements.

When external Battery Backup is used, battery undervoltage protection is not required. This protection is provided in the Battery Backup option.

Table D5-1. External Battery Power Consumption

MEMORY MODEL	BATTERY POWER CONSUMPTION
11601-08	0.5A
11601-16/11611-16	0.8A
11601-32/11611-32	1.5A
11642-XX	0.4A
11701-16/11711-16	0.8A
11701-32/11711-32	1.5A
53678-39	0.25A
53678-59	1.0A
53678-69	2.0A
53775-16	0.9
53775-32	1.4
53775-64	2.32
53819-16,32,64	2.0

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D5.3 CHARGERS FOR EXTERNAL BATTERIES

D5.3.1 Internal Charger

The internal constant current charger can be used for external Nickel-Cadmium batteries. The charger operates off the computer's ±12 volt power supply and therefore is limited to 0.25 amps. This charger can be used by connecting a customer-supplied external resistor, R, (see Figure 4-1) to the terminals provided. This resistor must be selected to regulate the current going to the battery to within 5% of the value C. The only exception to this rule is that the 12 volt power supply may not be overloaded. If the total draw on the 12 volt power supply will exceed its rating, then either a larger power supply, an external charger, or a lower charging rate should be considered. In any case, the resistor is in series with a 1N4002 diode, which has a 1.1 forward voltage at 1 amp current.

Table D5-2 shows typical battery amp/hour ratings, and expected memory data retention in hours. This table provides the user with a quick, simple method of extending the basic two minutes of data retention to 10 hours. This is accomplished by using a three- or four-wire cable, 6-volt Nickel-Cadmium battery, and a power resistor. The external resistor requirements are shown in Table D5-3. Care should be exercised when connecting the resistor so as to protect the -12 volt supply from shorting. Also see Section 6 for limitations.

D5.3.2 External Chargers

Nickel-Cadmium and Lead-Acid batteries require different external chargers: for Nickel-Cadmium batteries use a constant-current external charger; for Lead-Acid batteries use a constant voltage external charge. Suggested vendors include Mauratron Inc., Globe, Gates, and Cellmate.

D5.4 OTHER CONFIGURATIONS

A single external battery can be configured to operate in parallel with the Battery Pack option. However, the internal charger is limited to a total current draw of 0.25 amps from the Model 12046-03 power supply and 0.45 amps from either the Model 12046-05 or 20928-00 power supply. These limitations are necessary to ensure that the power supply is left with sufficient ± 12 volt power to drive the computer system.

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Table D5-2. Memory Retention With External Nickel-Cadmium Battery

MODEL	MEMORY RETENTION (Hours per battery rating)			
	1 amp/hour	2 amp/hour	2.5 amp/hour	4 amp/hour
11601-08	2.0	4.0	5.0	8.0
11601-16 and 11611-16	1.25	2.5	3.0	5.0
11611-32 and 11611-32	0.7	1.3	1.7	2.7
11642-14	2.0	4.0	5.0	8.0
11642-18	1.0	2.0	2.5	4.0
11701-16 and 11711-16	1.25	2.5	3.0	5.0
11701-32 and 11711-32	0.7	1.3	1.7	2.7
53678-39	4.0	8.0	10.0	16.0
53678-59	1.0	2.0	2.5	4.0
53678-69	0.5	1.0	1.25	2.0
53775-16	1.1	2.2	2.8	4.4
53775-32	0.7	1.4	1.8	2.8
53775-64	0.4	0.8	1.1	1.6
53819-16,32,64	0.5	1.0	1.25	2.0

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Table D5-3. Resistor For External Nickel-Cadminum Battery

BATTERY RATING (amp-hour)	EXTERNAL RESISTOR	
	VALUE ± 5%	WATTAGE
1	60 ohms	1
2	30 ohms	2
2.5	24 ohms	4
4	15 ohms	5

D6 OPERATING NOTES AND CAUTIONS

Note the following operating points:

1. The Internal/External battery switch should be set to "external" during storage or shipment to prevent internal battery discharge. Do not operate the Internal/External switch while the system is running on battery, or data may be lost.

2. An External customer-supplied battery can be disconnected while the system is running if the Internal/External battery switch has been set previously to the Internal position. If an Internal/ External switch is not present on the Backup option, the external battery may not be disconnected.

3. Internal battery recovery is approximately 10 hours after all power outage capability has been exhausted.

4. Fully discharged external batteries should not be attached to an LSI-3/05 or NAKED MINI® 4 system power supply when using an internal charger unless the external resistor sufficiently limits power supply for the +12 volt current to the appropriate value defined in Section D5.4.

5. An On-card Nickel-Cadmium battery normally discharges in storage. After 90 days of storage, the battery is fully discharged and should be re-charged.

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