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DSGN <i>V. Martin</i> V. Martin	12/2/80	SCOUT 4/04 2/4 CHANNEL RS-232 SERIAL I/O BOARD HARDWARE DESIGN SPECIFICATION		
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1.0

INTRODUCTION

The SCOUT 2/4 channel serial I/O board is an interface for up to four RS-232 compatible I/O devices with full duplex operation.

All the circuitry for the 2/4 channel serial I/O board is contained on a standard 6.25 inches x 8.3 inches SCOUT board. The board is connected to the mother board through a 70 pin edge connector. Input/Output devices are connected to the 2/4 channel serial I/O board through four (4) ten pin connectors. An appropriately configured 25-pin 'D' shell connector at the other end of the cable, provides connection to external devices.

Performance specification summary:

1. RS232 Signals

- a) Transmitter Data
- b) Request to Send
- c) Clear to Send
- d) Receiver Data
- e) Data Terminal Ready
- f) Data Set Ready

2. Baud Rates

- a) 110
- b) 150
- c) 300
- d) 600
- e) 1200
- f) 2400
- g) 4800
- h) 9600

3. Data Transfer Modes: Interrupt, Poll, or Auto I/O

2.0

FUNCTIONAL DESCRIPTION

The 2/4 channel serial I/O board consists of a baud rate generator, a UART for each channel and the necessary circuitry to interface to the SCOUT bus. Test capabilities are also provided.

2.1

Baud Rate Generator

The baud rate generator is comprised of a set of cascaded counters which divide FCLK to the required rates as listed in Paragraph 1.0. Baud rates are selectable for each UART via switches (SW1 through SW4). Every channel has an eight position DIP switch. Each position selects one of the baud rate generator outputs.

Note: Only one position of each switch is to be "ON" at any time.

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2.2 The UART

The Universal Asynchronous Receiver/Transmitter (UART) is programmed by the system software for maximum flexibility, thereby allowing the system to receive or transmit virtually any serial data communication signal presently in use. The UART performs serial-to-parallel conversion on data characters received from an input/output device or MODEM, and parallel to serial conversion on data characters received from the CPU. The UART is initialized following a reset operation by writing a mode and control word to it. The mode word contains the following data:

- a) Baud Rate Factor
- b) Character Length
- c) Parity Control
- d) Number of stop bits

The control word data is as follows:

- a) Transmit Enable
- b) Data Terminal Ready
- c) Receive Enable
- d) Send Break Character
- e) Error Reset
- f) Request to Send
- g) Internal Reset

The following data is available to the CPU in the status register of each channel:

- a) Transmit Ready
- b) Receive Ready
- c) Transmit Request
- d) Parity Error
- e) Overrun Error
- f) Framing Error
- g) Data Set Ready
- h) Break Detect

11 RS-232 input and output signals between the 2/4 channel serial I/O board and the I/O devices are buffered with line drivers and line receivers respectively.

2.3 Interface to SCOUT Bus

Interface to the bus is accomplished by buffering signals to and from the bus and with control and timing circuitry.

2.3.1 Buffering

The address bus (AB00-AB15), condition codes (CC0-CC3), reset (RST) and slow clock (SCLK) are buffered with Schmitt Trigger inverters. The data bus (DB00-DB15) is buffered with an inverting bus transceiver.

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2.3.2 Control Circuitry

The control circuitry consists of a device address, an ISOLITE ROM, a board ID, a condition code decoder, an ISOLITE indicator and an interrupt generation circuit.

2.3.2.1 Device Address

Communications between the CPU and the 2/4 channel serial I/O board is addressed through the four-bit device address. The device address is used during a data read, status read, data write, mode write, and a control write (see Paragraph 5.1).

2.3.2.2 ISOLITE ROM

The 2/4 channel serial I/O board, like all SCOUT boards, has provision for an ISOLITE ROM. Up to 4,096 bytes of ROM can be accommodated, both bipolar and MOS. An eight-pin socket with DIP shunts is used to provide the proper connections for the ROM selected. A 24 pin-socket for the ROM and all interface/control hardware are also provided.

2.3.2.3 Board ID

The on board ISOLITE ROM is addressed via board ID. A four-bit DIP switch allows one of 16 addresses which is used during the read ISOLITE ROM routine. The switches determine the order of reading individual board ISOLITE ROMs.

2.3.2.4 Condition Code Decoder

The condition code bits CC0 - CC3 are decoded internally to the Bus Interface controller (BIC) IC.

2.3.2.5 ISOLITE Indicator

The ISOLITE indicator is controlled by the CPU. It is "turned-on" at the beginning of the read ISOLITE ROM routine for the board. The indicator is "turned-off" by a system reset or after successful completion of the routine.

2.3.2.6 Interrupt Generation

Operation may be in Interrupt I/O, Auto I/O or polled mode. The mode is set by the CPU. The transmit data ready and receive data ready signals from each UART are priority encoded. An interrupt is generated when any UART "Transmit or Receive Data Ready" signal is active and operation is in the interrupt mode. The interrupt priorities are as follows:

- | | |
|-------------------------|----------------------|
| 1. Priority 0 (highest) | Read - Channel 1 |
| 2. Priority 1 | Read - Channel 2 |
| 3. Priority 2 | Read - Channel 3 |
| 4. Priority 3 | Read - Channel 4 |
| 5. Priority 4 | Transmit - Channel 1 |

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- | | |
|------------------------|----------------------|
| 6. Priority 5 | Transmit - Channel 2 |
| 7. Priority 6 | Transmit - Channel 3 |
| 8. Priority 7 (lowest) | Transmit - Channel 4 |

The outputs of the Priority Encoder are used to generate AB3-AB5 of the Vector Address. Address bits zero and one (AB0 & AB1) are always zeroes and address bit 2 selects between Data Interrupts and End-of-Block Interrupts.

2.3.3 Timing Circuitry

All timing is generated from slow clock (SCLK)] Three signals are created on the board and control all timing.

2.3.3.1 Pulse

A NOP condition code is asserted between bus cycles. After a new condition code is decoded, pulse (PLSE) is generated. Pulse is used to latch incoming signals.

2.3.3.2 Latch

The "latch" signal follows pulse and is used to latch data to be transmitted on the data bus (DB00-DB07).

2.3.3.3 Gate Out Data

"Gate out data" follows the "latch" signal and is used to enable tri-state buffers for transmission of data onto the data bus.

2.4 Test Capabilities

The SCOUT 2/4 Channel Serial I/O board is designed and developed around the ISOLITE self-test diagnostic feature. By enabling a test bit in the Function Decode Latch the on-board test circuitry automatically wrap-around channels one to two and channel three to four. The ISOLITE Diagnostic Firmware is then able to transmit and receive data between the two channel pairs. The data path between the two channel pairs does not include the drivers and receiver. However, an external wrap-around test cable can be connected from connector J1 to J2 and from J3 to J4 to allow the drivers and receivers to be included in the data path. If pin one on any of the I/O connectors (J1-J4) is grounded the presence of the wrap-around I/O cables can be detected by the ISOLITE Diagnostic through the execution of a Sense and Skip True (SST) Instruction. The test bit in the Function Decode Latch is then reset by the Diagnostic Firmware to enable the drivers and receivers.

3.0 FUNCTIONAL SPECIFICATIONS

3.1 Number of Channels

The board is available with either two or four serial channels.

3.2 Modes of Operation

The 2/4 channel serial I/O board can be operated in anyone of three modes:

1. Interrupt I/O
2. Auto I/O
3. Polled

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4.0 ELECTRICAL SPECIFICATIONS

The 2/4 channel serial I/O board is RS-232 compatible.

4.1	<u>Receiver Input Voltage</u>	Min	Type	Max	Units	Conditions
a)	Input Low Threshold Voltage (V_{TL})	0.75	--	1.25	V	$I_{OUT}=0.5ma$
b)	Input High Threshold Voltage (V_{TH})	1.00	--	1.5	V	$I_{OUT}=10ma$

4.2	<u>Receiver Input Current</u>					
	$V_{IN} = +25V$	+3.6	+5.6	+8.3	mA	
	$V_{IN} = -25V$	-3.6	-5.6	-8.3	mA	
	$V_{IN} = -5V$	- .71	-1.2	-1.7	mA	
	$V_{IN} = +5V$	+ .71	+1.2	+1.7	mA	

4.3	<u>Driver Output Voltage</u>					
a)	Low Level Output Voltage	--	-10.5	-9.0	V	$R_L=3.0K, V_{IN}=1.9V$ $V^+=13.2V, V^-=-13.2V$
b)	High Level Output Voltage	9.0	10.5			$R_L=3.0K, V_{IN}=0.8V$ $V^+=13.2, V^-=-13.2V$

4.4	<u>Driver Output Current</u>					
a)	High Level Output Short-Circuit Current	-6.0	-10.0	-12.0	mA	$V_{OUT} = 0V,$ $V_{IN} = 0.8V$
b)	Low Level Output Short-Circuit Current	6.0	10.0	12.0	mA	$V_{OUT} = 0V,$ $V_{IN} = 1.9V$

4.5	<u>Driver Output Resistance</u>	300		OHMS	$V^+=V^-=0V,$ $V_{OUT}^+=+2V$
-----	---------------------------------	-----	--	------	----------------------------------

5.0 COMPUTER INTERFACE SPECIFICATIONS

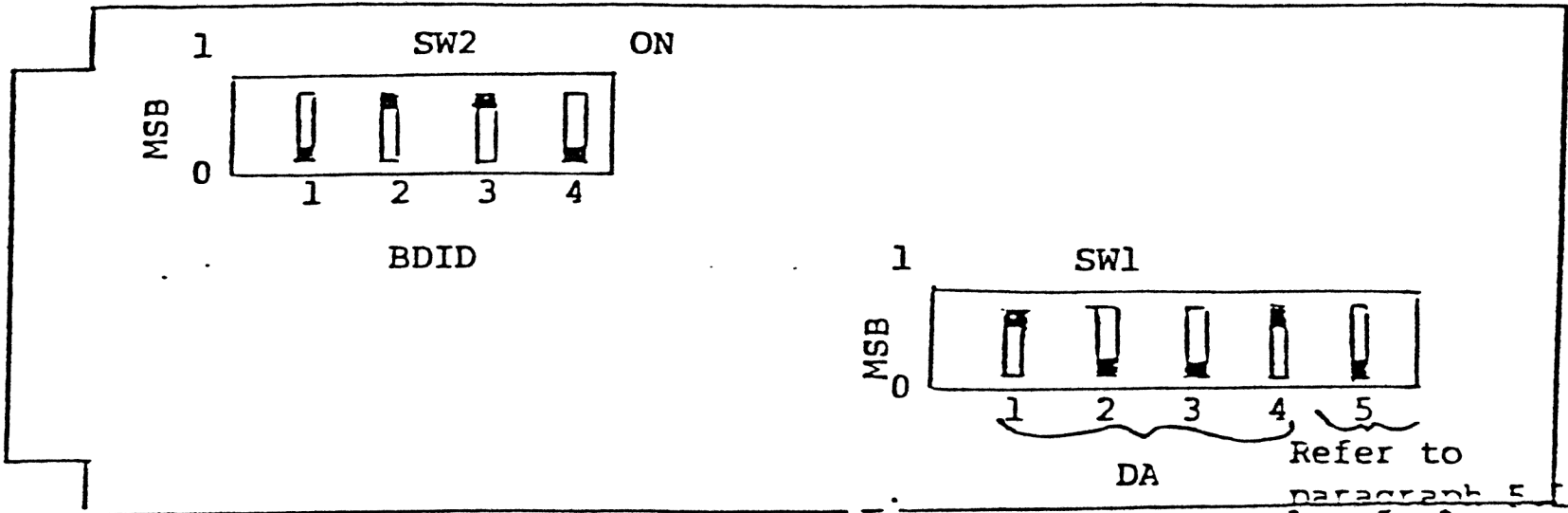
The 2/4 channel serial I/O board interfaces directly to the SCOUT Bus.

5.1 Device Address

The device address consists of four bits (AB04-AB07) which are selectable with dip switch SW7. SW7-1 selcts the most significant bit and SW7-4 selects the least significant bit. The "ON" (up) position of the switch represents a logical one (see Figure 5.1). Switch SW7-5 is undefined; however, the state of SW7-5 will be displayed in Data Bit1.1 (DB1.1) during the execution of a "RAL" instruction cycle together with the device address and data read from the ISOLITE ROM.

FIGURE 5.1

BOARD ID and DEVICE ADDRESS SWITCHES



5.2

Interrupt Vector Address

The Interrupt Vector Base Address (DB7 thru DB12) must be loaded into the Vector Address Latch using a Select and Present (SELP) output instruction prior to operating the Board in the Interrupt Mode. Vector Address Bits 0, 1, 13, 14, and 15 are always zero's and Bits two through seven (DB2-DB7) are automatically concatenated with the Base Vector Address Bit DB7 thru DB12 during normal operation. Data Bit six (DB6) is automatically set (logic 1) or reset (logic 0) depending on whether a ring interrupt or Data/EOB interrupt is being serviced respectively. Vector Address Bit two (DB2) is normally held in the reset (Logic Zero) state, however, in the Auto I/O Mode it is forced to a Logic one if an End-of-Block interrupt is generated.

5.3

ISOLITE ROM

Complete hardware has been provided on the serial I/O board to accommodate up to 4096 bytes of autoloader ROM. Three standard eight-pin DIP shunts are available to plug into the autoloader ROM addressing socket for several standard PROMs, both bipolar and MOS.

8 1	8 1	8 1	8 1
Bipolar	2716	275851856	
	2516	(Not Suggested as a STD. Pattern)	
	TI 2532	Straps For Indicated ROM Types	
	2758	Figure 5.3	

5.4 Board ID

The Board ID is selectable with DIP SWITCH SW5. SW5-4 selects the least significant bit and SW5-1 selects the most significant bit. Sixteen different values of board ID can be selected with this four-bit switch. The "ON" (up) switch position represents a logical one (See Figure 5.1).

5.5 Station ID

A Station ID Switch (SW6) is provided on the 2/4 channel serial I/O board to facilitate Multi-Drop Communication Systems. The 8-position Station I.D. DIP SWITCH allows a maximum of 256 unique Station I.D.'s to be selected. It can be read by the CPU at any time during the execution of a Status Read from any channel. The Address is placed on the Most Significant Byte of the System Data Bus (DB08 - DB15) simultaneously with the Status data read from the selected channel. Status information read from the UARTs are placed on the Least Significant Byte of the Data Bus (DB00-DB07).

5.6 Channel Address

The Channel Addresses are Software Selectable to allow for maximum system flexibility. Address bits 1 thru 3 (AB1-AB3) are used to select one of four channels. Refer to Paragraph 6.1.

6.0 SOFTWARE

The 2/4 channel serial I/O board can be operated in either the Interrupt I/O, Polled, or Auto I/O mode. Standard DIO type format has been used wherever possible. The instructions used are from the LSI 4/04 I/O instruction set.

6.1 Overview

During an I/O instruction, only the Least Significant Byte of the Address Bus is used by the Serial I/O Board. Bit fields are as follows:

a) Bits 4 - 7 Board Devide Address (switch selectable)

b) Bits 1, 2 and 3 Channel Address

000 Channel 1

001 Channel 2

010 Channel 3

011 Channel 4

c) Bit 0 Function Code

0 Data

1 Command

6.2 Write Format

An output instruction is used to write the mode, control, and data words into each channel.

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GENERAL FORMAT: OUT, DA, CH#, FC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	R2		0	0	0	1	0	Device Address			X	Ch. No.			FC

R2 = 00 A-Register
01 X-Register
10 Q-Register
11 Y-Register

CH # 00 Channel 1
01 Channel 2
10 Channel 3
11 Channel 4

X = Don't Care

DATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	—————Only Lower Byte Used—————							

x = Reserved

6.2.1 Format for Mode Write (FC = 1)

DATA (lower byte)

7	6	5	4	3	2	1	0
S2	S1	E/0	PE	L2	L1	1	0

Baud Rate Always = 10

Character Length

0	1	0	1
0	0	1	1
5 bits	6 bits	7 bits	8 bits

Parity Enable

1 = Enable
0 = Disable

Even/Odd Parity

1 = Even
0 = Odd

Number of Stop Bits

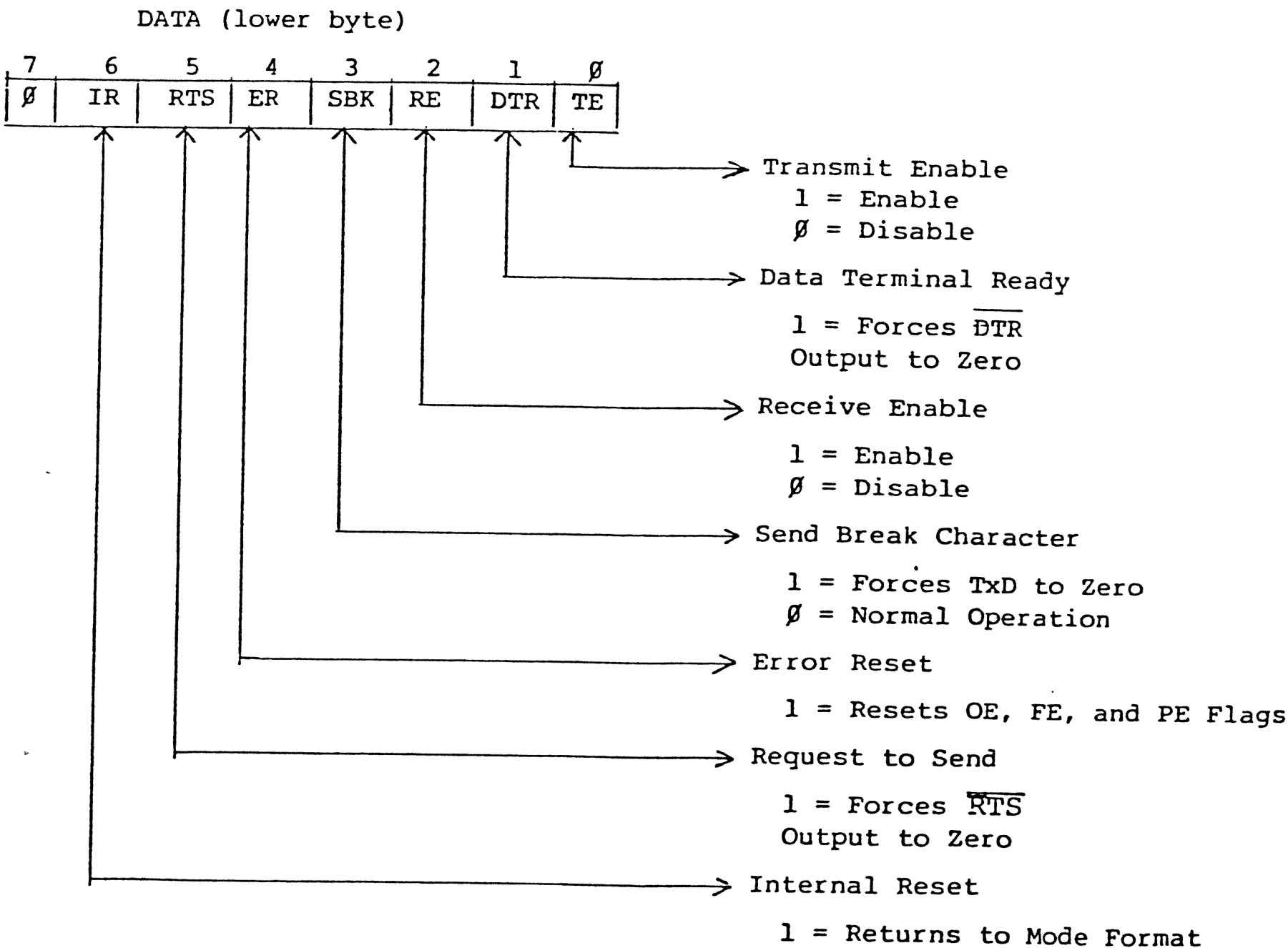
0	0	1	1
0	1	0	1
invalid	1 bit	1½ bits	2 bits

The first word (with FC=1) written to the UART following a system reset is the mode word. All subsequent words (FC=1) written to the UART are control words. The UARTs can be reset or forced to the mode instruction word format in three ways:

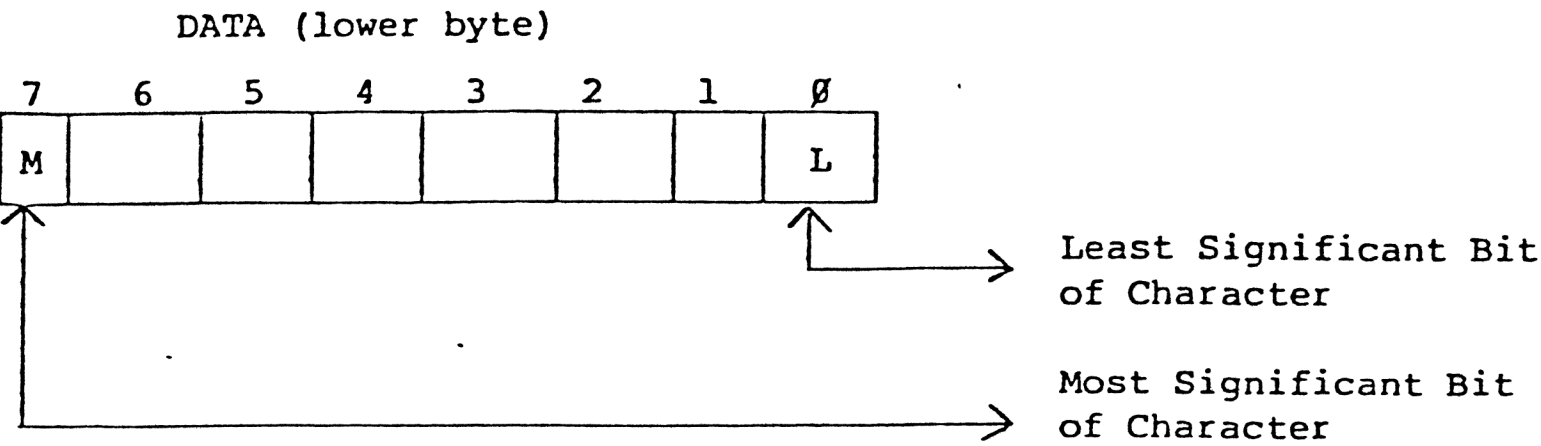
- Depressing the reset switch on the remote console will reset all UARTS and associated circuitry on the board.
- The execution of a "SELP" output instruction with DBØ3=Ø to the Function Decode Latch on the board latches all four UARTS in the reset state (See Paragraph 6.4
- Execution of an "OUT" instruction with data bit 6 equal to one and FC=1 (see control word paragraph 6.2.2) will reset only the UART specified by the channel number.

6.2.2

Format for Control Write (FC = 1)



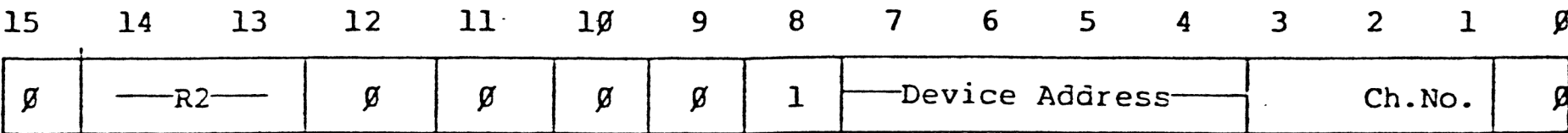
6.2.3
Format for Data Write (FC = 0)



6.3
Read Format

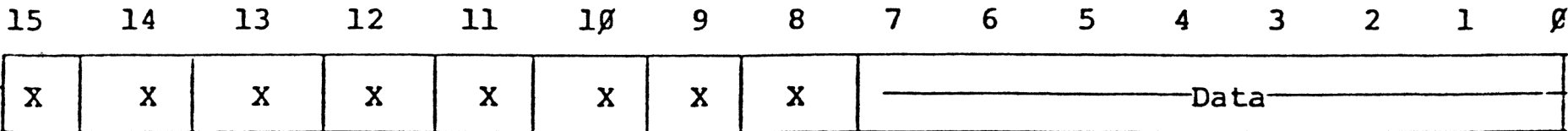
The input instruction reads status and data words from each channel.

GENERAL FORMAT: IN, DA, FC



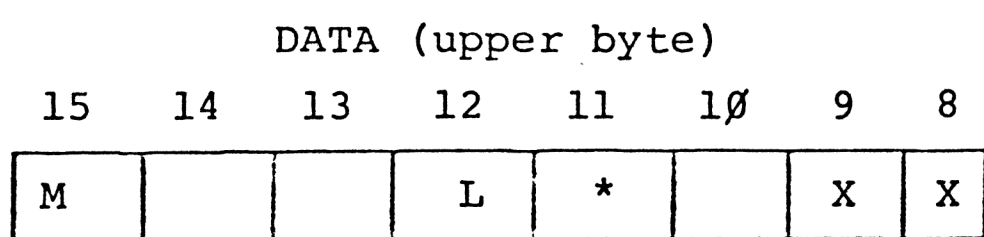
R2 = 00 A-Register
01 X-Register
10 Q-Register
11 Y-Register

DATA



x = Reserved (see Note below)

Note: When a RAL condition code is asserted by the CPU during a read ISOLITE ROM routine, data bits DB12-DB15 contain the device address, Bit 10 can be tested to determine if the ISOLITE LED is active, and Bit 11 is presently undefined.



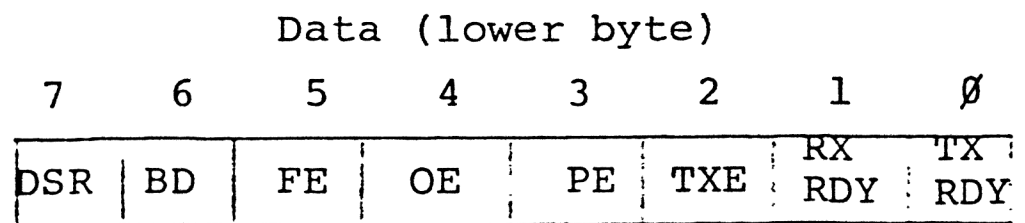
Most Significant Bit
of Device Address

1 = Isolite LED lit.
0 = Isolite LED not lit

Least Significant
Bit of Device Address

X = Reserved
* = Undefined

6.3.1 Format for Status Read (FC = 1)



Transmit Ready
1 = Ready to Receive Data from
CPU (not masked by transmit enable)

Receive Ready
1 = Ready to Transmit Data to CPU

Transmit Empty
1 = No Data to Transmit

Parity Error
1 = Parity Error Detected
0 = When ER Bit of Command In-
struction Word is a "1"

Overrun Error
1 = CPU does not read charac-
ter before the next one
becomes available.
0 = When ER Bit of Command
Instruction Word is a "1".

Framing Error
1 = Valid Stop Bit not detected at
the end of every character.
0 = When ER Bit of Command Instru-
ction Word is a "1".

Break Detect
1 = Break Character Received

Data Set Ready
1 = "Data Set Ready" Input Active

(Notes - Continued)

- NOTES:
1. FE, OE, and PE Flags do not inhibit the operation of the UART.

2. Tx RDY Status Bit = Data Buffer Empty

3. Tx RDY (pin 15) = DB Buffer Empty.CTS.TxEN.

6.3.2

Format for Status Read (FC = 1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Station I.D.								UART Status							

6.3.3

Format for Station I.D. Read (FC = 1)

An input instruction with Function Code (AB0=1) equal to one is used to read the Station I.D. switches.

GENERAL FORMAT: IN, DA, 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	R2		0	0	0	0	1	Device Address				X	X	X	1

X = Don't Care

R2 =

00 A-Register

01 X-Register

10 Q-Register

11 Y-Register

DATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Station I.D.								UART Status							

6.4

Control Format Write

A Select and Present (SELP) output instruction is used to write the Interrupt Vector Base Address, Special Character Ram, and the Function Decode Latch.

GENERAL FORMAT: SELP, DA, FC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	R2		0	0	1	0	0	Device Address				0	CH #	FC	

R2 =

00 A-Register

01 X-Register

10 Q-Register

11 Y-Register

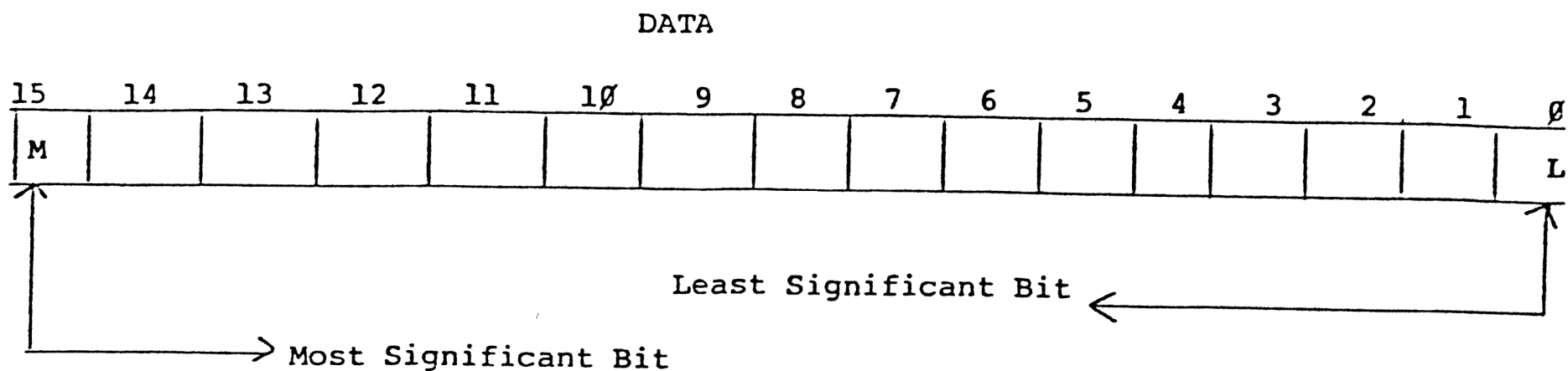
CH #

00 Channel 1

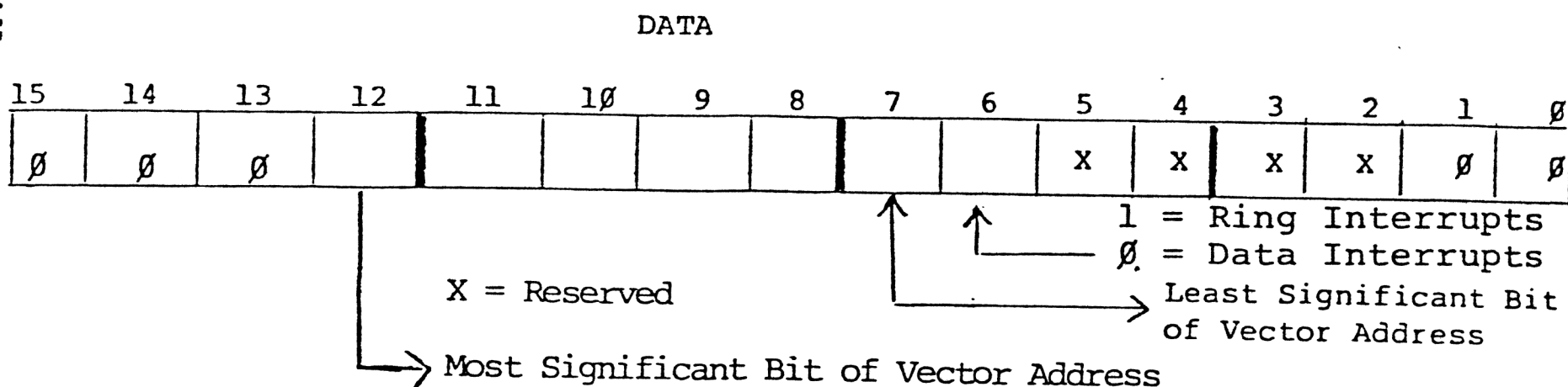
01 Channel 2

10 Channel 3

11 Channel 4



6.4.1 Interrupt Vector Write (FC = 1) SELP, DA, 1



This is the format for writing the interrupt vector base address (bits 7-12) to the board.

When a data interrupt is generated, the CPU responds with a Read Vector condition code. The interrupt vector that is transmitted to the CPU consists of the base address (bits 7-12), an interrupt index from the priority encoder (bits 3-5) and bit 0 & 1 which are always zeros to allow four program instructions at each vector. Data interrupt vectors are as follows: Note: Interrupt indexes listed below are in hexadecimal notation.

Vector Base Address	Channel 1 - Read
Vector Base + 8	Channel 2 - Read
Vector Base + 10	Channel 3 - Read
Vector Base + 18	Channel 4 - Read
Vector Base + 20	Channel 1 - Transmit
Vector Base + 28	Channel 2 - Transmit
Vector Base + 30	Channel 3 - Transmit
Vector Base + 38	Channel 4 - Transmit

EOB interrupt vectors are as follows:

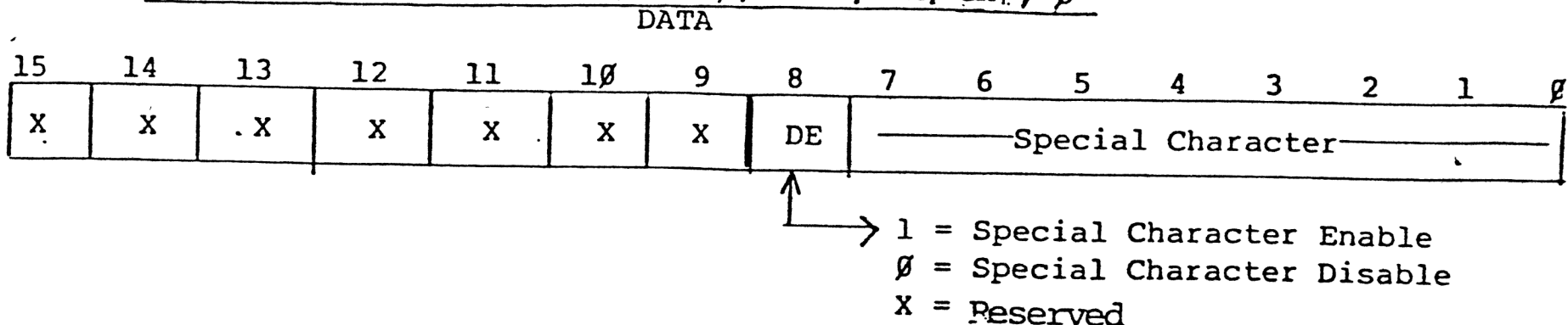
Vector Base Address + 4	Channel 1 - Read
Vector Base Address + 12	Channel 2 - Read
Vector Base Address + 14	Channel 3 - Read
Vector Base Address + 1C	Channel 4 - Read
Vector Base Address + 24	Channel 1 - Transmit

Vector Base Address + 2C Channel 2 - Transmit
Vector Base Address + 34 Channel 3 - Transmit
Vector Base Address + 3C Channel 4 - Transmit

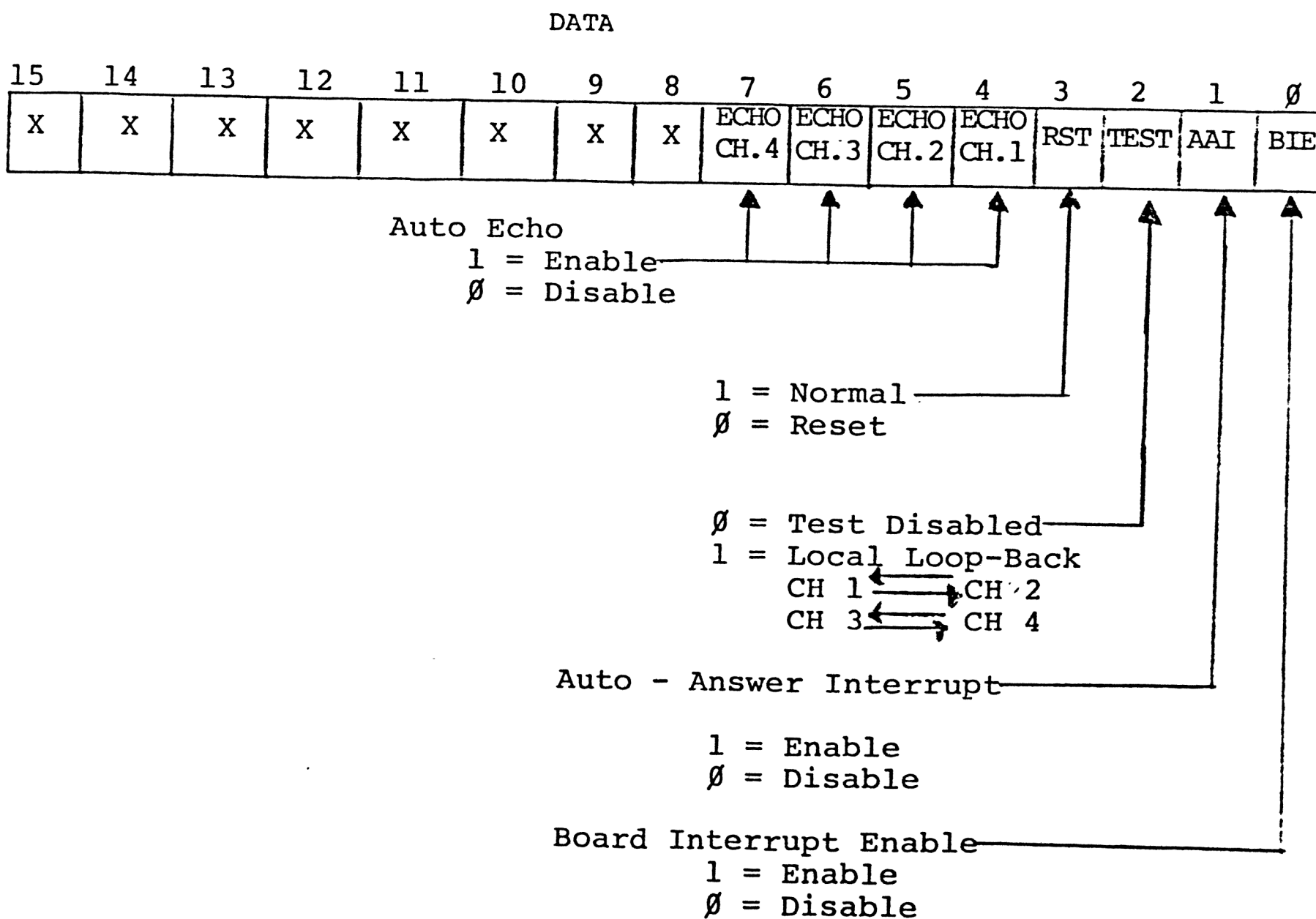
6.4.1 Ring Interrupt Vectors Are As Follows:

Vector Base Address + 40 Channel 1 - Ring Interrupt
Vector Base Address + 44 Channel 2 - Ring Interrupt
Vector Base Address + 48 Channel 3 - Ring Interrupt
Vector Base Address + 4C Channel 4 - Ring Interrupt

6.4.2 Special Character Write (FC = 0) SELP, DA, CH#, 0



6.4.3 Function Decode Latch Write (FC = 1) SELP, DA, 3



The board interrupt for all channels is controlled by the Board Interrupt Enable bit (DB 0). The Test Enable bit (DB 2) is set during the execution of a diagnostic program in the ISOLITE ROM. The Reset bit (DB 3) latches all four UARTs in the reset state, and DB1 enables

6.5 Control Format Read (FC = 0)

GENERAL FORMAT: SST DA, 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	Device Address			X	X	X	0	

X = Reserved

The control read is accomplished with a Sense & Skip True (SST) instruction. After the channel test enable bit has been set using a SELP instruction, a SST instruction is used to determine if an external wrap-around cable is present on the output connector. If the external wrap-around test cable is present (i.e. DB0 = 1) the diagnostic test program automatically resets the driver disable bit (DB2) in the Function Decode Latch thus forcing the drivers and receivers to be included in the wrap-around test loop.

6.6 Update Interrupt Status

In response to an Update Interrupt Status (UIS) instruction, the Data Inhibit Latch and the End-of-Block (EOB) Inhibit Latch will be set if Address Bit 13 or 12 is at a Logic One Level respectively. If the Data Inhibit Latch is set it will prevent the generation of Data Interrupt Requests to the CPU. Conversely, if the End-of-Block (EOB) Inhibit Latch is set it will Inhibit the generation of End-of-Block Interrupt Requests. The Data and/or End-of-Block (EOB) Inhibit Latch (ES) must be reset and the Board Interrupt Enable (BIE) Bit in the Function Decode Latch must be enabled (BIE = 1) to allow the generation of Interrupt Requests to the CPU.

6.7 Software General Procedures

Two procedures for communication with each channel are used during a power-up and data transfer routines.

6.7.1 Power-Up

The four UART's on the board will be held in the reset state whenever power is applied to the 2/4 Channel Serial I/O Board. The following procedure is recommended for initializing the board.



- a) Clear the Board Reset by setting data bit 03 in the Function Decode Latch to a logical one (DB 3 = 1). See paragraph 6.4.2 of this document.
- b) Write the appropriate data word into the Mode Register of the channel selected.
- c) Write the desired data word into the Control Register of the selected channel.
- d) A 1024 Bit x 1 Static RAM on the 2/4 Channel Serial I/O Board provides storage for 256 different special characters per channel. Special character/characters for selected channel/channels should be written into the RAM during the Initialization sequence to minimize software overhead. All 1024 locations must be addressed and unused locations must be set to zeros. A "one" in a selected memory location enables the detection of a special character for the channel selected. Refer to paragraph 6.4.2 for Special Character, Character Write Format. The detection of a special character on any channel will generate an EOB (End-of-Block) Interrupt for the corresponding channel.

6.7.2

Date Transfer

The UART's Status Register should be tested to determine if any error conditions exist prior to the transfer of data. The Error Flags (PE, OE, and FE) are not reset automatically. All the Error Flags are reset simultaneously when the Error Reset (ER) Bit of the Command Instruction Word is a "1".

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6.8

Auto I/O

The 2/4 channel serial I/O board supports Auto I/O operation. The board is designed to allow data transfers up to 9600 baud full-duplex on all four channels simultaneously with minimum loading on the CPU through the use of the Auto I/O feature.

The Auto I/O feature on the board responds to two types of interrupts: 1) Data Interrupts and 2) End-of-Block Interrupts. The Data Interrupts can be disabled or enabled by executing an Update Interrupt State (UIS) instruction in conjunction with address bit 13 set or reset respectively. If the Board Interrupt Enable (BIE) bit in the Function Decode Latch is set (i.e. BIE = 1) the board will generate a data interrupt for every receive or transmit data. The data interrupts are organized on a priority scheme with the receive data interrupts having priority over the transmit data interrupts. And conversely, all receive EOB interrupts have priority over all transmit EOB interrupts. An EOB interrupt will be generated if 1) the byte count in the Auto I/O Block is equal to zero (BC=0) or 2) a special character is detected. If an EOB interrupt is pending on any channel the corresponding channel's data interrupt will be inhibited until the EOB interrupt is serviced. For example, if channel zero is receiving a block of data and a special character is detected or the byte count is equal to zero the board will automatically inhibit data interrupts on channel zero. Therefore, if another burst (block) of data is transferred to channel zero before the pending EOB interrupt is serviced the data transferred to channel zero will be lost. Servicing the EOB interrupt for any channel automatically resets the EOB Request and re-enables the corresponding channel data interrupts.

The EOB interrupts are also disabled/enabled by executing an Update Interrupt Status (UIS) instruction to the board with address bit 12 (AB12) set or reset respectively. If the EOB interrupts are disabled special character detect and byte count equals zero will continue to set the EOB interrupt bit for the selected channel/channels, however, an interrupt will not be sent to the CPU. Note, however, that since the EOB logic on the board is still active if an EOB interrupt is pending the corresponding channel's data interrupt will be inhibited until the EOB is serviced. Re-enabling the EOB interrupts on the fly or at any time during the execution of the operating software will immediately generate an EOB interrupt if there is one pending. Refer to paragraphs 6.4.1 and 6.4.2 for data and EOB interrupt locations respectively.

6.9

Write Receive EOB

The Receive End-of-Block (EOB) bit is set whenever a Read I/O Data and Echo (RIDE) instruction is executed by the CPU following the detection of a Byte Count (BC) equal to zero on the appropriate channel or a Special Character is detected.

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GENERAL FORMAT: AIB DA, CH#, FC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	1	0	1	DA				0	CH#		0

CH# 00 Channel 1
01 Channel 2
10 Channel 3
11 Channel 4

6.10 Write Transmit EOB

The transmit End-of-Block interrupt bit is set whenever a Write I/O Data with Echo instruction is executed by the CPU following the detection of a byte count equal to zero on the appropriate transmit channel.

GENERAL FORMAT: AOB DA, CH#, FC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	1	DA				1	CH#		0

CH# = 00 Channel 1
01 Channel 2
10 Channel 3
11 Channel 4

6.11 Clear Transmit EOB

The transmit End-of-Block interrupt bit is reset following the execution of a Write I/O Data, Read I/O data or a Read Status operation from the appropriate channel. Channel address bit 3 must be set to a logic one to access the transmit EOB bits. Therefore, whenever setting or resetting the transmit EOB bits the effective channel addresses will be 8, A, C, or E for channels 1-4 respectively.

6.12 Clear Receive EOB

The receive End-of-Block interrupt bit is reset following the execution of a Write I/O Data, Read I/O data or Read Status operation from the appropriate channel. Channel address bit 3 must be a logic zero to access the receive EOB bits.

6.13 Special Character Detect

The 2/4 channel serial I/O board is capable of detecting 256 different special characters per channel. A 1K x 1 Static RAM is provided on the board to facilitate storage of up to 1024 characters.

Special characters should be loaded into the RAM during the Initialization Routine and all unused locations must be loaded with zeros. If no special characters are selected for any channel, all 1024 RAM locations must be filled with zeros.

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The detection of a special character on a selected channel will generate an End-of-Block (EOB) interrupt. A "Select and Present" output instruction with a Function Code equal to zero (FC = 0) is used to load the special character RAM]

GENERAL FORMAT: SELP DA: CH#, FC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	—R2—		∅	∅	1	∅	∅	—DA—			∅	Ch. #		∅	

R2 = 00 A-Register
01 X-Register
10 Q-Register
11 Y-Register

Ch.# = 00 Channel 1
01 Channel 2
10 Channel 3
11 Channel 4

DATA FORMAT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	Data	—Special Character—							

X = Don't Care

Data = 0 Load zero into RAM location addressed by special character.
i.e. Special character detect disabled.

= 1 Load one into RAM location addressed by special character.
i.e. Special character detect enabled.

6.14

Auto-Answer

A sixteen pin DIP socket is provided on the 2/4 channel Serial I/O Board to accomodate an optional auto-answer piggy-back board. The auto-answer circuitry is contained on a PCB that is dementionally scaled down to allow simultaneous placement with the existing Bus Interface Controller (BIC) Emulator Board. The Ring Indicator Signal (CE) for each channel is prioritized with channel one having the highest priority. Data and End-of-Block (EOB) interrupts all have priority over the Ring Interrupts. Each channel Ring Interrupt will vector to a unique memory address. Refer to Paragraph 6.4.1.

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6.15

Auto Echo

The Automatic Echo Mode is enabled independently for channels one through four by setting Bits four through seven (DB4 - DB7) in the Function Decode Latch to a logic one respectively.

In the Automatic Echo Mode received Data is automatically directed to the TXD Line while normal Receive Operation continues. The Receiver must be Enabled (CR2 = 1), but the transmitter need not be enabled. CPU to Receiver Communications continues normally, but the CPU to Transmitter Link is disabled.

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7.0

TESTING CAPABILITIES

Functional testing of the 2/4 channel serial I/O board is possible by transmitting data between two channels and checking for data and channel errors. During the execution of a diagnostic program in the ISOLITE ROM[Test Enable bit 2 (paragraph 6.4.2) is set and data is transmitted between channels one and two. The procedure is repeated with Test Enable bit 2 for channels three and four. When either test is enabled, all UART baud rates are automatically set to 9600. During the execution of an ISOLITE Diagnostic program, a test is made to detect the presence of a test cable on J1. If the cable is present then the data path is through the RS-232 drivers/receivers and the transmit channel's Request To Send is returned to its Clear To Send. (DTR and DSR are not connected.) Detection of the cable is made by executing a SST instruction after setting the Test Enable bit. A logical one on DB00 indicates the cable is connected. However, if the cable is not present then the data path is through a set of multiplexers and the RS-232 drivers/receivers are not functionally tested. Normally, a test cable will not be used by the customer during an ISOLITE test.

8.0

POWER REQUIREMENTS

All power for the 2/4 channel serial I/O board is supplied by the five-volt power supply.

8.1

DC to DC Converters

DC to DC Converters provide the required +12 volts and -12 volts for the RS-232 drivers.

8.2

POWER CONSUMPTION

Power consumption is dependent upon the population of the board.

- a) Two channels: 1.14 amps (typical)
1.74 amps (maximum)
- b) Four channels: 1.34 amps (typical)
2.02 amps (maximum)

9.0

ENVIRONMENTAL

The 2/4 channel serial I/O board will operate in an environment of 0° to 50°C. and from 10% to 90% relative humidity, non-condensing. Non Operating = -20° to +85°C.

10.0

CONNECTOR PIN IDENTIFICATION

Five connectors are available on the SCOUT RS-232 serial I/O board. Connector P1 interfaces the board to the SCOUT Bus and connectors J1-J4 interfaces the board to external serial I/O devices.

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10.1 P1 SCOUT Bus Connector

P1 follows the standard SCOUT bus pin assignments. (See SCOUT Bus specification 76-22009-00.)

J1-J4 Serial I/O Connectors

J1-J4 have the same pin out for channels one through four respectively.

<u>J1</u> <u>Pin Number</u>	<u>Signal</u> <u>Name</u>
1	Test
2	Data Terminal Ready
3	Transmit Data
4	Receive Data
5	Clear to Send
6	Data Set Ready
7	Ground
8	Ring Indicator
9	Reserved
10	Request To Send

Note: Recommended mating J1 connector part number is Berg double row conn. housing. P/N 65043-032, loose pins, crimp, 40 u gold over nickel P/N 47745.