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SCOUT 4/04
2/4 CHANNEL SERIAL I/O BOARD
HARDWARE DESIGN SPECIFICATION

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SIZE	DOC. NO.	REV
A	76-54121-01	
SCALE	SHEET 1 OF 22	

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1.0 Introduction

The SCOUT 2/4 channel serial I/O board is an interface for up to four RS-232 compatible I/O devices with full duplex operation.

All the circuitry for the 2/4 channel serial I/O board is contained on a standard SCOUT board which is 6.25 inches x 8.3 inches. The board is connected to the motherboard through a 70 pin edge connector. Input/Output devices are connected to the 2/4 channel serial I/O board through four (4) ten pin connectors. An appropriately configured 25-pin 'D' shell connector at the other end of the cable, provides connection to external devices.

Performance specification summary:

1. RS-232 Signals

- a) Transmitted Data
- b) Request to Send
- c) Clear to Send
- d) Received Data
- e) Data Terminal Ready
- f) Data Set Ready

2. Baud Rates

- a) 110
- b) 150
- c) 300
- d) 600
- e) 1200
- f) 2400
- g) 4800
- h) 9600

3. Data Transfer Mode - Interrupt or Poll

2.0 Functional Description

The 2/4 channel serial I/O board consists of a baud rate generator, a UART for each channel and the necessary circuitry to interface to the SCOUT bus. Test capabilities are also provided.

2.1 Baud Rate Generator

The baud rate generator is comprised of a set of cascaded counters which divide ECLK to the required rates as listed in Paragraph 1.0. Baud rates are selectable for each UART via switches (SW3 through SW6). Every channel has an eight position DIP switch. Each position selects one of the baud rate generator outputs.

Note: Only one position of each switch is to be "ON" at any time.

2.2 The UART

The Universal Asynchronous Receiver Transmitter (UART) provides serial and parallel data conversions and a status register for each channel.

The UART is initially programmed during an initialization sequence by the CPU. Programming each UART requires a mode word and control word. The mode word contains the following data:

- a) Baud Rate Factor
- b) Character Length
- c) Parity Control
- d) Number of stop bits

The control word data is as follows:

- a) Transmit Enable
- b) Data Terminal Ready
- c) Receive Enable
- d) Send Break Character
- e) Error Reset
- f) Request to Send
- g) Internal Reset

The following data is available to the CPU in the status register of each channel:

- a) Transmit Ready
- b) Receive Ready
- c) Transmit Request
- d) Parity Error
- e) Overrun Error
- f) Framing Error
- g) Data Set Ready

All RS-232 input and output signals between the 2/4 channel serial I/O board and the I/O devices are buffered with line drivers and line receivers respectively.

2.3 Interface to SCOUT Bus

Interface to the bus is accomplished by buffering signals to and from the bus and with control and timing circuitry.

2.3.1 Buffering

The address bus (AB00-AB15), condition codes (CC0-CC3), reset (RST) and slow clock (SCLK) are buffered with Schmitt Trigger inverters. The data bus (DB00-DB15) is buffered with an inverting bus transceiver.

2.3.2 Control Circuitry

The control circuitry consists of a device address, an ISOLITE ROM, a board ID, a condition code decoder, an ISOLITE indicator and interrupt generation circuitry.

2.3.2.1 Device Address

Communications between the CPU and the 2/4 channel serial I/O board is addressed through the five-bit device address. The device address is used during a data read, status read, data write, mode write, and a control write (see Paragraph 5.1).

2.3.2.2 ISOLITE ROM

The 2/4 channel serial I/O board, like all SCOUT boards, has provision for an ISOLITE ROM. Up to 4,096 bytes of ROM can be accommodated,

both bipolar and MOS. An eight-pin socket with DIP shunts is used to provide the proper connections for the ROM selected. A 24 pin-socket for the ROM and all interface/control hardware are also provided.

2.3.2.3 Board ID

The on board ISOLITE ROM is addressed via board ID. A four-bit DIP switch allows one of 16 addressing which is used during the read ISOLITE ROM routine. The switches determine the order of reading individual board ISOLITE ROMs.

2.3.2.4 Condition Code Decoder

The condition code bits CC0 - CC3 are decoded internally to the Bus Interface controller (BIC) IC.

2.3.2.5 ISOLITE Indicator

The ISOLITE indicator is controlled by the CPU. It is "turned-on" at the beginning of the read ISOLITE ROM routine for the board. The indicator is "turned-off" by a system reset or after successful completion of the routine.

2.3.2.6 Interrupt Generation

Operation may be in either an interrupt mode or a polled mode. The mode is set by the CPU. The transmit data ready and receive data ready signals from each UART are priority encoded. An interrupt is generated when any UART "Transmit or Receive Data Ready" signal is active and operation is in the interrupt mode. The interrupt priorities are as follows:

- | | |
|-------------------------|----------------------|
| 1. Priority 0 (highest) | Read - Channel 1 |
| 2. Priority 1 | Read - Channel 2 |
| 3. Priority 2 | Read - Channel 3 |
| 4. Priority 3 | Read - Channel 4 |
| 5. Priority 4 | Transmit - Channel 1 |
| 6. Priority 5 | Transmit - Channel 2 |
| 7. Priority 6 | Transmit - Channel 3 |
| 8. Priority 7 (lowest) | Transmit - Channel 4 |

The priority code is used for three lower address bits (AB01-AB 03) to determine the interrupt vector.

2.3.3 Timing Circuitry

All timing is generated from slow clock (SCLK). Three signals are created on the board and control all timing.

2.3.3.1 Pulse

A NOP condition code is asserted between bus cycles. After a new condition code is decoded, pulse (PLSE) is generated. Pulse is used to latch incoming signals.

2.3.3.2 Latch

The "latch" signal follows pulse and is used to latch data to be transmitted on the data bus (DB00-DB07).

2.3.3.3 Gate Out Data

"Gate out data" follows the "latch" signal and is used to enable tri-state buffers for transmission of data onto the data bus.

2.4 Test Capabilities

A functional test of the 2/4 channel serial I/O board can be accomplished executing a diagnostic routine in the ISOLITE ROM. Data is transmitted between two channels and received data is checked. The data path from one channel to the other is via a multiplexer which by-passes the RS-232 drivers and receivers. However, a test cable can be connected to J1 and the data path will include the RS-232 drivers and receivers. The program detects the presence of the test cable by a pin being grounded which asserts the SER signal driving a Sense and Skip True (SST) instruction.

3.0 Functional Specifications

3.1 Number of Channels

The board is available with either two or four serial channels.

3.2 Modes of Operation

The two modes of operation are interrupt and polled.

4.0 Electrical Specifications

The 2/4 channel serial I/O board is RS-232 compatible.

4.1 Receiver Input Voltage

	<u>Min</u>	<u>Type</u>	<u>Max</u>	<u>Units</u>	<u>Notes</u>
a) Input Low Threshold Voltage (V_{TL})	0.75	--	1.25	V	$I_{OUT}=0.5ma$
b) Input High Threshold Voltage (V_{TH})	1.10	--	1.5	V	$I_{OUT}=10ma$

4.2 Receiver Input Current

$V_{IN} = +25V$	+3.6	+5.6	+8.3	mA
$V_{IN} = -2.5V$	-3.6	-5.6	-8.3	mA
$V_{IN} = -5V$	-.71	-1.2	-1.7	mA
$V_{IN} = +5V$	+.71	+1.2	+1.7	mA

4.3 Driver Output Voltage

a) Low Level Output Voltage	--	-10.5	-9.0	V	$R_L=3.0K, V_{IN}=1.9V$ $V+=13.2V, V-=13.2V$
b) High Level Output Voltage	9.0	10.5			$R_L=3.0K, V_{IN}=0.8V$ $V+=13.2, V-=13.2V$

4.4 Driver Output Current

a) High Level Output Short-Circuit Current	-6.0	-10.0	-12.0	mA	$V_{OUT} = 0V,$ $V_{IN} = 0.8V$
b) Low Level Output Short-Circuit Current	6.0	10.0	12.0	mA	$V_{OUT} = 0V,$ $V_{IN} = 1.9V$

4.5 Driver Output Resistance

300

 $V+=V-=0V,$
 $V_{OUT}=\pm 2V$

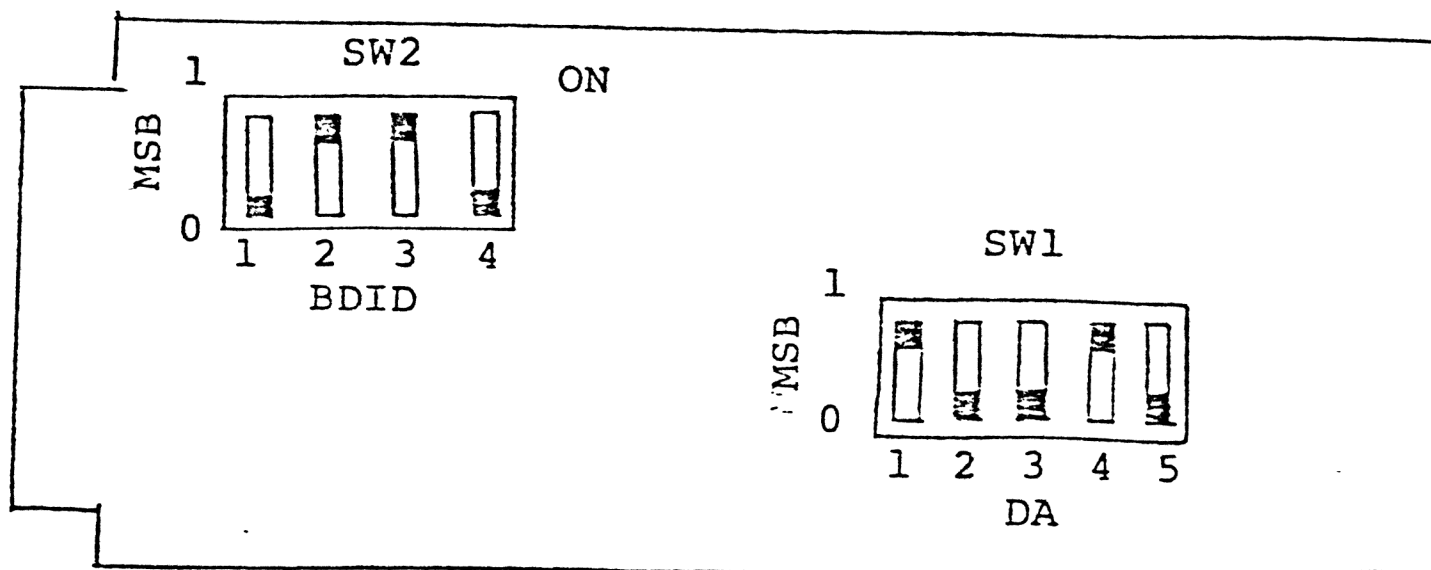
5.0 Computer Interface Specifications

The 2/4 Channel Serial I/O Board interfaces directly to the SCOUT Bus.

5.1 Device Address and Channel Number

The device address consists of five bits (AB03-AB07) which are selectable with dip switch SW1. SW-1 selects the most significant bit and SW1-5 selects the least significant bit. The "ON" (up) position of the switch represents a logical one (see Figure 5.1). Address bits 01 and 02 are used to select one of four Serial I/O Channels. (See paragraph 6.1).

FIGURE 5.1
BOARD ID and DEVICE ADDRESS SWITCHES

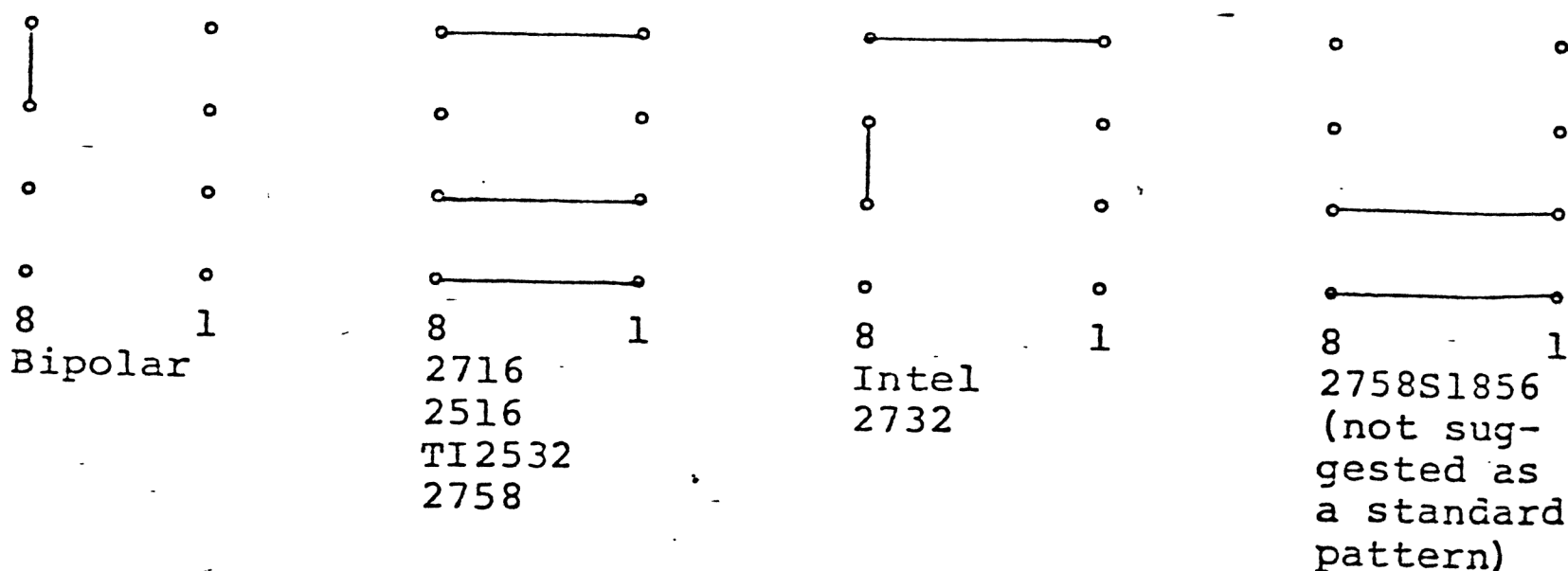


5.2 Interrupt Vector Address

If operation is in the interrupt mode, an interrupt vector must be determined by the CPU. The 12 most significant bits of the data bus (BDB04-DB15) are latched during a SELP instruction. Data bits DB01-DB03 are provided by the priority encoded interrupt signals from the UARTs. Bit 0 of the vector address is always zero.

5.3 ISOLITE ROM

Complete hardware has been provided on the serial I/O board to accommodate up to 4096 bytes of autoloader ROM. Three standard eight-pin DIP shunts are available to plug into the autoloader ROM addressing socket for several standard PROMs, both bipolar and MOS.



STRAPS FOR INDICATED ROM TYPES

Figure 5.3

5.4 Board ID

The Board ID is selectable with DIP SWITCH SW2. SW2-4 selects the least significant bit and SW2-1 selects the most significant bit. Sixteen different values of board ID can be selected with this four-bit switch. The ON (up) switch position represents a logical one (See Figure 5.1).

5.5 Station ID

A Station ID Switch (SW) is provided on the 2/4 Channel Serial I/O Board to facilitate Multi-Drop Communication Systems. The 8-position Station I.D. DIP SWITCH allows a maximum of 256 unique Station I.D.'s to be selected. It can be read by the CPU at any time during the execution of a Status Read from any channel. The Address is placed on the Most Significant Byte of the system Data Bus (DB08-DB15) simultaneously with the Status data read from the selected channel. Status information read from the UARTS are placed on the Least Significant Byte of the Data Bus (DB00-DB07).

6.0 Software

The 2/4 Channel Serial I/O Board is controlled by programmed I/O. Standard DIO type format has been used wherever possible. The instructions used are from the LSI 4/04 I/O instruction set.

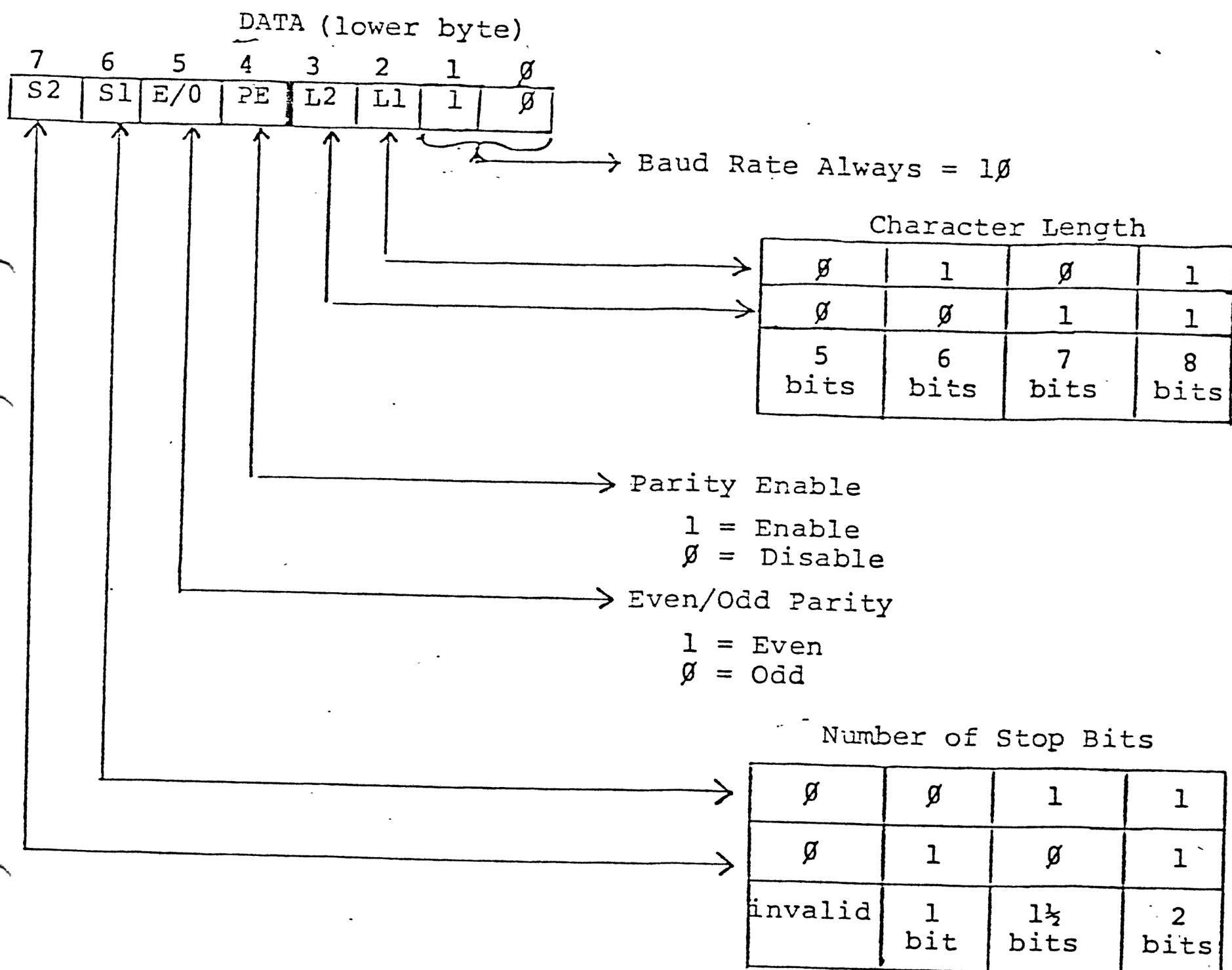
6.1 Overview

During an I/O instruction, only the Least Significant Byte of the Address Bus is used by the Serial I/O Board. Bit fields are as follows:

- a) Bits 3 - 7 Board Device Address is switch selectable
- b) Bits 1 and 2 Channel Address

00	Channel 1
01	Channel 2
10	Channel 3
11	Channel 4

6.2.1 FORMAT FOR MODE WRITE (FC = 1)

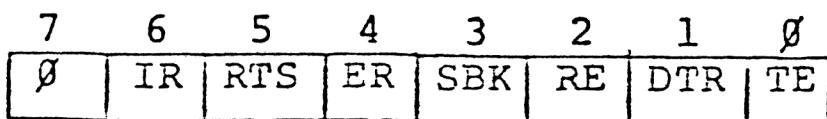


The first word (with FC=1) written to a UART after system reset is the mode word. All subsequent words (F=1) written to the UART are control words. The reset can be generated in three methods:

- 1) Assertion of a signal on the reset (RST) line will reset all UARTs and the remaining board circuitry.
- 2) Execution of a SELP instruction with the reset bit set will have the same effect as in 1 above (See Paragraph 6.4.2).
- 3) Execution of an OUT instruction with FC=1 (see control word paragraph 6.2.2) will reset only the UART specified by the channel number.

6.2.2 FORMAT FOR CONTROL WRITE (FC =1)

DATA (lower byte)



Transmit Enable

1 = Enable

0 = Disable

Data Terminal Ready

1 = Forces $\overline{\text{DTR}}$

Output to Zero

Receive Enable

1 = Enable

0 = Disable

Send Break Character

1 = Forces TxD to Zero

0 = Normal Operation

Error Reset

1 = Resets OE,

FE and PE Flags

Request to Send

1 = Forces to $\overline{\text{RTS}}$

Output to Zero

Internal Reset

1 = Returns to Mode Format

6.3.1 FORMAT FOR STATUS READ (FC = 1)

DATA (lower byte)

7	6	5	4	3	2	1	0
DR	X	FE	OE	PE	TE	RR	TR

Transmit Ready
1 = Ready to Receive Data from CPU (not masked by transmit enable)

Receive Ready
1 = Ready to Transmit Data to CPU

Transmitter Empty
1 = No Data to Transmit

Parity Error
1 = Error; Reset in Command Word (ER bit), will not inhibit operation

Overrun Error
1 = Error if CPU does not read character before the next one becomes available. Reset in Command Word (ER bit), will not inhibit operation

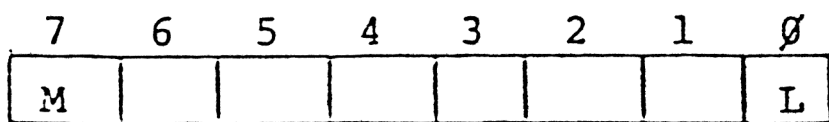
Framing Error
1 = Valid stop bit not detected at end of every character. Reset in Command Word (ER bit), will not inhibit operation

Don't Care

Data Ready
1 = Data Set Ready Indicated

6.2.3 FORMAT FOR DATA WRITE (FC = 0)

DATA (lower byte)

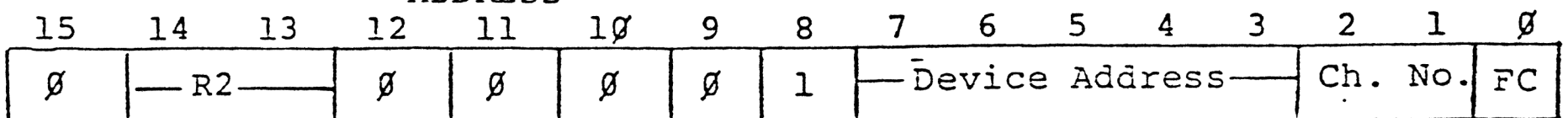
Least Significant Bit
of CharacterMost Significant Bit
of Character

6.3 Read Format

The input instruction reads status and data words from each channel.

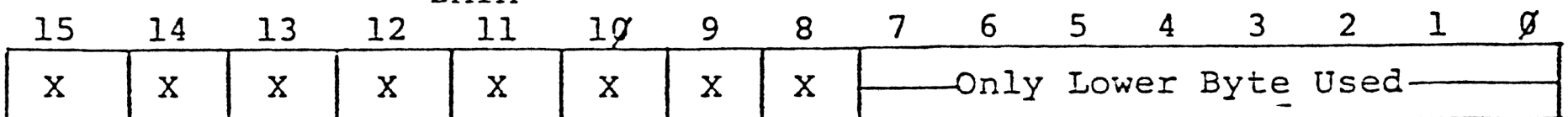
GENERAL FORMAT: IN, DA, FC

ADDRESS



R2 = 00 A Register
 01 X Register
 10 Q Register
 11 Y Register

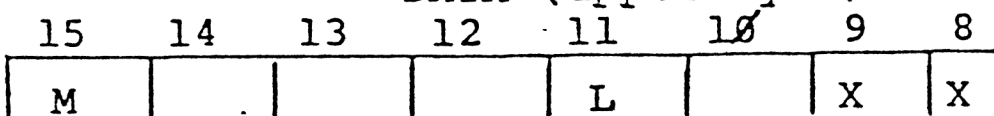
DATA



X = Don't Care (see Note below)

Note: When a RAL condition code is asserted by the CPU during a read ISOLITE ROM routine, data bits DB11-DB15 contain the device base address.

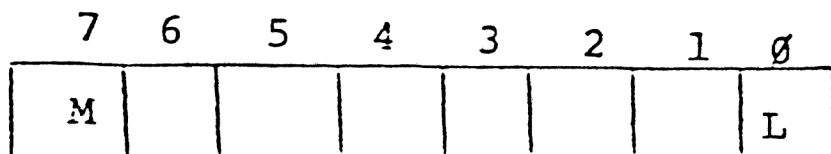
DATA (upper byte)

Most Significant Bit
of Device Address.

1 = Isolite LED lit.
 0 = Isolite LED not lit.
 Least Significant Bit
of Device Address

6.3.2 Format for Data Read (FC = 0)

DATA (lower byte)



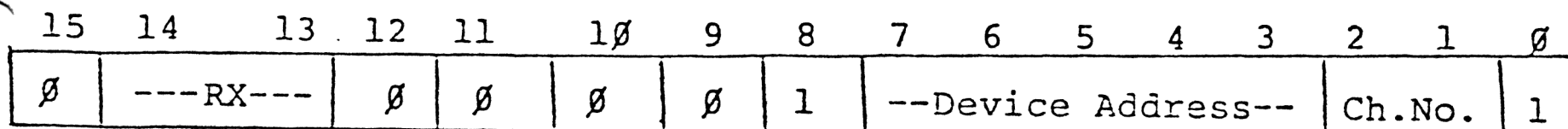
Least Significant bit of character

Most Significant bit of character

6.3.3 Format for Station I.D. Read (FC = 1)

An input instruction with Function Code (DB0=1) equal to one is used to read the Station I.D. switches.

GENERAL FORMAT: IN, DA, FC+1



RX = 00 A Register
 01 X Register
 10 Q Register
 11 Y Register

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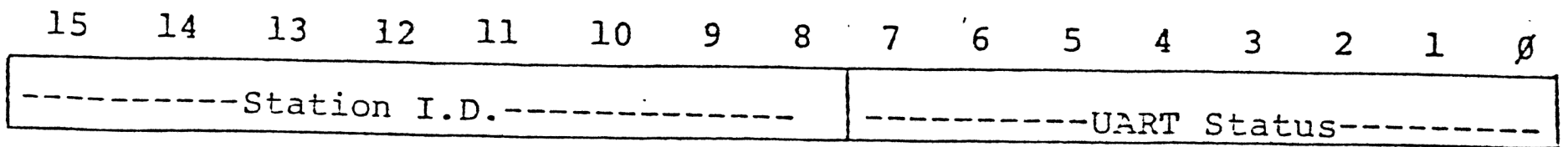
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DATA

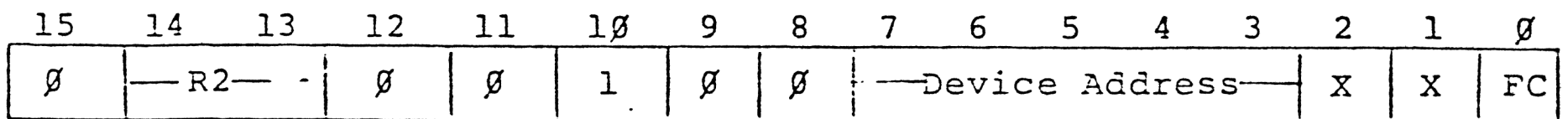


6.4 Control Format Write

The select and present instruction writes the interrupt vector address and an interrupt inhibit bit to the board.

GENERAL FORMAT: SELP, DA, FC

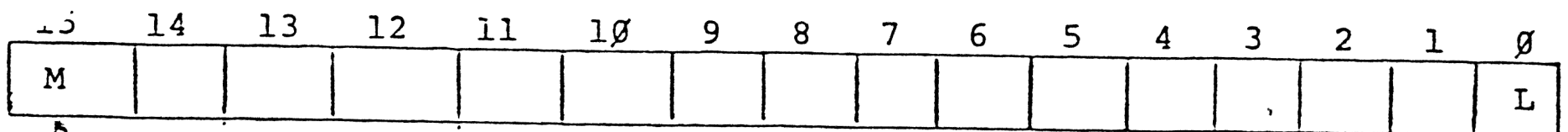
ADDRESS



R2 = 00 A Register
 01 X Register
 10 Q Register
 11 Y Register

X = Don't Care

DATA



Least Significant Bit ←

→ Most Significant Bit

c) Bit 0

Function Code

0 Data

1 Command

6.2 Write Format

An output instruction is used to write the mode, control, and data words into each channel.

GENERAL FORMAT: OUT, DA, FC

ADDRESS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	R2		0	0	0	1	0	Device Address					Ch.No.		FC

RS = 00 A-Register
01 X-Register
10 Q-Register
11 Y-Register

DATA															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	-----Only Lower Byte Used-----							

X = Don't Care

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2/4 Channel Serial I/O Board

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6.4.1 INTERRUPT VECTOR WRITE (FC = 0)

DATA															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												X	X	X	X

X = Don't Care

Most Significant Bit of Vector Address

This is the format for writing the interrupt vector base address (bits 4-15) to the board.

When an interrupt is generated, the CPU responds with a Read Vector condition code. The interrupt vector that is transmitted to the CPU consists of the base address (bits 4-15), an interrupt index from the priority encoder (bits 1-3) and bit 0 which is always a zero to allow two program instructions at each vector. Interrupt vectors are as follows:

Vector Base Address	Channel 1 - Read
Vector Base +2	Channel 2 - Read
Vector Base +4	Channel 3 - Read
Vector Base +6	Channel 4 - Read
Vector Base +8	Channel 1 - Transmit
Vector Base +10	Channel 2 - Transmit
Vector Base +12	Channel 3 - Transmit
Vector Base +14	Channel 4 - Transmit

6.4.2 BOARD CONTROL WRITE (FC = 1)

DATA															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	R	T	X	II

X = Don't Care

Reset (0 = Reset Board)

Test Enable

T1

0 Test Disabled

1 Test Channels 1 and 2

1 Test Channels 3 and 4

Interrupt Inhibit

0 = Inhibit

1 = Enable

The board interrupt for all channels is controlled by the Interrupt Inhibit bit (Bit 0). The Test Enable bit (Bit 2) is set during the execution of a diagnostic program in the ISOLITE ROM. The Reset bit (Bit 3) resets the board and all UARTs.

6.5 CONTROL FORMAT READ (FC = 0)

ADDRESS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	—Device Address—					X	X	0

X = Don't Care

The control read is accomplished with a Sense and Skip True (SST) instruction. After a channel test enable has been set using a SELP instruction, an SST instruction is used to determine if an ISOLITE ROM diagnostic program should be executed (yes if true).

6.6 Update Interrupt Status

In response to an Update Interrupt Status (UIS) instruction, the Event Inhibit latch will be set if address bit 13 is a logical one. The Event Inhibit latch prevents interrupt requests from asserting IUR so no interrupts are generated by the board. Both the Event Inhibit and Board Interrupt Inhibit latches must be reset to generate an interrupt.

6.7 Software General Procedures

Two procedures for communication with each channel are used during a power-up and data transfer routines.

6.7.1 Power-Up

The four UART'S on the board will be held in the reset state whenever power is applied to the 2/4 Channel Serial I/O Board. The following procedure is recommended for initializing the board.

- Clear the Board Reset by setting data bit 03 in the Function Decode Latch to a logical one (DB 3 = 1). See paragraph 6.4.2 of the Hardware Engineering Spec.
- Write the appropriate data word into the Mode Register of the channel/channels selected.

- c) Finally, write the desired data word into the Control Register of the selected channel.

6.7.2 Data Transfer

Check the status register of the UART before a data transfer to determine any error conditions.

Note: Do not disable the Transmit Enable bit of the control word (see paragraph 6.2.2) during transmission of a character. Transmission will terminate immediately.

6.8 Auto I/O

The 2/4 channel serial I/O board does not support auto I/O.

7.0 Testing Capabilities

Functional testing of the 2/4 channel serial I/O board is possible by transmitting data between two channels and checking for data and channel errors. During the execution of a diagnostic program in the ISOLITE ROM, Test Enable bit 2 (paragraph 6.4.2) is set and data is transmitted between channels one and two. The procedure is repeated with Test Enable bit 2 for channels three and four. When either test is enabled, all UART baud rates are automatically set to 9600. During the execution of an ISOLITE Diagnostic program, a test is made to detect the presence of a test cable on J1. If the cable is present then the data path is through the RS-232 drivers/receivers and the transmit channel's Request To Send is returned to its Clear To Send. (DTR and DSR are not connected.) Detection of the cable is made by executing a SST instruction after setting the Test Enable bit. A logical one on DB00 indicates the cable is connected. However, if the cable is not present then the data path is through a set of multiplexers and the RS-232 drivers/receivers are not functionally tested. The cable will not normally be used by a customer for an ISOLITE test.

8.0 Power Requirements

All power for the 2/4 channel serial I/O board is supplied by the five-volt power supply.

8.1 DC to DC Converters

DC to DC Converters provide the required +12 volts and -12

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volts for the RS-232 drivers.

8.2 Power Consumption

Power consumption is dependent upon the population of the board.

- a) Two channels: 1.14 amps (typical)
1.74 amps (maximum)
- b) Four channels: 1.34 amps (typical)
2.02 amps (maximum)

9.0 Environmental

The 2/4 channel serial I/O board will operate in an environment of 0° to 50°C . and from 5% to 90% relative humidity, non-condensing.

10.0 Connector Pin Identification

There are five connectors on the board. P1 is an edge connector to the mother board and J1-J4 are cable connectors for serial I/O devices.

10.1 P1 SCOUT Bus Connector

P1 follows the standard SCOUT bus pin assignments. (See SCOUT Bus specification 099-0001.)

10.2 J1-J4 Serial I/O Connectors

J1-J4 have the same pin out for channels one through four respectively.

<u>J1</u> <u>Pin Number</u>	<u>Signal</u> <u>Name</u>
1	Test
2	Data Terminal Ready
3	Transmit Data
4	Receive Data
5	Clear to Send
6	Data Set Ready
7	Ground
8	Not Used
9	Not Used
10	Request To Send

Note: Recommended mating J1 connector part number is Berg double row conn. housing. P/N 65043-032, loose pins, crimp, 40 μ gold over nickel P/N 47745.